30 **NANOTECHNOLOGY RELATED INTEGRATED CIRCUIT DESIGN**
50 **DESIGN OF SEMICONDUCTOR MASK OR RETICLE**
51 .Analysis and verification (process flow, inspection)
52 ..Defect (including design rule checking)
53 ..Optical proximity correction (including RET)
54 .Manufacturing optimizations
55 .Layout generation (polygon, pattern feature)
56 .Yield
100 **INTEGRATED CIRCUIT DESIGN PROCESSING**
101 .Logic design processing
102 ..Design entry
103 ..Translation (logic-to-logic, logic-to-netlist, netlist processing)
104 ..Logic circuit synthesis (mapping logic)
105 ...With partitioning
106 ..Design verification (functional simulation, model checking)
107 ...Equivalence checking
108 ...Timing verification (timing analysis)
109 ...Power estimation
110 .Physical design processing
111 ..Verification
112 ...Defect Analysis
113 ...Timing Analysis
114 ....Buffer or repeater insertion
115 ...Noise (e.g., crosstalk, electromigration, etc.)
116 ..Mapping circuit design to programmable logic devices (PLDs)
117 ...Configuring PLDs (including data file, bitstream generation, etc.)
118 ..Floorplanning
119 ...Placement or layout
120 ....Power distribution
121 ....For PLDs
122 ....Constraint-based
123 ....Iteration
124 ....With partitioning
125 ...With partitioning
126 ..Routing
127 ...Power (voltage islands)
128 ...PLDs
129 ...Global
130 ...Detailed
131 ...With partitioning
132 .Optimization
133 ..For power
134 ..For timing
135 ..For area
136 .Testing or Evaluating
137 .PCB, MCM Design
138 .System-on-chip design
139 .Layout editor (with ECO, reuse, GUI)

FOREIGN ART COLLECTIONS

FOR 000 **CLASS-RELATED FOREIGN DOCUMENTS**

Any foreign patents or non-patent literature from subclasses that have been reclassified have been transferred directly to FOR Collections listed below. These Collections contain ONLY foreign patents or non-patent literature. The parenthetical references in the Collection titles refer to the abolished subclasses from which these Collections were derived.

FOR 100 **CIRCUIT DESIGN (716/1)**
FOR 101 .Optimization (e.g., redundancy, compaction) (716/2)
FOR 102 .Translation (e.g., conversion, equivalence) (716/3)
FOR 103 .Testing or evaluating (716/4)
FOR 104 ..Design verification (e.g., wiring line capacitance, fanout checking, minimum path width) (716/5)
FOR 105 ...Timing analysis (e.g., delay time, path delay, latch timing) (716/6)
FOR 106 .Partitioning (e.g., function block, ordering constraint) (716/7)
FOR 107 .Floorplanning (716/8)
FOR 108 ..Detailed placement (i.e., iterative improvement) (716/9)

FOR 109 ..Constraint-based placement (e.g., critical block assignment, delay limits, wiring capacitance) (716/10)
FOR 110 ..Layout editor (e.g., updating) (716/11)
FOR 111 .Routing (e.g., routing map, netlisting) (716/12)
FOR 112 ..Global routing (e.g., shortest path, dead space, or duplicate trace elimination) (716/13)
FOR 113 ..Detailed routing (e.g., channel routing, switch box routing((716/14)
FOR 114 ..PCB wiring (716/15)
FOR 115 ..PLA, PLD, FPGA, OR MCM (716/16)
FOR 116 .Programmable integrated circuit (e.g., basic cell, standard cell, macrocell) (716/17)
FOR 117 .Logical circuit synthesizer (716/18)
FOR 118 **DESIGN OF SEMICONDUCTOR MASK (716/19)**
FOR 119 .Mesh generation (716/20)
FOR 120 .Pattern exposure (716/21)

APPLICATIONS (364/400)

FOR 489 .Circuit design and analysis (364/489)
FOR 490 ..Integrated (364/490)
FOR 491 ...Layout (364/491)