## CLASS 714 ERROR DETECTION/CORRECTION AND FAULT DETECTION/RECOV- 714 - 1 ERY

100	DATA PROCESSING SYSTEM ERROR OR	13	Prepared backup processor
	FAULT HANDLING		hackup) or undating backup
1	.Reliability and availability		processor (e.g. by checkpoint
2	Fault recovery		message)
3	By masking or reconfiguration	1 /	Of power gupply
4.1	Of network	15	
4.11	Backup or standby (e.g.,	10	or data file)
	tallover, etc.)	16	Forward recovery (e.g.,
4.12	Hot swapping (i.e., while	10	redoing committed action)
	network is up)	17	Reevecuting single
4.2	Isolate or remove failed	± /	instruction or bus cycle
	node without replacement	10	monomiagion data regard
	(e.g., bypassing, re-routing,	ΤO	(a m for not constant is a con
	etc.)	1.0	(e.g., for retransmission)
4.21	Reintegrate node back into	19	Undo record
	network	20	Plural recovery data sets
4.3	Repair failed node without		containing set interrelation
	replacement (i.e., on-line		data (e.g., time values or log record numbers)
	repair)	21	State validity check
4.4	Remote repair	22	With nower supply status
4.5	<pre>Bus network (e.g., PCI, AGP, etc.)</pre>	22	monitoring
5.1	Of peripheral subsystem	23	Resetting processor
5.11	Access processor affected	24	Safe shutdown
0.11	(e.g., I/O processor, MMIL or	25	Fault locating (i.e., diagnosis
	DMA processor etc.)		or testing)
6 1	Of momory	26	Artificial intelligence (e.g.,
6 11	Within single memory device		diagnostic expert system)
0.11	(a gradial atg.)	27	Particular access structure
C 10	(e.g., disk, etc.)	28	Substituted emulative
6.12	Recovery partition		component (e.g., emulator
6.13	Isolating failed storage		microprocessor)
	location (e.g., sector	29	Memory emulator feature
	remapping, etc.)	30	Built in hardware for
6.2	Plurality of memory devices	50	diagnoging or togting within
	(e.g., array, etc.)		diagnosing of testing within-
6.21	Array controller		system component (e.g.,
6.22	RAID		microprocessor test mode
6.23	Mirror (i.e., level 1	21	circuit, scan path)
	RAID)	31	Additional processor for in-
6.24	ECC, parity, or fault code		system fault locating (e.g.,
-	(i.e., level 2+ BAID)		distributed diagnosis program)
63	Backup or standby (e g	32	Particular stimulus creation
0.5	failower eta )	33	Derived from analysis (e.g.,
6 21			of a specification or by
0.31	Remote repair		stimulation)
6.32	Replacement of failed	34	Halt, clock, or interrupt
	memory device		signal (e.g., freezing,
10	Of processor		hardware breakpoint, single-
11	Concurrent, redundantly		stepping)
	operating processors	35	Substituted or added
12	Synchronization maintenance	-	instruction (e.g., code
	of processors		instrumenting, breakpoint
			instruction)

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36	Test sequence at power-up or initialization	701	.Data formatting to improve error detection correction
37	Analysis (e.g., of output,	700	capability
201	state, or design)	102	Memory access (e.g., address
38.1	Of computer software faults	702	permutation)
38.11	Memory dump	703	l'esting of error-check system
38.12	Time-out (i.e., of program)	704	.Error count or rate
38.13	Interrupt (i.e., halt the	705	Pseudo-error rate
	program)	706	Up-down counter
38.14	By remotely	707	Synchronization control
39	Monitor recognizes sequence	708	Shutdown or establishing system
	of events (e.g., protocol or logic state analyzer)		parameter (e.g., transmission rate)
40	Component dependent technique	709	.Data pulse evaluation/bit
41	For reliability enhancing		decision
	component (e.g., testing backup spare, or fault	710	.Replacement of memory spare location, portion, or segment
	injection)	711	Spare row or column
42	Memory or storage device	712	.Transmission facility testing
	component fault	713	For channel having repeater
43	Bus, I/O channel, or network	714	By tone signal
	path component fault	715	Test pattern with comparison
44	Peripheral device component	716	Loop-back
	fault	717	Loop or ring configuration
45	Output recording (e.g.,	718	.Memory testing
	signature or trace)	719	Read-in with read-out and
46	Operator interface for		compare
	diagnosing or testing	720	Special test pattern (e.g.,
47.1	Performance monitoring for	•	checkerboard, walking ones)
	fault avoidance	721	Electrical parameter (e.g.,
47.2	Threshold		threshold voltage)
47.3	Trends (i.e., expectancy)	722	Performing arithmetic function
48	Error detection or notification		on memory contents
49	State error (i.e., content of	723	Error mapping or logging
	instruction, data, or message)	724	.Digital logic testing
50	State out of sequence	725	Programmable logic array (PLA)
51	Control flow state sequence	. 20	testing
	monitored (e.g., watchdog	726	Scan path testing (e.g., level
	processor for control-flow		sensitive scan design (LSSD))
	checking)	727	Boundary scan
52	Error checking code	728	Random pattern generation
53	Address error		(includes pseudorandom
54	Storage content error		pattern)
55	Timing error (e.g., watchdog	729	Plural scan paths
	timer time-out)	730	Addressing
56	Bus or I/O channel device	731	Clock or synchronization
	fault	732	Signature analysis
57	Error forwarding and	733	Built-in testing circuit
	presentation (e.g., operator		(BILBO)
	console, error display)	734	Structural (in-circuit test)
699	PULSE OR DATA ERROR HANDLING	735	Device response compared to
700	.Skew detection correction		input pattern

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737      Device response compared to       DRAM's)         738      Including test pattern       memory address         739      Random pattern generation       770      Disk strarg         739      Random pattern generation       771      Disk strarg         740      Simulation       771      Solid state memory         741      Simulation       774      Adaptive error-correcting         742      Code word parallel access      Synchronization         744      Clock or synchronization       776      For packet or frame         744      Clock or synchronization       776      For packet or frame         744      Clock or synchronization       776      For packet or frame         744      Clock or synchronization       776      For packet or frame         747      Subsitution of previous valid       780      For packet or frame         748      Request for retransmission       781      For backet or frame         749      Retransmission if no ACK      Boee Chaudhuri Hocquenghem         751      Retransmission if no ACK      Boee Chaudhuri Hocquenghem         751      Louding forward error      Gode based	736	Device response compared to expected fault-free response	767	<pre>Code word for plural n-bit  (n&gt;1) storage units (e.g., x4</pre>
<ul> <li>Fault Gigtionary/Fruth table</li> <li>Fault Gigtionary</li> <li>Fault Gigti</li></ul>	737	Device response compared to	760	DRAM's)
generator     769    Dynamic data storage       739    Bandom pattern generation     770    Disk array       740    Having analog signal     773    Solid state memory       741    Simulation     774    Solid state memory       742    Festing specific device     capability       743    Solid state memory       744    Solid state memory       745    Beternination of marginal     multiplexed data       operation limits     777    Nonbinary data (e.g., ternary)       746     .Digital data error correction     778    Nonbinary data (e.g., ternary)       747    Substitution of previous valid     779    Variable length data       748    Request for retransmission     Information (e.g., soft       750    Feedback to transmitter for     polynomial       returned     781    Code based on generator       751    Forevard correction by block     784       752    Forward correcting with     786       753    Bouble error correcting with     781       754    Error correcting code     787       755    Bouble error correcting code     787       756    Double error correcting code     787       757     <	738	fault dictionary/truth table Including test pattern	/08	memory address
739      Bandom pattern generation       770      Disk array         740      Code word parallel access         741      Simulation       774      Solid state memory         741      Simulation       774      Adaptive error-correcting         742      Testing specific device       capability         743      Clock or synchronization       776      Norp tacket or frame         744      Clock or synchronization       776      Nonbinary data (e.g., ternary)         744      Clock or synchronization       778      Nonbinary data (e.g., ternary)         747      Substitution of previous valid       779      Variable length data         748      Retransmission if no ACK       decision)      Code based on generator         750      Feedback to transmitter for       polynomial      Golay code         751      Forward correction by block       784      Golay code         752      Forward correcting with       786      Synchronization         753      Beads and burst error      Bynchron code         754      Forward correcting with       786      Code based on generator         754      Renocoling codes (e.g.,		generator	769	Dynamic data storage
(includes pseudorandom771Tapepattern)772Code word parallel access740Baving analog signal773Solid state memory741Simulation774Addressing742Testing specific devicecapability743Addressing775Synchronization744Clock or synchronization776Synchronization745Determination of marginalmultiplexed dataoperation limits777Nonbinary data (e.g., ternary)747Substitution of previous valid779Variable length data748Request for retransmissionLing symbol reliability749Retransmission if no ACK781Code based on generator750Feedback to transmitter forpolynomial751Including forward errorBose Chaudhuri Hocquenghem752Forward correction by block784Rede-Solomon code753Double error correcting with780Rendom and burst errors754Error correcting dode787Random and burst errors755Double encoding codes (e.g.,788Synchronization756Colay code787Random and burst error757Duble encoding codes (e.g.,788Syndrome computed758Double error correcting with790Forward error759Duble encoding codes (e.g.,788Burst error759Dubl	739	Random pattern generation	770	Disk array
pattern)772Code word parallel access740Having analog signal773Solid state memory741Simulation774Adaptive error-correcting742Addresing775Synchronization743Addresing775Synchronization744Clock or synchronization776Synchronization745Determination of marginalmultiplexed data746Determination of previous valid778Nonbinary data (e.g., ternary)747Substitution of previous valid780Variable length data748Request for retransmission780Variable length data750Feedback to transmitter for comparison781Code based on generator751Including forward error codecodeSynchronic code753Double error correcting with single error correcting code787Read-Bolmon code754Error correcting code781Coola y code755Double error correcting codeSynchronization756Double error correcting code781Synchronization756Double error correcting codeSynchronization757Farallel generation of check bits792Synchronization759Double error correcting code with yroduct, concatenated)789Synchronization757Farallel generation of check bits792Synchronization759Double erro		(includes pseudorandom	771	Tape
740      Iaving analog signal       773      Solid state memory         741      Simulation       774      Addprive error-correcting         742      Addressing       775      Synchronization         744      Olcok or synchronization       776      For packet or frame         745      Determination of marginal       multiplexed data         746      Digital data error correction       777      Nonbinary data (e.g., ternary)         747      Substitution of previous valid       779      Variable length data         748      Request for retransmission      Using symbol reliability         749      Request to transmitter for       polynomial         750      Freadback to transmitter for       code         751      Including forward error       code         752      Forward correcting yold       783        Berer correcting with       785      Forward error correcting yold         753      Double error correcting code       785      Forward errors         754      Error correcting code with       786      Forward errors         755      Double encoding codes (e.g.,       788      Synchronization         756 <td></td> <td>pattern)</td> <td>772</td> <td>Code word parallel access</td>		pattern)	772	Code word parallel access
741      Simulation       774      Adaptive error-correcting capability         742      Testing specific device      Synchronization         743      Addressing       775      Synchronization         744      Clock or synchronization       776      Synchronization         745      Determination of marginal       multiplexed data         0peration limits       777      Naming code         746      Synchronization ender       778      Nonbinary data (e.g., ternary)         747      Substitution of previous valid       779      Variable length data         748      Request for retransmission       780      Using symbol reliability         749      Retransmission if no ACK       decision)      Code based on generator         750      Feedback to transmitter for       polynomial      Code         751      Including forward error       783      Golay code         753      Double error correcting with       786      Syndrome computed         754      Fore acnetated)       789      Supdromization         755      Double encoding codes (e.g., 788      Burst error      Sequential decoder (e.g., Fano         756	740	Having analog signal	773	Solid state memory
742    Testing specific device     capbility       743    Addressing     775    Synchronization       744    Clock or synchronization     776    For packet or frame       745    Determination of marginal     multiplexed data       746     .Digital data error correction     778    Wainble length data       747    Substitution of previous valid     779    Variable length data       748    Request for retransmission    Using symbol reliability       749    Retransmission if no ACK     decision       750    Freedback to transmitter for    Code based on generator       751    Including forward error     code       752    Forward correcting with 786    Forward error correcting code       753    Double error correcting code     785       754    Error correcting code     780       755    Double encoding codes (e.g., 788    Burst error       756    Cross-interleave Reed-Solomon     790       757    Parallel generation of check     792       758    Double encoding code (e.g., 788    Burst error       759    Double encoding or 796    Syndrome decoder (e.g., 780       750    For and correction during    Syndromi decoder (e.g., 780 <td>741</td> <td>Simulation</td> <td>774</td> <td>Adaptive error-correcting</td>	741	Simulation	774	Adaptive error-correcting
743      Addressing       775      Synchronization         744      Clock or synchronization       776      For packet or frame         745      Determination of marginal       multiplexed data         0peration limits       777      Nonbinary data (e.g., ternary)         747      Substitution of previous valid       778      Nonbinary data (e.g., ternary)         747      Substitution of previous valid       779      Variable length data         748      Request for retransmission       780      Using symbol reliability         749      Retransmission if no ACK       781      Code based on generator         750      Feedback to transmitter for       rolynomial      Code based on generator         751      Including forward error       code      Bose-Chaudhuri-Hocquenghem         correction capability       781      Code based on generator         753      Double error correcting with       786      Forward error correction by         754      Error correcting code      Synchronization      Synchronization         755      Double encoding codes (e.g.,       788      Burst error         756      Cross-interleave Reed-Solomon       790      Furc	742	Testing specific device		capability
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745      Determination of marginal operation limits       multiplexed data         746       Digital data error correction       778         747      Substitution of previous valid       779         748      Request for retransmission       780         749      Request for retransmission       780         740      Request for retransmission       780         750      Retransmission if no ACK       decision)         751      Including forward error      Bose Chaudhuri-Hocquenghem         752      Forward error      Bose Chaudhuri-Hocquenghem         753      Duble error correcting with       786      Bose Chaudhuri-Hocquenghem         754      Forward error correcting with       786      Bordrame computed         755      Duble error correcting code      Synchronization      Bose Chaudhuri Hocquenghem         756      Duble encoding codes (e.g., 788      Burst error      Synchronization         756      Duble encoding codes (e.g., 788      Burst error      Gode (e.g., Fano         757      Parallel generation of check      Synchronization      Synchromization         758      Dubue error detection       790      Furor correcting code with	744	Clock or synchronization	776	For packet or frame
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747      Substitution of previous valid data       779      Variable length data         748      Request for retransmission       780      Using symbol reliability         749      Retransmission if no ACK returned       781      Code based on generator polynomial         750      Feedback to transmitter for correction capability       781      Code based on generator polynomial         751      Including forward error correction capability       783      Golay code         752      Forward correcting with single error correcting code       786      Syndrome computed         753      Double error correcting code       787      Random and burst errors         754      Feror correcting codes       788      Burst error         755      Double encoding codes (e.g., product, concatenated)       789      Synchronization         756      Forror correcting code with bits       792      Syndrome decodable (e.g., self orthogonal)         756      Error correcting code with additional error detection code (e.g., cyclic redundancy character, parity)       794      Maximum likelihood character, parity         759      Look-up table encoding (e.g., majority logic)       797      Faror detection for synchronization control         761      Random and burst error corr	746	.Digital data error correction	778	Nonbinary data (e.g., ternary)
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748      Request for retransmission      Information (e.g., soft decision)         749      Retransmission if no ACK       decision)         740      Retransmission if no ACK       decision)         750      Feedback to transmitter for comparison       782      Gode based on generator polynomial         751      Including forward error      Golay code      Golay code         752      Forward correction by block       784      Golay code         753      Double error correcting code       785      Spndrome computed         754      Error correcting duding       convolutional)       ref cesh cycle         755      Double encoding codes (e.g., 788      Burst error       product, concatenated)         756      Cross-interleave Reed-Solomon       790      Sequential decoder (e.g., Fano or stack algorithm)         758      Error correcting code with 793      Syndrome decodable (e.g., self orthogonal)         759      Devup table encoding or 796      Fror detection correction for majority logic)      Syndrome decoding         759      Doubu error correction       791      Sequential decoding      spinorization control         760      Fror correcting code with 793      Supdrome decodable (e.g., self orthogona		data	780	Using symbol reliability
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returned 781Code based on generator polynomial comparison 782Code based on generator polynomial comparison 782Code based on generator polynomial code 785Bose-Chaudhuri-Hocquenghem code 785Syndrome computed Syndrome computed Puncturing code (CIRC) 791Sequential decoder (e.g., Fano or stack algorithm) bits 792Fror correcting code with additional error detection code (e.g., cyclic redundancy 794Maximum likelihood character, parity) 795Viterbi decoding Iook-up table encoding or 796Branch metric calculation decoding 797Maximum likelihood correction 800Parity bit Threshold decoding (e.g., 798 Error detection for majority logic) Error correct and restore 802Parity generator or checker circuit detail Parity generator or checker circuit detail Parity prediction Error pointer 803Parity prediction Parity prediction Parity prediction Parity prediction Parity prediction Parity prediction Parity check area of memory 805Storage accessing (e.g., address parity check)	749	Retransmission if no ACK		decision)
750Feedback to transmitter for comparison782Bose-Chaudhuri-Hocquenghem code751Including forward error correction capability783Golay code752Forward correction by block code784Reed-Solomon code753Double error correcting with single error correcting code786Syndrome computed754Error correction during refresh cycle787Random and burst errors755Double encoding codes (e.g., product, concatenated)789Synchronization756Cross-interleave Reed-Solomon code (CIRC)791Sequential decoder (e.g., Fano or stack algorithm)757Fror correcting code with additional error detection code (e.g., cyclic redundancy refrashed decoding792Trellis code759Look-up table encoding or additional error correction decoding794Maximum likelihood760Threshold decoding (e.g., majority logic)795Maximum likelihood761Random and burst error synchronization control799Furor detection for synchronization control762Burst error correction address parity logic794Barity generator or checker circuit755Double encoding or address parity check area of memory794Burst error correction755Double encoding (e.g., majority logic)795Fror detection for synchronization control756Error correction majority logic)Burst error correction	/ 15	returned	781	Code based on generator
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752      Forward correction by block code       784      Reed-Solomon code         753      Double error correcting with single error correcting code       785      Syndrome computed         754      Error correction during refresh cycle       787      Rendom and burst errors         755      Double encoding codes (e.g., product, concatenated)       789      Synchronization         756      Cross-interleave Reed-Solomon bits       791      Sequential decoder (e.g., Fano or stack algorithm)         757      Parallel generation of check bits       792      Trellis code         758      Error correcting code with additional error detection code (e.g., cyclic redundancy decoding       794      Maximum likelihood         759      Look-up table encoding or majority logic)       795      Viterbi decoding         761      Random and burst error majority logic)       798      Fror detection for synchronization control         762      Encom and burst error majority logic)       794      Maximum likelihood         763      Look-up table encoding or decoding       797      Branch metric calculation decoding         764      Evror correction       801      Parity generator or checker circuit detail         764      Evror pointer       803	191	correction canability	783	Golay, code
752Near753Nearcode785Near753Double error correcting with single error correcting code786Forward error correction by tree code (e.g., convolutional)754Error correcting during refresh cycle787Random and burst errors755Double encoding codes (e.g., product, concatenated)789Synchronization756Cross-interleave Reed-Solomon ocde (CIRC)791Sequential decoder (e.g., Fano or stack algorithm)757Parallel generation of check bits792Trellis code758Error correcting code with additional error detection code (e.g., cyclic redundancy decoding794Syndrome decodable (e.g., self orthogonal)759Look-up table encoding or decoding796Branch metric calculation synchronization control760Threshold decoding (e.g., majority logic)797Majority decision/voter circuit761Random and burst error correction799.Error/fault detection technique correction for synchronization control762Burst error correct and restore 63803Parity generator or checker circuit detail763Error pointer803Parity prediction764Error pointer803Parity prediction765Error pointer803Parity prediction766Error pointer803Parity prediction766Error pointer803Parity prediction	752	Forward correction by block	78/	Pood Solemon codo
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<ul> <li>754Error correction during convolutional)</li> <li>refresh cycle</li> <li>787Random and burst errors</li> <li>755Double encoding codes (e.g., 788Burst error product, concatenated)</li> <li>789Synchronization</li> <li>756Cross-interleave Reed-Solomon 790Puncturing code (CIRC)</li> <li>791Sequential decoder (e.g., Fano or stack algorithm)</li> <li>758Error correcting code with 793Syndrome decodable (e.g., self orthogonal)</li> <li>759Look-up table encoding or 796Branch metric calculation decoding 797Najority decision/voter circuit</li> <li>760Threshold decoding (e.g., 798Fror detection for majority logic)</li> <li>761Random and burst error 799Parity bit</li> <li>762Burst error correction 801Parity generator or checker circuit detail</li> <li>764Error pointer 803Parity prediction</li> <li>766Check bits stored in separate 804Plural dimension parity check area of memory</li> <li>765Error gaity 804</li> </ul>	155	single error correcting code	700	tree code (e a
<ul> <li>1.1. Infor Correction during</li> <li>refresh cycle</li> <li>787</li> <li>Random and burst errors</li> <li>product, concatenated)</li> <li>789</li> <li>Burst error</li> <li>product, concatenated)</li> <li>789</li> <li>Burst error</li> <li>product, concatenated)</li> <li>789</li> <li>Synchronization</li> <li>Puncturing</li> <li>code (CIRC)</li> <li>791</li> <li>Sequential decoder (e.g., Fano</li> <li>or stack algorithm)</li> <li>bits</li> <li>792</li> <li>Trellis code</li> <li>Syndrome decodable (e.g., self</li> <li>orthogonal)</li> <li>code (e.g., cyclic redundancy</li> <li>character, parity)</li> <li>796</li> <li>Look-up table encoding or</li> <li>decoding</li> <li>Random and burst error</li> <li>majority logic)</li> <li>761</li> <li>Random and burst error</li> <li>799</li> <li>Look-up table error</li> <li>majority logic)</li> <li>761</li> <li>Random and burst error</li> <li>correction</li> <li>801</li> <li>Parity generator or checker</li> <li>circuit detail</li> <li>764</li> <li>Error correct and restore</li> <li>802</li> <li>Even and odd parity</li> <li>referst calculation</li> <li>Parity prediction</li> <li>Check bits stored in separate</li> <li>804</li> <li>Purity check)</li> </ul>	754	Error correction during		convolutional)
<ul> <li>755Double encoding codes (e.g., product, concatenated)</li> <li>756Cross-interleave Reed-Solomon code (CIRC)</li> <li>791Sequential decoder (e.g., Fano or stack algorithm)</li> <li>757Parallel generation of check or stack algorithm)</li> <li>758Error correcting code with additional error detection code (e.g., cyclic redundancy 794Maximum likelihood character, parity)</li> <li>795Look-up table encoding or 796Franch metric calculation decoding 797Majority decision/voter circuit</li> <li>760Threshold decoding (e.g., majority logic)</li> <li>761Random and burst error 799Parity generator or checker circuit detail</li> <li>762Burst error correction 801Parity generator or checker circuit detail</li> <li>764Error pointer 802Even and odd parity 765Check bits stored in separate 804Plural dimension parity check area of memory 800</li> </ul>	734	refresh cycle	787	Random and burst errors
<ul> <li>1.1. Double encoding codes (erg., product, concatenated)</li> <li>756Cross-interleave Reed-Solomon</li> <li>790Parallel generation of check bits</li> <li>792Trellis code</li> <li>758Error correcting code with additional error detection code (e.g., cyclic redundancy code (e.g., cyclic redundancy reduct) additional error detection decoding</li> <li>759Look-up table encoding or reduction decoding</li> <li>760Threshold decoding (e.g., reduct) reduction for synchronization control</li> <li>761Random and burst error reduction synchronization correction</li> <li>762Euror correction</li> <li>763Euror correct and restore</li> <li>764Error correct and restore</li> <li>765Error pointer</li> <li>766Check bits stored in separate area of memory</li> <li>805Euror coresting code site sparate and memory</li> <li>765Error pointer</li> <li>766Check bits stored in separate</li> <li>766Check bits stored in separate</li> <li>766Euror pointer</li> <li>767Euror pointer</li> <li>768Euror correction</li> <li>769Euror pointer</li> <li>760Check bits stored in separate</li> <li>760Euror pointer</li> <li>761Euror pointer</li> <li>762Euror pointer</li> <li>763Euror pointer</li> <li>764</li></ul>	755	Double encoding codes (e g	788	Burst error
756Cross-interleave Reed-Solomon code (CIRC)790Puncturing757Parallel generation of check bits791Sequential decoder (e.g., Fano or stack algorithm)758Parallel generation of check bits792Trellis code758Error correcting code with additional error detection code (e.g., cyclic redundancy character, parity)793Syndrome decodable (e.g., self orthogonal)759Look-up table encoding or decoding796Branch metric calculation synchronization control760Threshold decoding (e.g., majority logic)798.Error detection for synchronization control761Random and burst error correction799Parity generator or checker circuit detail763Memory access801Parity prediction764Error pointer803Parity prediction765Check bits stored in separate area of memory804Plural dimension parity check address parity check)	155	product concatenated)	789	Symphronization
750	756	Cross_interleave Reed_Solomon	790	Puncturing
757Parallel generation of check bits791Sequencial decoder (e.g., Failo or stack algorithm) or stack algorithm)758Error correcting code with additional error detection code (e.g., cyclic redundancy character, parity)792Trellis code759Look-up table encoding or decoding794Maximum likelihood or thogonal)Maximum likelihood759Look-up table encoding or decoding797Majority decision/voter circuit760Threshold decoding (e.g., majority logic)798.Error detection for synchronization control761Random and burst error correction799.Error/fault detection technique correction technique circuit detail762Burst error correct and restore 63801Parity generator or checker circuit detail764Error pointer803Parity prediction765Check bits stored in separate area of memory804Plural dimension parity check address parity check)	750	code (CIPC)	701	Compartial decoder (e.g. Eano
1.1. Interference of the construction of the const	757	Parallel generation of check	191	or stack algorithm)
758Error correcting code with additional error detection code (e.g., cyclic redundancy character, parity)793Syndrome decodable (e.g., self orthogonal)759Look-up table encoding or decoding796Maximum likelihood other decoding760Threshold decoding (e.g., majority logic)797Majority decision/voter circuit761Random and burst error correction799Parity bit762Burst error correction800Parity bit763Memory accesscircuit detail764Error pointer803Parity prediction765Error pointer804Pural dimension parity check area of memory805766Check bits stored in separate area of memory805Storage accessing (e.g., address parity check)	151	hite	700	Trollia and
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code (e.g., cyclic redundancy character, parity)794Maximum likelihood character, parity)759Look-up table encoding or decoding796Branch metric calculation decision/voter circuit760Threshold decoding (e.g., majority logic)797Majority decision/voter circuit synchronization control761Random and burst error correction799.Error/fault detection technique correction technique solution762Burst error correction801Parity generator or checker circuit detail764Error pointer802Even and odd parity765Check bits stored in separate area of memory805Storage accessing (e.g., address parity check)	750	additional error detection	195	orthogonal)
obset (erg.), openite redundancy794Maximum filterinoodcharacter, parity)795Viterbi decoding759Look-up table encoding or decoding796Branch metric calculation760Threshold decoding (e.g., majority logic)797Majority decision/voter circuit761Random and burst error correction799.Error/fault detection technique correction technique time762Burst error correction801Parity bit763Memory accessError pointer802764Error pointer803Parity prediction765Error pointer803Parity prediction766Check bits stored in separate area of memory805Storage accessing (e.g., address parity check)		code (e.g., cyclic redundancy	791	Maximum likelihood
<ul> <li>759Look-up table encoding or decoding</li> <li>760Threshold decoding (e.g., majority logic)</li> <li>761Random and burst error 799 .Error/fault detection technique correction</li> <li>762Burst error correction</li> <li>763Memory access</li> <li>764Error pointer</li> <li>765Error pointer</li> <li>766Check bits stored in separate area of memory</li> <li>7790Viterbit decoding</li> <li>796Viterbit decoding</li> <li>796Branch metric calculation</li> <li>797Branch metric calculation</li> <li>798Branch metric calculation</li> <li>799 .Error detection for synchronization control</li> <li>799Parity bit</li> <li>799Branch metric calculation</li> <li>790Branch metric calculation</li> <li>791Branch metric calculation</li> <li>792Branch metric calculation</li> <li>793Branch metric calculation</li> <li>794Branch metric calculation</li> <li>795Branch metric calculation</li> <li>796Branch metric calculation</li> <li>796Branch metric calculation</li> <li>798Branch metric calculation</li> <li>799Branch metric calculation</li> <li>790Branch met</li></ul>		character, parity)	794	Maximum TIKeTINOOd
7551.1.1601 up claste encoding of decoding7961.1.Branch metric calculation detric calculation760Threshold decoding (e.g., majority logic)797Majority decision/voter circuit .Error detection for synchronization control761Random and burst error correction799.Error/fault detection technique oParity bit762Burst error correction801Parity generator or checker circuit detail763Memory access802Erven and odd parity765Error pointer803Parity prediction766Check bits stored in separate area of memory804Storage accessing (e.g., address parity check)	759	Look-up table encoding or	795	Viterbi decoding
760Threshold decoding (e.g., majority logic)797Majority decision/voter circuit761Random and burst error correction799.Error detection for synchronization control761Random and burst error correction799.Error/fault detection technique correction technique time762Burst error correction801Parity bit763Memory accesscircuit detail764Error correct and restore802Even and odd parity765Error pointer803Parity prediction766Check bits stored in separate area of memory805Storage accessing (e.g., address parity check)	135	decoding	790	Branch metric calculation
760	760	Threshold decoding (e a	797	Majority decision/voter circuit
761Random and burst error 799 .Error/fault detection technique correction 800Parity bit 762Burst error correction 801Parity generator or checker circuit detail 764Error correct and restore 802Even and odd parity 765Error pointer 803Parity prediction 766Check bits stored in separate 804Plural dimension parity check area of memory 805Storage accessing (e.g., address parity check)	,	majority logic)	190	synchronization control
correction800Parity bit762Burst error correction801Parity generator or checker circuit detail763Memory accesscircuit detail764Error correct and restore802Even and odd parity765Error pointer803Parity prediction766Check bits stored in separate804Plural dimension parity check area of memory805Storage accessing (e.g., address parity check)	761	Random and burst error	799	.Error/fault detection technique
762Burst error correction801Parity generator or checker circuit detail763Memory accesscircuit detail764Error correct and restore802Even and odd parity765Error pointer803Parity prediction766Check bits stored in separate804Plural dimension parity checkarea of memory805Storage accessing (e.g., address parity check)		correction	800	. Parity bit
763      Memory access       circuit detail         764      Error correct and restore       802      Even and odd parity         765      Error pointer       803      Parity prediction         766      Check bits stored in separate area of memory       804      Plural dimension parity check        Storage accessing (e.g., address parity check)      Storage area	762	Burst error correction	801	Parity generator or checker
764      Error correct and restore       802      Even and odd parity         765      Error pointer       803      Parity prediction         766      Check bits stored in separate area of memory       804      Plural dimension parity check        Storage accessing (e.g., address parity check)      Storage accessing (e.g., address parity check)	763	Memory access		circuit detail
765      Error pointer       803      Parity prediction         766      Check bits stored in separate area of memory       804      Plural dimension parity check         805      Storage accessing (e.g., address parity check)	764	Error correct and restore	802	Even and odd parity
766      Check bits stored in separate area of memory       804      Plural dimension parity check         805      Storage accessing (e.g., address parity check)	765	Error pointer	803	Parity prediction
area of memory 805Storage accessing (e.g., address parity check)	766	Check bits stored in separate	804	Plural dimension parity check
address parity check)		area of memory	805	Storage accessing (e.g.
				address parity check)

### 714 - 4 CLASS 714 ERROR DETECTION/CORRECTION AND FAULT DETECTION/RECOV-ERY

806	Constant-ratio code (m/n)
807	Check character
808	Modulo-n residue check
	character
809	Code constraint monitored
810	Multilevel coding (n>2)
811	Forbidden combination or
	improper condition
812	Specified digital signal or
	pulse count
813	Two key-down detector
814	Data timing/clocking
815	Time delay/interval monitored
816	Two-rail logic
817	Noise level
818	Missing-bit/drop-out detection
819	Comparison of data
820	Plural parallel devices of
	channels
821	Transmission facility
822	Sequential repetition
823	True and complement data
824	Device output compared to
	input

#### E-SUBCLASSES

The following subclasses beginning with the letter E are E-subclasses. Each E-subclass corresponds in scope to a classification in a foreign classification system, for example, the European Classification system (ECLA). The foreign classification equivalent to an E-subclass is identified in the subclass definition. In addition to US documents classified in E-subclasses by US examiners, documents are regularly classified in E-subclasses according to the classification practices of any foreign Offices identified in parentheses at the end of the title. For example, "(EPO)" at the end of a title indicates both European and US patent documents, as classified by the EPO, are regularly added to the subclass. E-subclasses may contain subject matter outside the scope of this class.Consult their definitions, or the documents themselves to clarify or interpret titles.

E11.001	ERROR DETECTION; ERROR
	CORRECTION; MONITORING (EPO)
E11.002	.Error detection other than by
	redundancy in data
	representation, operation, or
	hardware, or by checking the
-11 000	order of processing (EPO)
EI1.003	(EPO) (EPO)
E11.004	By count or rate limit, e.g.,
	word- or bit count limit, etc. (EPO)
E11.005	By other limits, e.g., analog
	values, etc. (EPO)
E11.006	By bit configuration check,
	e.g., of formats or tags, etc. (EPO)
E11.007	.Error correction, recovery or
	fault tolerance using at least
	two different redundancy
	techniques and at least one
	technique not involving
<b>E11 000</b>	redundancy (EPO)
EII.008	Fault tolerant soltware (EPO)
EII.009	
	the same number of connections
	per node (EPO)
E11.01	Interconnection networks.
	i.e., comprising
	interconnecting link and
	switching elements (EPO)
E11.011	Fault-tolerant routing (EPO)
E11.012	In rings and buses (EPO)
E11.013	In n-dimensional structures,

- e.g., arrays, trees, cubes,
- etc. (EPO) E11.014 ...Neural networks (EPO)
- E11.015 ..By degradation, i.e., a slowdown occurs but full processing capability is maintained, e.g., discarding a faulty element or unit, etc. (EPO)
- E11.016 .. In systems, e.g., multiprocessors, etc. (EPO)
- E11.017 .Security measures, i.e., ensuring safe condition in the event of error, e.g., for controlling element (EPO)
- E11.018 .Protecting against parasitic influences, e.g., noise, temperatures, etc. (EPO)
- E11.019 .Identification, e.g., of a performed repair, of a defined circuit, etc. (EPO)

## CLASS 714 ERROR DETECTION/CORRECTION AND FAULT DETECTION/RECOV- 714 - 5 ERY

- E11.02 .Reliability or availability analysis (EPO)
- E11.021 .Responding to the occurrence of a fault, e.g., fault tolerance, etc. (EPO)
- E11.022 ..Error or fault processing without redundancy, i.e., by taking additional measures to deal with the error/fault (EPO)
- E11.023 ... Error or fault handling (EPO)
- E11.024 ...Error or fault detection or monitoring (EPO)
- E11.025 ...Error or fault reporting or logging (EPO)
- E11.026 ...Error or fault localization (EPO)
- E11.027 ....By collation, i.e., correlating different errors (EPO)
- E11.028 ....By identifying the faulty software code (EPO)
- E11.029 ... Error or fault analysis (EPO)

E11.03 ..Error detection or correction by redundancy in data representation, e.g., by using checking codes, etc. (EPO)

- E11.031 ... Using codes with inherent redundancy, e.g., n-out-of-m codes (EPO)
- E11.032 ... Adding special bits or symbols to the coded information, e.g., parity check, casting out 9's or 11's, etc. (EPO)
- E11.033 ....Using arithmetic codes i.e., codes which are preserved during operation, e.g., modulo 9 or 11 check, etc. (EPO)
- E11.034 .... In memories (EPO)
- E11.035 ..... In static stores (EPO)
- E11.036 .....Integrated on a chip (EPO)
- E11.037 .....In cache or content addressable memories (EPO)
- E11.038 .....In sector programmable memories, e.g., flash disk, etc. (EPO)
- E11.039 .....In multilevel memories (EPO)
- E11.04 .....To protect a block of data words, e.g., CRC, checksum, etc. (EPO)
- E11.041 .....To protect individual data words written into, or read out of, the addressable memory subsystem of data processing equipment (EPO) E11.042 .....Codes or arrangements adapted for a specific type of error (EPO) E11.043 .....Error in accessing a memory location, i.e., addressing error (EPO) E11.044 .....Error in check bits (EPO) E11.045 .....Identification of the type of error (EPO) E11.046 .....Adjacent error, e.g., error in n-bit (n>1) wide storage units, i.e., package error, etc. (EPO) E11.047 .....Simple parity (EPO) E11.048 .....Unidirectional errors (EPO) E11.049 .....Arrangements adapted for a specific error detection or correction feature (EPO) E11.05 .....Bypassing or disabling error detection or correction (EPO) E11.051 .....Updating check bits on partial write, i.e., read/ modify/write (EPO) E11.052 .....Correcting systematically all correctable errors, i.e., scrubbing (EPO) E11.053 .... Using single parity bit (EPO) E11.054 .. Error detection or correction of the data by redundancy in hardware (EPO) E11.055 ... Error detection by comparing the output signals of redundant hardware (EPO) E11.056 .... In static storage, e.g., matrix, registers, etc. (EPO) E11.057 .... In coding, decoding circuits, e.g. parity circuits (EPO) E11.058 .... In communications, e.g., transmission, interfaces, etc. (EPO) E11.059 ....Control processors, e.g., for sensors, actuators, etc. (EPO) E11.06 ....With exchange of data between units (EPO) E11.061 ....With data processors, i.e., data processors compare their

computations (EPO)

### 714 - 6 CLASS 714 ERROR DETECTION/CORRECTION AND FAULT DETECTION/RECOV-ERY

- E11.062 ....In storage with relative movement between record carrier and transducer, e.g., tapes, disks, etc. (EPO)
- E11.063 .... In systems, i.e. comprising a multiplicity of resources, e.g., cpu with its memory and I/O, etc. (EPO)
- E11.064 ....In arithmetic, logic or counter circuits or a combination thereof, e.g., alu, adder, etc. (EPO)
- E11.065 ....In I/O devices or adapters therefor (EPO)
- E11.066 .....Displays (EPO)
- E11.067 ... Timing and synchronization therein (EPO)
- E11.068 ....By using fault tolerant clocks (EPO)
- E11.069 ...Using passive fault-masking of the redundant circuits, e.g., by quadding or by majority decision circuits, etc. (EPO)
- E11.07 ....Synchronization therefor (EPO)
- E11.071 ... Using active fault-masking, e.g., by switching out faulty elements or by switching in spare elements, etc. (EPO)
- E11.072 ....In systems, e.g., multiprocessors, etc. (EPO)
- E11.073 ....In distributed systems (EPO)
- E11.074 .....In regular structures (EPO)
- E11.075 .....Array of processors, e.g., systolic arrays, etc. (EPO)
- E11.076 ..... Hypercubes (EPO)
- E11.077 .....Trees (EPO)
- E11.078 ....In interconnections, e.g., rings, etc. (EPO)
- E11.079 .....Bus (EPO) E11.08 ....Data exchange between units, e.g., for updating backup units, etc. (EPO)
- E11.081 ....For control, e.g., actuators, etc. (EPO)
- E11.082 .... In arithmetic units (EPO)
- E11.083 ....Redundant power supplies (EPO)
- E11.084 ....Masking faults in storage systems using spares and/or by reconfiguring (EPO)
- E11.085 .....Removing defective units from operation (EPO)
- E11.086 .....Bypassing defective units on a serial bus (EPO)
- E11.087 .....With address translations and modifications (EPO) E11.088 ..... Handling defects in a Redundant Array of Inexpensive Disks (RAID) by remapping (EPO) E11.089 .....Managing spare storage units (EPO) E11.09 .....Hot spares (EPO) E11.091 .....Via redundancy in hardware accessing the storage components (EPO) E11.092 .....Using redundant I/O processors, storage control units or array controllers (EPO) E11.093 .....With serial buses (EPO) E11.094 .....To file servers (EPO) E11.095 .....Connection redundancy between storage system components (EPO) E11.096 .....With serial buses (EPO) E11.097 .....To file servers (EPO) E11.098 .....Using the replication of data, e.g., with two or more copies, etc. (EPO) E11.099 .....Duplex memories, e.g., twin boot ROMs, etc. (EPO) E11.1 .....Duplexed caches, e.g., cashe paired with non-volatile storage, etc. (EPO) E11.101 ..... Mirroring, i.e., the concept of maintaining data on two or more units in the same state at all times (EPO) E11.102 .....Resynchronization of failed mirrors (EPO) E11.103 ..... Mirror management, e.g., pairing of units, etc. (EPO) E11.104 .....Mirroring on the same storage unit (EPO) E11.105 .....Mirroring on different storage units with a common controller (RAID 1) (EPO) E11.106 .....Mirroring with multiple controllers (EPO) E11.107 .....Asynchronous mirroring (EPO) E11.108 .....Synchronous mirroring (EPO) E11.109 .....De-clustering of replicated data (EPO) E11.11 .....Using more than two copies (EPO)

# CLASS 714 ERROR DETECTION/CORRECTION AND FAULT DETECTION/RECOV- 714 - 7 ERY

E11.111	In Logic Arrays, e.g., programmable or iterative
E11.112	of the data by redundancy in
E11.113	operation (EPO) Saving, restoring, recovering or retrying (EPO)
E11.114	(EPO) (EPO) (EPO)
E11.115	Checkpointing the instruction stream (EPO)
E11.116	For bus or memory accesses (EPO)
E11.117 E11.118	<pre>Of application data (EPO)Backing up, restoring or mirroring files or drives (EPO)</pre>
E11.119	Backing up, i.e., point-in- time backup (EPO)
E11.12	Hardware arrangements for backup (EPO)
E11.121	Backup Management techniques (EPO)
F11 122	Recovery techniques (FPO)
E11.123	(EPO)
E11 124	Scheduling policy (EPO)
E11.125	For networked
	environments (EPO)
E11.126	(EPO)
E11.127	Mirroring (EPO)
E11.128	Distributed database
<b>E</b> 11 100	systems; Replica control (EPO)
611.129	mobile agents and networked agents (EPO)
E11.13	Using logs or checkpoints (EPO)
E11.131	In transactions (EPO)
E11.132	<pre>At operating system level  (EPO)</pre>
E11.133	Boot up procedures (EPO)
E11.134	<pre>Reconfiguring to eliminate the error (EPO)</pre>
E11.135	<pre>During software upgrading (EPO)</pre>
E11.136	<pre>At file system or disk access level (EPO)</pre>
E11.137	<pre>Restarting or rejuvenating (EPO)</pre>
E11.138	<pre>Resetting or repowering (EPO)</pre>
E11.139	Cleaning up resources (EPO)

E11.14	Suspending and resuming a running system (EPO)
E11.141	errors (EPO)
E11.142	Error detection (EPO)
E11 143	By time redundancy (EPO)
E11 111	Error queidence e g error
LII.I44	spreading countermeasures, fault avoidance, etc. (EPO)
E11.145	.Detection or location of
	defective computer hardware by
	testing during standby
	operation or during idle time,
	e.g., start-up testing, etc. (EPO)
E11.146	Verification or detection of
	system hardware configuration (EPO)
E11.147	Logging of test results (EPO)
E11.148	Test methods (EPO)
E11.149	Power-On Test, e.g., POST,
	etc. (EPO)
E11 15	Configuration test (EPO)
F11 151	Background testing (EPO)
F11 152	Poriodia tosting (EPO)
E11 152	most trigger logic (EDO)
EII.IJJ	Magningl shashing (EPO)
EII.134	Marginal checking (EPO)
ELL.155	. Testing of logic operation,
	······································
	e.g., by logic analyzers, etc. (EPO)
E11.156	e.g., by logic analyzers, etc. (EPO) Using Fault Dictionaries (EPO)
E11.156 E11.157	<pre>e.g., by logic analyzers, etc. (EPO) Using Fault Dictionaries (EPO) Using Expert Systems (EPO)</pre>
E11.156 E11.157 E11.158	<pre>e.g., by logic analyzers, etc. (EPO) Using Fault Dictionaries (EPO) Using Expert Systems (EPO) Using Neural Networks (EPO)</pre>
E11.156 E11.157 E11.158 E11.159	<ul> <li>e.g., by logic analyzers, etc. (EPO)</li> <li>Using Fault Dictionaries (EPO)</li> <li>Using Expert Systems (EPO)</li> <li>Using Neural Networks (EPO)</li> <li>Functional testing (EPO)</li> </ul>
E11.156 E11.157 E11.158 E11.159 E11.16	<ul> <li>e.g., by logic analyzers, etc. (EPO)</li> <li>Using Fault Dictionaries (EPO)</li> <li>Using Expert Systems (EPO)</li> <li>Using Neural Networks (EPO)</li> <li>Functional testing (EPO)</li> <li>Reconfiguring circuits for testing, e.g., LSSD,</li> </ul>
E11.156 E11.157 E11.158 E11.159 E11.16	<ul> <li>e.g., by logic analyzers, etc. (EPO)</li> <li>Using Fault Dictionaries (EPO)</li> <li>Using Expert Systems (EPO)</li> <li>Using Neural Networks (EPO)</li> <li>Functional testing (EPO)</li> <li>Reconfiguring circuits for testing, e.g., LSSD, partitioning, etc. (EPO)</li> </ul>
E11.156 E11.157 E11.158 E11.159 E11.16 E11.161	<ul> <li>e.g., by logic analyzers, etc. (EPO)</li> <li>Using Fault Dictionaries (EPO)</li> <li>Using Expert Systems (EPO)</li> <li>Using Neural Networks (EPO)</li> <li>Functional testing (EPO)</li> <li>Reconfiguring circuits for testing, e.g., LSSD, partitioning, etc. (EPO)</li> <li>Test of buses, lines or</li> </ul>
E11.156 E11.157 E11.158 E11.159 E11.16 E11.161	<ul> <li>e.g., by logic analyzers, etc. (EPO)</li> <li>Using Fault Dictionaries (EPO)</li> <li>Using Expert Systems (EPO)</li> <li>Using Neural Networks (EPO)</li> <li>Functional testing (EPO)</li> <li>Reconfiguring circuits for testing, e.g., LSSD, partitioning, etc. (EPO)</li> <li>Test of buses, lines or interfaces, e.g., stuck-at or</li> </ul>
E11.156 E11.157 E11.158 E11.159 E11.16 E11.161	<ul> <li>e.g., by logic analyzers, etc. (EPO)</li> <li>Using Fault Dictionaries (EPO)</li> <li>Using Expert Systems (EPO)</li> <li>Using Neural Networks (EPO)</li> <li>Functional testing (EPO)</li> <li>Reconfiguring circuits for testing, e.g., LSSD, partitioning, etc. (EPO)</li> <li>Test of buses, lines or interfaces, e.g., stuck-at or open line faults, etc. (EPO)</li> </ul>
E11.156 E11.157 E11.158 E11.159 E11.16 E11.161 E11.162	<ul> <li>e.g., by logic analyzers, etc. (EPO)</li> <li>Using Fault Dictionaries (EPO)</li> <li>Using Expert Systems (EPO)</li> <li>Using Neural Networks (EPO)</li> <li>Functional testing (EPO)</li> <li>Reconfiguring circuits for testing, e.g., LSSD, partitioning, etc. (EPO)</li> <li>Test of buses, lines or interfaces, e.g., stuck-at or open line faults, etc. (EPO)</li> <li>Test or error correction or</li> </ul>
E11.156 E11.157 E11.158 E11.159 E11.16 E11.161 E11.162	<ul> <li>e.g., by logic analyzers, etc. (EPO)</li> <li>Using Fault Dictionaries (EPO)</li> <li>Using Expert Systems (EPO)</li> <li>Using Neural Networks (EPO)</li> <li>Functional testing (EPO)</li> <li>Reconfiguring circuits for testing, e.g., LSSD, partitioning, etc. (EPO)</li> <li>Test of buses, lines or interfaces, e.g., stuck-at or open line faults, etc. (EPO)</li> <li>Test or error correction or detection circuits (EPO)</li> </ul>
E11.156 E11.157 E11.158 E11.159 E11.16 E11.161 E11.162 E11.163	<ul> <li>e.g., by logic analyzers, etc. (EPO)</li> <li>Using Fault Dictionaries (EPO)</li> <li>Using Expert Systems (EPO)</li> <li>Using Neural Networks (EPO)</li> <li>Functional testing (EPO)</li> <li>Reconfiguring circuits for testing, e.g., LSSD, partitioning, etc. (EPO)</li> <li>Test of buses, lines or interfaces, e.g., stuck-at or open line faults, etc. (EPO)</li> <li>Test or error correction or detection circuits (EPO)</li> <li>Test of input/output devices</li> </ul>
E11.156 E11.157 E11.158 E11.159 E11.16 E11.161 E11.162 E11.163	<ul> <li>e.g., by logic analyzers, etc. (EPO)</li> <li>Using Fault Dictionaries (EPO)</li> <li>Using Expert Systems (EPO)</li> <li>Using Neural Networks (EPO)</li> <li>Functional testing (EPO)</li> <li>Reconfiguring circuits for testing, e.g., LSSD, partitioning, etc. (EPO)</li> <li>Test of buses, lines or interfaces, e.g., stuck-at or open line faults, etc. (EPO)</li> <li>Test or error correction or detection circuits (EPO)</li> <li>Test of input/output devices or peripheral units (EPO)</li> </ul>
E11.156 E11.157 E11.158 E11.159 E11.16 E11.161 E11.162 E11.163 E11.164	<ul> <li>e.g., by logic analyzers, etc. (EPO)</li> <li>Using Fault Dictionaries (EPO)</li> <li>Using Expert Systems (EPO)</li> <li>Using Neural Networks (EPO)</li> <li>Functional testing (EPO)</li> <li>Reconfiguring circuits for testing, e.g., LSSD, partitioning, etc. (EPO)</li> <li>Test of buses, lines or interfaces, e.g., stuck-at or open line faults, etc. (EPO)</li> <li>Test or error correction or detection circuits (EPO)</li> <li>Test of input/output devices or peripheral units (EPO)</li> <li>Test of ALU (EPO)</li> </ul>
E11.156 E11.157 E11.158 E11.159 E11.16 E11.161 E11.162 E11.163 E11.164 E11.164	<ul> <li>e.g., by logic analyzers, etc. (EPO)</li> <li>Using Fault Dictionaries (EPO)</li> <li>Using Expert Systems (EPO)</li> <li>Using Neural Networks (EPO)</li> <li>Functional testing (EPO)</li> <li>Functional testing (EPO)</li> <li>Reconfiguring circuits for testing, e.g., LSSD, partitioning, etc. (EPO)</li> <li>Test of buses, lines or interfaces, e.g., stuck-at or open line faults, etc. (EPO)</li> <li>Test or error correction or detection circuits (EPO)</li> <li>Test of input/output devices or peripheral units (EPO)</li> <li>Test of ALU (EPO)</li> <li>Test of interrupt circuits</li> </ul>
E11.156 E11.157 E11.158 E11.159 E11.16 E11.161 E11.162 E11.163 E11.164 E11.164	<ul> <li>e.g., by logic analyzers, etc. (EPO)</li> <li>Using Fault Dictionaries (EPO)</li> <li>Using Expert Systems (EPO)</li> <li>Using Neural Networks (EPO)</li> <li>Functional testing (EPO)</li> <li>Reconfiguring circuits for testing, e.g., LSSD, partitioning, etc. (EPO)</li> <li>Test of buses, lines or interfaces, e.g., stuck-at or open line faults, etc. (EPO)</li> <li>Test or error correction or detection circuits (EPO)</li> <li>Test of input/output devices or peripheral units (EPO)</li> <li>Test of ALU (EPO)</li> <li>Test of interrupt circuits (EPO)</li> </ul>
E11.156 E11.157 E11.158 E11.159 E11.16 E11.161 E11.162 E11.163 E11.164 E11.165 E11.166	<ul> <li>e.g., by logic analyzers, etc. (EPO)</li> <li>Using Fault Dictionaries (EPO)</li> <li>Using Expert Systems (EPO)</li> <li>Using Neural Networks (EPO)</li> <li>Functional testing (EPO)</li> <li>Reconfiguring circuits for testing, e.g., LSSD, partitioning, etc. (EPO)</li> <li>Test of buses, lines or interfaces, e.g., stuck-at or open line faults, etc. (EPO)</li> <li>Test or error correction or detection circuits (EPO)</li> <li>Test of input/output devices or peripheral units (EPO)</li> <li>Test of ALU (EPO)</li> <li>Test of interrupt circuits (EPO)</li> <li>Test of CPU or processors</li> </ul>
E11.156 E11.157 E11.158 E11.159 E11.16 E11.161 E11.162 E11.163 E11.164 E11.165 E11.166	<ul> <li>e.g., by logic analyzers, etc. (EPO)</li> <li>Using Fault Dictionaries (EPO)</li> <li>Using Expert Systems (EPO)</li> <li>Using Neural Networks (EPO)</li> <li>Functional testing (EPO)</li> <li>Reconfiguring circuits for testing, e.g., LSSD, partitioning, etc. (EPO)</li> <li>Test of buses, lines or interfaces, e.g., stuck-at or open line faults, etc. (EPO)</li> <li>Test or error correction or detection circuits (EPO)</li> <li>Test of input/output devices or peripheral units (EPO)</li> <li>Test of ALU (EPO)</li> <li>Test of interrupt circuits (EPO)</li> <li>Test of CPU or processors (EPO)</li> </ul>
E11.156 E11.157 E11.158 E11.159 E11.16 E11.161 E11.162 E11.163 E11.164 E11.165 E11.166 E11.166	<ul> <li>e.g., by logic analyzers, etc. (EPO)</li> <li>Using Fault Dictionaries (EPO)</li> <li>Using Expert Systems (EPO)</li> <li>Using Neural Networks (EPO)</li> <li>Functional testing (EPO)</li> <li>Reconfiguring circuits for testing, e.g., LSSD, partitioning, etc. (EPO)</li> <li>Test of buses, lines or interfaces, e.g., stuck-at or open line faults, etc. (EPO)</li> <li>Test or error correction or detection circuits (EPO)</li> <li>Test of input/output devices or peripheral units (EPO)</li> <li>Test of ALU (EPO)</li> <li>Test of CPU or processors (EPO)</li> <li>Test simulating additional</li> </ul>
E11.156 E11.157 E11.158 E11.159 E11.16 E11.161 E11.162 E11.163 E11.164 E11.165 E11.166 E11.166	<ul> <li>e.g., by logic analyzers, etc. (EPO)</li> <li>Using Fault Dictionaries (EPO)</li> <li>Using Expert Systems (EPO)</li> <li>Using Neural Networks (EPO)</li> <li>Functional testing (EPO)</li> <li>Reconfiguring circuits for testing, e.g., LSSD, partitioning, etc. (EPO)</li> <li>Test of buses, lines or interfaces, e.g., stuck-at or open line faults, etc. (EPO)</li> <li>Test or error correction or detection circuits (EPO)</li> <li>Test of input/output devices or peripheral units (EPO)</li> <li>Test of ALU (EPO)</li> <li>Test of cPU or processors (EPO)</li> <li>Test of CPU or processors</li> <li>(EPO)</li> <li>By simulating additional hardware e g fault</li> </ul>
E11.156 E11.157 E11.158 E11.159 E11.16 E11.161 E11.162 E11.163 E11.164 E11.165 E11.166 E11.166	<ul> <li>e.g., by logic analyzers, etc. (EPO)</li> <li>Using Fault Dictionaries (EPO)</li> <li>Using Expert Systems (EPO)</li> <li>Using Neural Networks (EPO)</li> <li>Using Neural Networks (EPO)</li> <li>Functional testing (EPO)</li> <li>Reconfiguring circuits for testing, e.g., LSSD, partitioning, etc. (EPO)</li> <li>Test of buses, lines or interfaces, e.g., stuck-at or open line faults, etc. (EPO)</li> <li>Test or error correction or detection circuits (EPO)</li> <li>Test of input/output devices or peripheral units (EPO)</li> <li>Test of ALU (EPO)</li> <li>Test of CPU or processors (EPO)</li> <li>By simulating additional hardware, e.g., fault simulation (EPO)</li> </ul>
E11.156 E11.157 E11.158 E11.159 E11.16 E11.161 E11.162 E11.163 E11.164 E11.165 E11.166 E11.166 E11.167	<ul> <li>e.g., by logic analyzers, etc. (EPO)</li> <li>Using Fault Dictionaries (EPO)</li> <li>Using Expert Systems (EPO)</li> <li>Using Neural Networks (EPO)</li> <li>Functional testing (EPO)</li> <li>Reconfiguring circuits for testing, e.g., LSSD, partitioning, etc. (EPO)</li> <li>Test of buses, lines or interfaces, e.g., stuck-at or open line faults, etc. (EPO)</li> <li>Test or error correction or detection circuits (EPO)</li> <li>Test of input/output devices or peripheral units (EPO)</li> <li>Test of ALU (EPO)</li> <li>Test of CPU or processors (EPO)</li> <li>By simulating additional hardware, e.g., fault simulation, (EPO)</li> <li>Emulators (EPO)</li> </ul>
E11.156 E11.157 E11.158 E11.159 E11.16 E11.161 E11.162 E11.163 E11.164 E11.165 E11.166 E11.166 E11.167 E11.168	<ul> <li>e.g., by logic analyzers, etc. (EPO)</li> <li>Using Fault Dictionaries (EPO)</li> <li>Using Expert Systems (EPO)</li> <li>Using Neural Networks (EPO)</li> <li>Functional testing (EPO)</li> <li>Reconfiguring circuits for testing, e.g., LSSD, partitioning, etc. (EPO)</li> <li>Test of buses, lines or interfaces, e.g., stuck-at or open line faults, etc. (EPO)</li> <li>Test or error correction or detection circuits (EPO)</li> <li>Test of input/output devices or peripheral units (EPO)</li> <li>Test of ALU (EPO)</li> <li>Test of CPU or processors (EPO)</li> <li>Test of CPU or processors (EPO)</li> <li>By simulating additional hardware, e.g., fault simulation, (EPO)</li> <li>Emulators (EPO)</li> </ul>

### 714 - 8 CLASS 714 ERROR DETECTION/CORRECTION AND FAULT DETECTION/RECOV-ERY

- E11.17 ...Tester hardware, i.e., output processing circuits, etc. (EPO) E11.171 ....Test interface between tester
- and unit under test (EPO)
- E11.172 ....Using a storage for the test inputs, e.g., test-ROM, script files, etc. (EPO)
- E11.173 ....Remote test (EPO)
- E11.174 ....Using a dedicated service processor for test (EPO)
- E11.175 ....With comparison between actual response and known fault-free response, e.g., signature analyzer, etc. (EPO)
- E11.176 ....In Multi-processor systems, e.g., one processor becoming the test master, etc. (EPO)
- E11.177 ...Generation of test inputs, e.g., test vectors, patterns or sequences, etc. (EPO)
- E11.178 .By checking the correct order of processing (EPO)
- E11.179 .Monitoring (EPO)
- E11.18 ..With visual or acoustical indication of the functioning of the machine (EPO)
- E11.181 ...Visualization of programs or trace data (EPO)
- E11.182 ...Display for diagnostics, e.g., diagnostic result display, self-test user interface, etc. (EPO)
- E11.183 ....Display of waveforms, e.g., of logic analyzers, etc. (EPO)
- E11.184 ...Display of status information (EPO)
- E11.185 ....By lamps or LED's (EPO)
- E11.186 .....For error or online/offline status (EPO)
- E11.187 ....Alarm or error message display (EPO)
- E11.188 ....Computer systems status display (EPO)
- E11.189 ..Recording or statistical evaluation of computer activity, e.g., of down time, of input/output operation, etc. (EPO)
- E11.19 ...Of interconnections, e.g., interconnecting networks, etc. (EPO)
- E11.191 ... Of parallel or distributed programming (EPO)
- E11.192 ... Performance measurement (EPO)

E11.193	Workload generation, e.g.,
F11 19/	Bonchmarking (EPO)
D11.10F	
ETT.192	Time measurement, e.g.,
	response time, etc. (EPO)
E11.196	Of active or idle time (EPO)
E11.197	Performance evaluation by
	modeling or statistical
	analysis (EPO)
E11.198	Performance evaluation by
	simulation (EPO)
E11.199	Trace driven simulation (EPO)
E11.2	Performance evaluation by
	tracing or monitoring (EPO)
E11 201	For interfaces buses (EPO)
E11 202	Ear gygtomg (EDO)
E11.202	Address transient (EDO)
EII.203	Address tracing (EPO)
E11.204	Data logging (EPO)
EII.205	Circuit details, i.e., tracer
-11 000	hardware (EPO)
EII.206	For I/O devices (EPO)
E11.207	.Preventing errors by testing or
	debugging software (EPO)
E11.208	Software debugging (EPO)
E11.209	Compilers or other tools
	operating on the source text
	(EPO)
E11.21	Debuggers (EPO)
E11.211	Error checking code in the
	program under test (EPO)
E11.212	Tracing methods or tools (EPO)
E11.213	By using additional hardware
	(EPO)
E11.214	By making modifications to
	the CPU (EPO)
F11 215	By monitoring the bug (FPO)
E11 216	By omulating the CDU (EDO)
EII.210	By emulating the CPO (EPO)
ETT'	User interfaces for testing or
-11 010	debugging software (EPO)
EI1.218	Methods or tools for writing
	reliable software and for
	evaluating software (EPO)
E11.219	Methods or tools to render
	software testable (EPO)
E11.22	Software metrics (EPO)

#### FOREIGN ART COLLECTIONS

FOR 000 CLASS-RELATED FOREIGN DOCUMENTS

## CLASS 714 ERROR DETECTION/CORRECTION AND FAULT DETECTION/RECOV- 714 - 9 ERY

Any foreign patents or non-patent literature from subclasses that have been reclassified have been transferred directly to FOR Collections listed below. These Collections contain ONLY foreign patents or non-patent literature. The parenthetical references in the Collection titles refer to the abolished subclasses from which these Collections were derived.

#### DIGITAL LOGIC TESTING (371/22.1)

- FOR 100 .Scan path testing (LSSD) (371/ 22.3)
- FOR 101 .Including test pattern generator (371/27)

### DIGITAL DATA ERROR CORRECTION (371/30)

- FOR 102 .Block code (371/37.1)
- FOR 103 .. Memory access (371/40.1)
- FOR 104 .Convolutional code (371/43)
- FOR 288 ERROR/FAULT ANTICIPATION (371/4) .Replacement with spare device or system (371/8.1)
- FOR 289 ..Transmission facility or channel (371.8.2)
- FOR 290 .. Memory (371/10.1)
- FOR 291 .. Transmission facility (371/ 11.2)
- FOR 292 ..Data processor or computer (371/11.3)

### DIAGNOSTIC TESTING (371/15.1)

- FOR 293 .Programmable processor testing (371/16.1)
- FOR 294 .. Emulator device (371/16.2)
- FOR 295 ..Watchdog timer (e.g., time-out) (371/16.3)
- FOR 296 .. Processor within diverse (microwave, photocopier) (371/ 16.4)
- FOR 297 .. Error or fault, logging or tracking (371/16.5)
- FOR 298 ..Dedicated maintenance subsystem (371/18)
- FOR 299 .Testing of external device by programmable digital computer (371/20)

FOR 300 ERROR DETECTION FOR SYNCHRONIZATION CONTROL (371/ 47.1) DATA PROCESSING SYSTEM ERROR OR

FAULT HANDLING (714/100) .Reliability and availability (714/1) .. Fault recovery (714/2)

- ...By masking or reconfiguration (714/3)
- FOR 306 .... Of network (714/4)
- FOR 307 .... Of memory or peripheral subsystem (714/5)
- FOR 308 ....Redundant stored data accessed (e.g., duplicated data, error correction coded data, or other parity-type data) (714/6)
- FOR 309 .....Reconfiguration (e.g., adding a replacement storage component (714/7)
- FOR 310 .....Isolating failed storage location (e.g., sector remapping) (714/8)
- FOR 311 ....Access processor affected (e.g., I/O processor, MMU, DMA processor (714/9)
  - ..Fault locating (i.e., diagnosis or testing) (714/25)
  - ...Analysis (e.g., of output, state, or design) (714/37)
- FOR 312 .... Of computer software (714/38)
- FOR 313 .. Performance monitoring for fault avoidance (714/47)