CLASS 714, ERROR DETECTION/CORRECTION AND FAULT DETECTION/RECOVERY

SECTION I - CLASS DEFINITION

This class provides for process or apparatus for detecting and correcting errors in electrical pulse or pulse coded data.

This class also provides for process or apparatus for detecting and recovering from faults in electrical computers and digital data processing systems, as well as logic level based systems.

SECTION II - REFERENCES TO OTHER CLASSES

SEE OR SEARCH CLASS:

324, Electricity: Measuring and Testing, appropriate subclasses for process and apparatus for measuring, testing or sensing of electric properties or measuring, testing or sensing of non-electric properties by electric means.

341, Coded data Generation or Conversion, appropriate subclasses for process and apparatus utilizing electrical pulse coding techniques without error correcting/detecting functions for the generating or conversion of coded data.

358, Facsimile and Static Presentation Processing, appropriate subclasses for process and apparatus for testing and performance monitoring of facsimile devices.

365, Static Information Storage and Retrieval, subclass 200 and 201, for process and apparatus including the specifics of memory devices which are tested for defects or erroneous information.

370, Multiplex Communications, appropriate subclasses for process and apparatus for measuring and testing part of a multiplex system.

375, Pulse or Digital Communications, subclasses 213 and 224 - 228 for process and apparatus for testing pulse or digital communication systems.

379, Telephonic Communications, subclasses 1.01 through 33 for process and apparatus for testing of telephone circuits.

455, Telecommunications, appropriate subclasses for process and apparatus for measuring, testing and monitoring of telecommunication systems.

706, Data Processing: Artificial Intelligence, subclasses 1+ for fuzzy logic, subclasses 15+ for neural networks and subclasses 45+ for knowledge processing systems.

707, Data Processing: Database, Data Mining, and File Management or Data Structures, 609 through 686 for database maintenance including synchronizing, archiving, backing up and recovering databases, subclasses 758 through 780 for record, file and data search and comparison, and subclasses 687 through 704 for data integrity in databases.

708, Electrical Computers: Arithmetic Processing and Calculating, appropriate subclasses for process and apparatus for computer arithmetic circuits.

709, Electrical Computers and Digital Processing Systems: Multicomputer Data Transferring or Plural Processor Synchronization, appropriate subclasses for multiple computer or computer process systems.

710, Electrical Computers and Digital Data Processing Systems: Input/Output, appropriate subclasses for process and apparatus for computer input or output systems.

711, Electrical Computers and Digital Processing Systems: Memory, subclasses 133+ for entry replacement strategies and page fault recovery, and subclasses 161+ for data archiving.

712, Electrical Computers and Digital Processing Systems: Processing Architectures and Instruction Processing(e.g., processors), appropriate subclasses for process and apparatus for computer structure and program execution systems.

713, Electrical Computers and Digital Processing Systems: Support, appropriate subclasses for process and apparatus for computer cases, housing and supports.

726, Information Security, subclasses 1 through 36 for information security in computers or digital processing system.

SECTION III - GLOSSARY

BUS

A conductor used for transferring data, signals or power.

COMPUTER

A machine that inputs data, processes data, stores data, and outputs data.

DATA

Representation of information in a coded manner suitable for communication, interpretation, or processing.

ADDRESS DATA

Data that represent or identify a source or destination.

INSTRUCTION DATA

Data that represent an operation and identify its operands, if any.

STATUS DATA

Data that represent conditions of data, digital data processing systems, computers, peripherals, memory, etc.

USER DATA

Data other than address data, instruction data, or status data.

DATA PROCESSING

See PROCESSING, below.

DIGITAL DATA PROCESSING SYSTEM

An arrangement of processor(s) in combination with either memory or peripherals, or both, performing data processing.

ERROR

Manifestation of a fault as an undesired event that occurs when actual behavior deviates from the behavior that is required by initial specification. This includes a change in information content of pulse or pulse coded data to a state or value other than the normal state or value of a properly operating device or system.

FAULT

A flaw in a functional unit (hardware or software).

INFORMATION

Meaning that a human being assigns to data by means of the conventions applied to that data.

MEMORY

A functional unit to which data can be stored and from which data can be retrieved.

PERIPHERAL

A functional unit that transmits data to or receives data from a computer to which it is coupled.

PROCESSING

Methods or apparatus performing systematic operations upon data or information exemplified by functions such as data or information transferring, merging, sorting, and computing (i.e., arithmetic operations or logical operations).

(1) Note. In this class, the glossary term data is used to modify processing in the term data processing; whereas the term digital data processing system refers to a machine performing data processing.

PROCESSOR

A functional unit that interprets and executes instruction data.

RECOVERY

Responding to a fault in a system by either returning a system to a previous level of correct operation, achieving a degraded level of correct operation, or safely shutting down the system.

SECURITY

Extent of protection for system hardware, software, or data from maliciously caused destruction, unauthorized modification, or unauthorized disclosure.

SUBCLASSES

1 Reliability and availability:
This subclass is indented under subclass 100.
Subject matter further including means or steps for increasing a probability of correctly performing services (e.g., data processing) throughout a time interval, given correct performance at the beginning of the interval, or for increasing the probability of correctly performing services at any given instant.

(1) Note. Reliability features in a data processing control system are classified elsewhere.

SEE OR SEARCH THIS CLASS, SUBCLASS:

746+, for data error detection and correction, and fault detection and recovery.

SEE OR SEARCH CLASS:

380, Cryptography, subclass 4 for stored digital data access or copy prevention in combination with data encryption; e.g., software program protection or computer virus detection in combination with data encryption.

700, Data Processing: Generic Control Systems or Specific Applications, subclasses 79 through 82 for reliability features in a data processing generic control system.

2 Fault recovery:

This subclass is indented under subclass 1. Subject matter further including means or steps for responding to a failure by either returning a system to a previous level of correct operation, achieving a degraded level of correct operation, or safely shutting down the system after detecting the error or locating the fault.

(1) Note. Classification here requires significant data processing features claimed. For fault recovery in a system without significant data processing method or apparatus, classification is elsewhere. See the SEE OR SEARCH THIS CLASS, SUBCLASS and SEE OR SEARCH CLASS notes below.

(2) Note. Classification here requires notification or detection of the fault, its location, and a further action. Subcombinations used in the process of fault recovery; e.g., fault locating, are classified below.

(3) Note. “Page faults” are a species of faults peculiar to memory accessing and are classified elsewhere in this class. See the SEE OR SEARCH THIS CLASS, SUBCLASS notes below.

SEE OR SEARCH THIS CLASS, SUBCLASS:

746+, for data error detection and correction of general utility.

SEE OR SEARCH CLASS:

711, Electrical Computers and Digital Processing Systems: Memory, subclasses 133+ for entry replacement strategies and page fault recovery.

3 By masking or reconfiguration:

This subclass is indented under subclass 2. Subject matter further including means or steps for recovery by selecting a correct output from a concurrently active redundant functional unit in place of the output of the failed functional unit, or by replacing or isolating the failed functional unit.

(1) Note. This subclass is for fault recovery by masking or reconfiguration in combination with significant data processing. Generic fault recovery is classified elsewhere. See the SEE OR SEARCH CLASS notes below.

SEE OR SEARCH THIS CLASS, SUBCLASS:

825, for fault recovery by replacing or isolating the failed functional unit not provided for elsewhere.

4.1 Of network:

This subclass is indented under subclass 3. Subject matter further including means or steps for recovery from nodal failure at a network level.

(1) Note. This subclass is for the recovery and integration of the processing within the node itself, as opposed to the data flow/routing of the network via a communication channel. This subclass definition specifically states that it handles the failure of the processing aspects of the node, and not the impact on the network itself.

(2) Note. Subject matter that involves hardware devices such as switches to re-route communications in the multiplex environment are classified elsewhere.

SEE OR SEARCH CLASS:

340, Communications: Electrical, subclass 2.23 for alternate routing in a plural stage communication system, and subclasses 286.01-333 for residual electrical communication systems.

342, Communications: Directive Radio Wave Systems and Devices (e.g., Radar, Radio Navigation), subclasses 1 through 465 for alternate routing in a plural stage radar network.

343, Communications: Radio Wave Antennas, subclasses 700 through 916 for alternate routing in a plural antenna system.

370, Multiplex Communications, subclasses 216 through 228 for fault recovery, and subclasses 229-240 for data flow congestion prevention and control in a multiplex communication system, i.e., the hardware devices (switches, etc.) to re-route communications in the multiplex environment.

375, Pulse or Digital Communications, subclass 356 for network synchronizing more than two stations.

4.11 Backup or standby (e.g., failover, etc.):
This subclass is indented under subclass 4.1. Subject matter wherein the network has a spare substitute node ready to take over in the event the main one crashes.

SEE OR SEARCH THIS CLASS, SUBCLASS:

13, for prepared backup processor or updating backup processor.

SEE OR SEARCH CLASS:

370, Multiplex Communications, subclasses 216 through 228 for fault recovery, and subclasses 229-240 for data flow congestion prevention and control in a multiplex communication system.

379, Telephonic Communications, subclass 112.02 for call traffic recording by redundant processor or backup processor, and subclass 221.04 for restoring failed network routing.

700, Data Processing: Generic Control Systems or Specific Applications, subclass 82 for relating to the protection and reliability of the control system.

707, Data Processing: Database and File Management or Data Structures, subclasses 640 through 686 for archiving, backup, or recovery under database management.

711, Electrical Computers and Digital Processing Systems: Memory, subclasses 161 through 162 for archiving and backup under memory accessing, and subclass 165 for internally relocating data.

713, Electrical Computers and Digital Processing Systems: Support, subclass 323 for relating to sleep/resume, suspend/resume or standby of data processing systems.

4.12 Hot swapping (i.e., while network is up):
This subclass is indented under subclass 4.11. Subject matter wherein the failed node is replaced without significant interruption to the network.

4.2 Isolate or remove failed node with replacement (e.g., bypassing, re-routing, etc.):
This subclass is indented under subclass 4.1. Subject matter further comprising means or steps to separate, detach, bypass, or re-route a failed node.

4.21 Reintegrate node back into network:
This subclass is indented under subclass 4.2. Subject matter further comprising means or steps for putting back or establishing a failed node back into network without replacement of the failed node.

4.3 Repair failed node without replacement (i.e., on-line repair):
This subclass is indented under subclass 4.1. Subject matter further comprising means or steps to fix the failed node through dial-up, or dedicated communications links, or through the Internet without replacing the node.

4.4 Remote repair:
This subclass is indented under subclass 4.1. Subject matter further comprising means or

steps to repair nodes located at a site remote from the network.

SEE OR SEARCH THIS CLASS, SUBCLASS:

6.31, for repair at the plurality of memory devices.

4.5 Bus network (e.g., PCI, AGP, etc.):

This subclass is indented under subclass 4.1. Subject matter wherein the network shares a common path such as Peripheral Component Interconnect (PCI) or Accelerated Graphics Port (AGP) for enabling redundancy in the communication between a plurality of peripheral devices and a host.

SEE OR SEARCH CLASS:

370, Multiplex Communications, subclass 258 for a bus network having a closed transmission path.

5.1 Of peripheral subsystem:

This subclass is indented under subclass 3. Subject matter further including means or steps for recovery from a faulted peripheral device.

SEE OR SEARCH THIS CLASS, SUBCLASS:

710, through 711, for replacement of memory spare location, portion, or segment.

SEE OR SEARCH CLASS:

710, Electrical Computers and Digital Data Processing Systems: Input/Output, subclasses 1 through 74 for transferring data from one or more peripherals to one or more computers for the latter to process, store, or further transfer or for transferring data from the computers to the peripherals.

711, Electrical Computers and Digital Processing Systems: Memory, subclasses 100 through 317 for means (e.g., processor, controller, etc.) or steps for governing memory in a digital data processing system or the passage (e.g., reading or writing, etc.) of data thereto, and subclasses 133-136 for entry replacement strategies and page fault recovery.

5.11 Access processor affected (e.g., I/O processor, MMU, or DMA processor, etc.):

This subclass is indented under subclass 5.1. Subject matter further comprising means or steps for recovery from a fault limited to a specialized processor accessing I/O processor, Memory Management Unit (MMU), or Direct Memory Access (DMA) processor.

SEE OR SEARCH CLASS:

712, Electrical Computers and Digital Processing Systems: Processing Architectures and Instruction Processing (e.g., Processors), appropriate subclasses for digital data processing system architecture, per se.

6.1 Of memory:

This subclass is indented under subclass 3. Subject matter further including means or steps for recovery from a fault of a memory function level.

(1) Note. “Page faults” are a species of faults peculiar to memory accessing which are classified elsewhere. See the SEE OR SEARCH THIS CLASS, SUBCLASS notes below.

SEE OR SEARCH THIS CLASS, SUBCLASS:

710, through 711, for replacement of memory spare location, portion, or segment.

SEE OR SEARCH CLASS:

710, Electrical Computers and Digital Data Processing Systems: Input/Output, subclasses 1 through 74 for transferring data from one or more peripherals to one or more computers for processing or storing.

711, Electrical Computers and Digital Processing Systems: Memory, subclasses 100 through 132 for means (e.g., processor, controller, etc.) or steps for governing memory in a digital data processing system or the passage (e.g., reading or writing, etc.) of data thereto, and subclasses 133-146 for entry replacement strategies and page fault recovery.

6.11 Within single memory device (e.g., disk, etc.):

This subclass is indented under subclass 6.1. Subject matter further including means or steps for recovery of a fault within a single memory device such as a floppy disk, micro-floppy disk, removable cartridge, or hard disk.

6.12 Recovery partition:

This subclass is indented under subclass 6.11. Subject matter further including means or steps for recovery of a fault within a distinct portion of single memory.

6.13 Isolating failed storage location (e.g., sector remapping, etc.):

This subclass is indented under subclass 6.11. Subject matter further including means or steps for recovery by disabling or detaching access to a failed single memory location.

(1) Note. Classification herein requires more than selecting a correct output from a concurrently active redundant functional unit in place of the output of the failed component.

SEE OR SEARCH THIS CLASS, SUBCLASS:

710, through 711, for replacement of memory spare location, portion, or segment.

SEE OR SEARCH CLASS:

365, Static Information Storage and Retrieval, subclasses 200and 201 for bad bit and testing of static storage.

711, Electrical Computers and Digital Processing Systems: Memory, subclasses 170 through 173 for automatically determining memory space allocation.

6.2 Plurality of memory devices (e.g., array, etc.):

This subclass is indented under subclass 6.1. Subject matter further including means or steps for recovery of a fault within a plurality of memory devices, e.g., array, etc.

SEE OR SEARCH CLASS:

326, Electronic Digital Logic Circuitry, subclasses 39 through 45 for programmable gate arrays.

710, Electrical Computers and Digital Data Processing Systems: Input/Output, subclasses 20 through 21 for systems directed to parallel data transfer.

711, Electrical Computers and Digital Processing Systems: Memory, subclasses 170 through 173 for automatically determining memory space allocation.

6.21 Array controller:

This subclass is indented under subclass 6.2. Subject matter wherein a memory array controller performs the recovery of the fault.

6.22 RAID:

This subclass is indented under subclass 6.2. Subject matter wherein the plurality of memory devices are redundant array of inexpensive disks (RAID) for recovery of a fault.

6.23 Mirror (i.e., level 1 RAID):

This subclass is indented under subclass 6.22. Subject matter wherein the RAID has a level one that has one disk drive and an exact backup on a second disk, i.e., all data is redundantly recorded on a second disk for recovery of a fault.

6.24 ECC, parity, or fault code (i.e., level 2+ RAID):

This subclass is indented under subclass 6.22. Subject matter wherein the RAID has a level more than two, which has error checking and correcting code, parity data, or fault code for recovery of a fault.

6.3 Backup or standby (e.g., failover, etc.):

This subclass is indented under subclass 6.2. Subject matter wherein the plurality of memory devices has a spare standby memory ready to take over in the event of the main one crashes.

SEE OR SEARCH THIS CLASS, SUBCLASS:

4.11, for prepared backup or updating backup memory devices.

6.31 Remote repair:
This subclass is indented under subclass 6.3. Subject matter further comprising means or steps to repair a memory located at a site remote from the network.

SEE OR SEARCH THIS CLASS, SUBCLASS:
4.4, for repair of a network remotely.

6.32 Replacement of failed memory device:
This subclass is indented under subclass 6.2. Subject matter further comprising means or steps for replacing a malfunctioning memory device within a plurality of memory devices for recovering a fault.

10 Of processor:
This subclass is indented under subclass 3. Subject matter further including means or steps for recovery from fault of a processor.

SEE OR SEARCH CLASS:
712, Electrical Computers and Digital Processing Systems: Processing Architectures and Instruction Processing (e.g., processors), appropriate subclasses for digital data processing system architecture, per se.

11 Concurrent, redundantly operating processors:
This subclass is indented under subclass 10. Subject matter further including means or steps for recovery employing redundant processors substantially simultaneously performing the same operation.

SEE OR SEARCH CLASS:
700, Data Processing: Generic Control Systems or Specific Applications, subclass 3 for master/slave processors in a data processing generic control system, and subclasses 79-82 for protection or reliability in a digital data processing control system.

12 Synchronization maintenance of processors:
This subclass is indented under subclass 11. Subject matter further including means or steps for maintaining processor state synchronization to achieve redundancy of operation.

(1) Note. Classification here requires a redundant processor for the purpose of reliability, such as by consideration of state of internal registers and the like of the redundant processors and thus the machines themselves. Synchronization in the form of timing and clock skew is classified elsewhere. See the SEE OR SEARCH THIS CLASS, SUBCLASS notes below.

(2) Note. Classification here requires the existence of a fault condition. Synchronization maintenance at the clock level, however, is classified elsewhere. See the search class notes below.

SEE OR SEARCH CLASS:
375, Pulse or Digital Communications, subclasses 354+ for communications synchronizing.
709, Electrical Computers and Digital Processing Systems: Multicomputer Data Transferring or Plural Processor Synchronization, appropriate subclasses for multicomputer and synchronizing, and for synchronization maintenance of plural processors, per se.
712, Electrical Computers and Digital Processing Systems: Processing Architectures and Instruction Processing (e.g., processors), appropriate subclasses for task management, per se.
713, Electrical Computers and Digital Processing Systems: Support, subclasses 400+, for clock synchronization, per se, subclasses 500+, for digital data processing system clock, pulse and timing interval generation, per se.

13 Prepared backup processor (e.g., initializing cold backup) or updating backup processor (e.g., by checkpoint message):
This subclass is indented under subclass 10. Subject matter further including means or steps for readying a backup processor or digital data processing system to replace a failed primary processor or digital data processing system, or to receive recent processing result(s) from a backup processor or digital data processing system that may be relied upon.

(1) Note. Classification here allows for the backup processor or digital data processing system to be performing operations unrelated to backup operation before or after failure of the primary processor or digital data processing systems.

SEE OR SEARCH CLASS:
700, Data Processing: Generic Control Systems or Specific Applications, subclasses 2 through 7 for data processing control system applications employing plural processors, and subclasses 79-82 for protection or reliability in a digital data processing system based control system.

14 Of power supply:
This subclass is indented under subclass 3. Subject matter further including means or steps for recovery using power supply subsystem component redundancy.

SEE OR SEARCH CLASS:
713, Electrical Computers and Digital Processing Systems: Support, subclasses 300+, for power control in a digital data processing system environment, and subclass 321 for electrical digital calculating computer (i.e., calculator) with power saving feature.

15 State recovery (i.e., process or data file):
This subclass is indented under subclass 2. Subject matter further including means or steps for recovery by restoring data in a data file, or data for a process, to data at a previous point in time.

(1) Note. The species of fault recovery or avoidance concerned with storing verbatim copies of data is classified elsewhere. See the SEE OR SEARCH THIS CLASS, SUBCLASS notes below.

(2) Note. Parity and error-correction coded storage of general utility in a system without data processing features claimed is classified elsewhere.

(3) Note. This state recovery subclass provides for reliability and availability recovery under the condition of a fault. Data management, per se, is classified elsewhere. See the search class notes below.

SEE OR SEARCH THIS CLASS, SUBCLASS:
6.1 through 6.23 for recovery by accessing redundant stored data.
763+, for memory access block coding.
805, for storage accessing error/fault detection techniques.

SEE OR SEARCH CLASS:
711, Electrical Computers and Digital Processing Systems: Memory, subclasses 141+ for cache memory coherency, per se; subclasses 147+ for shared memory data processing which may employ data management principles; and subclasses 161+ for preventing the corruption, loss, alteration, or disclosure of data by storing, as in making backup copies.
712, Electrical Computers and Digital Processing Systems: Processing Architectures and Instruction Processing (e.g., processors), appropriate subclasses for source code management and software version management.

16 Forward recovery (e.g., redoing committed action):
This subclass is indented under subclass 15. Subject matter further including means or steps for recovery by re-executing an operation in response to detecting an error in an operation.

(1) Note. Recovery by operation retry or error detection by sequential repetition in a system without data processing features is classified elsewhere.

SEE OR SEARCH THIS CLASS, SUBCLASS:
822, for sequential repetition.

SEE OR SEARCH CLASS:
707, Data Processing: Database, Data Mining, and File Management or Data Structures, subclasses 609 through 686 for database maintenance including synchronizing, archiving, backing up and recovering databases; subclasses 758 through 780 for record,

file and data search and comparison, and subclasses 687 through 704 for data integrity in databases.

17 Reexecuting single instruction or bus cycle:
This subclass is indented under subclass 16. Subject matter further including means or steps for recovery by retrying single instruction or bus cycle.

SEE OR SEARCH CLASS:
710, Electrical Computers and Digital Data Processing Systems: Input/Output, subclasses 100+, for system intraconnecting and bus processing, per se.

18 Transmission data record (e.g., for retransmission):
This subclass is indented under subclass 15. Subject matter further including means or steps for recovery of a communication process (e.g., a session) using a record.

SEE OR SEARCH THIS CLASS, SUBCLASS:
748+, for retransmission in a system without data processing features claimed.

SEE OR SEARCH CLASS:
710, Electrical Computers and Digital Data Processing Systems: Input/Output, appropriate subclasses for I/O processing and communication between computers and peripherals.

19 Undo record:
This subclass is indented under subclass 15. Subject matter further including means or steps for recovery of data in the presence of uncommitted action using a record of the data created before the action.

SEE OR SEARCH CLASS:
707, Data Processing: Database, Data Mining, and File Management or Data Structures, subclasses 609 through 686 for database maintenance including synchronizing, archiving, backing up and recovering databases; subclasses 758 through 780 for record, file and data search and comparison, and subclasses 687 through 704 for data integrity in databases.
715, Data Processing: Presentation Processing of Document, Operator Interface Processing, and Screen Saver Display Processing, appropriate subclasses for a word data processing application on computer, particularly subclasses 255 through 272 for editing in a text data processing application.

20 Plural recovery data sets containing set interrelation data (e.g., time values or log record numbers):
This subclass is indented under subclass 15. Subject matter further including means or steps for recovery using sets of sequenced or linked recovery data containing set sequencing or linking data.

21 State validity check:
This subclass is indented under subclass 15. Subject matter further including means or steps wherein recovery is controlled by verifying the accuracy of the state data.

22 With power supply status monitoring:
This subclass is indented under subclass 15. Subject matter further including means or steps wherein recovery is controlled by a power supply status monitor.

SEE OR SEARCH CLASS:
713, Electrical Computers and Digital Processing Systems: Support, subclass 321 for electrical digital calculating computer (i.e., calculator) with power saving feature, and subclass 340, for generic power control monitoring in a digital data processing system environment.

23 Resetting processor:
This subclass is indented under subclass 2. Subject matter further including means or steps for recovery using clearing or initializing of a processor register.

24 Safe shutdown:
This subclass is indented under subclass 2. Subject matter further including means or steps for recovery including termination of a system component to a safe condition.

(1) Note. Isolating (i.e., disabling) an output of a failed network, processor, memory, peripheral, I/O, or power supply component is classified elsewhere. See SEE OR SEARCH THIS CLASS, SUBCLASS notes below.

SEE OR SEARCH THIS CLASS, SUBCLASS:

4.1 through 4.5, for network affected fault recovery.

5.1 through 6.23, for memory or peripheral subsystem affected.

6.13, for isolating failed storage locations.

10, for processor affected fault recovery.

14, for power supply affected fault recovery.

SEE OR SEARCH CLASS:

713, Electrical Computers and Digital Processing Systems: Support, subclasses 300+, for power control in a digital data processing system environment.

25 Fault locating (i.e., diagnosis or testing):

This subclass is indented under subclass 1. Subject matter further including means or steps for pinpointing a fault using either a reactive diagnosing or a proactive testing, including testing for developmental stage fault avoidance, for assurance, or for maintenance.

(1) Note. An invention directed to locating a fault in a digital data processing system including more than nominal data processing, or where the fault is specific to a nongeneral use of a digital data processing system, is classified here. fault locating in combination with a specific art device not of the basic subject matter of this class is classified with the art device.

SEE OR SEARCH CLASS:

324, Electricity: Measuring and Testing, subclass 73.1 for various electrical testing arrangements that may include fault locating.

370, Multiplex Communications, subclasses 241+ for diagnostic testing in multiplex communications.

399, Electrophotography, subclasses 9+ for diagnostic testing of a photocopier, including computer controlled malfunction warning and recovery.

26 Artificial intelligence (e.g., diagnostic expert system):

This subclass is indented under subclass 25. Subject matter wherein the testing is performed using an artificial intelligence technique; e.g., fault tree, reasoning rules, self-learning.

SEE OR SEARCH CLASS:

706, Data Processing: Artificial Intelligence, appropriate subclasses, for artificial intelligence, per se.

27 Particular access structure:

This subclass is indented under subclass 25. Subject matter further including means or steps related to an access structure specialized for observing or controlling a test or diagnosis.

28 Substituted emulative component (e.g., emulator microprocessor):

This subclass is indented under subclass 27. Subject matter further including means or steps for using a tester component that can emulate (i.e., functionally operate as) a normal component in the tested system.

SEE OR SEARCH CLASS:

703, Data Processing: Structural Design, Modeling, Simulation, and Emulation, appropriate subclasses.

716, Computer-Aided Design and Analysis of Circuits and Semiconductor Masks, appropriate subclasses.

29 Memory emulator feature:

This subclass is indented under subclass 28. Subject matter further including means or steps for using memory that can functionally replace a system component.

(1) Note. For classification here the replaced component need not be a memory.

SEE OR SEARCH CLASS:

703, Data Processing: Structural Design, Modeling, Simulation, and Emulation, appropriate subclasses for general purpose simulation or emulation of system components.

30 Built-in hardware for diagnosing or testing within-system component (e.g., microprocessor test mode circuit, scan path):
This subclass is indented under subclass 27. Subject matter further including means or steps for testing or diagnostic access using specialized testing or diagnosing hardware permanently built into a component of the system being tested or diagnosed.

31 Additional processor for in-system fault locating (e.g., distributed diagnosis program):
This subclass is indented under subclass 27. Subject matter further including an additional processor for controlling all or part of in-system testing or diagnosis.

32 Particular stimulus creation:
This subclass is indented under subclass 25. Subject matter further including means or steps for selection or generation of a signal (i.e., data) for testing or diagnosing.

SEE OR SEARCH THIS CLASS, SUBCLASS:
712+, for memory testing including pattern generation.

SEE OR SEARCH CLASS:
365, Static Information Storage and Retrieval, subclass 201 for static memory testing.

33 Derived from analysis (e.g., of a specification or by simulation):
This subclass is indented under subclass 32. Subject matter further including means or steps for deriving a test or diagnosis program based on an analysis of specification, design, or output of the system to be tested or diagnosed.

SEE OR SEARCH CLASS:
324, Electricity: Measuring and Testing, subclass 73.1 for various electrical testing arrangements that may include fault locating.
703, Data Processing: Structural Design, Modeling, Simulation, and Emulation, subclasses 13 through 22 for simulating electronic device and electrical system.
716, Computer-Aided Design and Analysis of Circuits and Semiconductor Masks, appropriate subclasses.

34 Halt, clock, or interrupt signal (e.g., freezing, hardware breakpoint, single-stepping):
This subclass is indented under subclass 32. Subject matter further including means or steps for controlling a processor or digital data processing system to be tested or diagnosed by applying an interrupt, halt, or clock signal to a processor or digital data processing system.

SEE OR SEARCH CLASS:
710, Electrical Computers and Digital Data Processing Systems: Input/Output, subclasses 48+, for Input/Output device interrupt processing.
711, Electrical Computers and Digital Processing Systems: Memory, subclass 204 for virtual address branch or jump address predicting; and subclasses 213 for generalized prefetch, look-ahead, jump, or predictive address generating.
712, Electrical Computers and Digital Processing Systems: Processing Architecture and Instruction Processing (e.g., Processors), subclass 227, for instruction processing in support of testing, debugging, emulation, etc.
713, Electrical Computers and Digital Processing Systems: Support, subclasses 500+, for clock processing, per se.
717, Data Processing: Software Development, Installation, and Management, subclasses 100 through 167 for software development tools.

35 Substituted or added instruction (e.g., code instrumenting, breakpoint instruction):
This subclass is indented under subclass 32. Subject matter further including means or steps for substituting or adding a testing or diagnosing instruction into a program or instruction data stream of a processor or digital data processing system being tested or diagnosed.

SEE OR SEARCH CLASS:
712, Electrical Computers and Digital Processing Systems: Processing Architecture and Instruction Processing (e.g., Processors), appropriate subclasses for instruction processing, per

se, including instruction alignment, fetching and decoding, and for processing control at the processor level, per se, particularly subclass 227, for instruction processing in support of testing, debugging, emulation, etc.

36 Test sequence at power-up or initialization:
This subclass is indented under subclass 32. Subject matter further including means or steps for performing a sequence of tests automatically in response to a power-up or initialization action.

SEE OR SEARCH CLASS:
710, Electrical Computers and Digital Data Processing Systems: Input/Output, appropriate subclasses, for assigning operating characteristics to peripherals, particularly subclass 104, for utilizing a hardware structure for providing a processor with an arrangement of the digital data processing system including characteristics of the digital data processing system's components.
711, Electrical Computers and Digital Processing Systems: Memory, subclass 170 for automatically determining and allocating memory space or specifying an allocation.
713, Electrical Computers and Digital Processing Systems: Support, subclasses 1 through 100, for digital data processing system initialization and configuration at boot-time.

37 Analysis (e.g., of output, state, or design):
This subclass is indented under subclass 25. Subject matter further including means or steps for evaluating the output, state, or design, of a computer system or a processor or a program, for fault locating.

SEE OR SEARCH CLASS:
324, Electricity: Measuring and Testing, subclass 73.1 for various electrical testing arrangements that may include fault locating.
703, Data Processing: Structural Design, Modeling, Simulation, and Emulation, subclasses 13 through 22 for the use of database in simulating electronic device and electrical system.
716, Computer-Aided Design and Analysis of Circuits and Semiconductor Masks, appropriate subclasses.

38.1 Of computer software faults:
This subclass is indented under subclass 37. Subject matter further including means or steps for locating a fault in software or testing software for determining the location of a fault.

(1) Note. This subclass also provides for detecting an error in instruction data in combination with a digital data processing system. Analysis or monitoring of program code execution is used for the purpose of fault location and recovery during actual use of computer software, and it is used subsequent to software development.

(2) Note. This subclass also provides for fault locating in software analysis by mechanisms such as debugging, automatic code generating, object oriented design, etc.

(3) Note. Generic coded information error detection for determining efficiency of a program during execution, so as to utilize the determination in debugging of the software during the development process, is classified elsewhere. See SEE OR SEARCH CLASS notes below.

SEE OR SEARCH THIS CLASS, SUBCLASS:
799, through 824, for coded information error detecting.

SEE OR SEARCH CLASS:
703, Data Processing: Structural Design, Modeling, Simulation, and Emulation, subclass 22 for modeling (i.e., artificially mimic) a computer software program so as to predict or analyze its performance.
717, Data Processing: Software Development, Installation, and Management, subclasses 131 through 133 for determining efficiency of program execution time analysis.

38.11 Memory dump:
This subclass is indented under subclass 38.1. Subject matter further including means or steps for generating a memory image of the existing state of software executing on the system at the time of a crash.

38.12 Time-out (i.e., of program):
This subclass is indented under subclass 38.1. Subject matter further including an event which occurs at the end of a predetermined interval of time during testing of the software.

38.13 Interrupt (i.e., halt the program):
This subclass is indented under subclass 38.1. Subject matter comprising means or steps for executing reset interruption or interruption signal, for example, for a break command.

38.14 By remotely:
This subclass is indented under subclass 38.1. Subject matter wherein fault location determination during software testing or analysis is performed remotely.

39 Monitor recognizes sequence of events (e.g., protocol or logic state analyzer):
This subclass is indented under subclass 37. Subject matter further including means or steps for locating a fault by using a monitor for classifying or otherwise recognizing a sequence of events.

SEE OR SEARCH CLASS:
709, Electrical Computers and Digital Processing Systems: Multicomputer Data Transferring or Plural Processor Synchronization, subclass 224 for computer network managing including monitoring.

40 Component dependent technique:
This subclass is indented under subclass 25. Subject matter further including means or steps for fault locating that are specific to a device under test.

41 For reliability enhancing component (e.g., testing backup spare, or fault injection):
This subclass is indented under subclass 40. Subject matter further including means or steps for fault locating specific to fault in a reliability enhancing component.

42 Memory or storage device component fault:
This subclass is indented under subclass 40. Subject matter further including means or steps for fault locating specific to a fault in a memory.

43 Bus, I/O channel, or network path component fault:
This subclass is indented under subclass 40. Subject matter further including means or steps for fault locating specific to a fault in a bus, peripheral or I/O channel, or network path.

SEE OR SEARCH CLASS:
710, Electrical Computers and Digital Data Processing Systems: Input/Output, subclasses 100+, for subject matter directed to system intraconnecting and bus access processing.

44 Peripheral device component fault:
This subclass is indented under subclass 40. Subject matter further including means or steps for fault locating specific to a fault in a peripheral device.

SEE OR SEARCH CLASS:
710, Electrical Computers and Digital Data Processing Systems: Input/Output, appropriate subclasses, for subject matter directed to Input/Output processing and communication between peripherals and computers or digital data processing systems.

45 Output recording (e.g., signature or trace):
This subclass is indented under subclass 25. Subject matter further including means or steps for recording output from the system under test or diagnosis.

SEE OR SEARCH THIS CLASS, SUBCLASS:
47.1 through 47.3, for error logging without recording.
48, for error detecting, per se.

46 Operator interface for diagnosing or testing:
This subclass is indented under subclass 25. Subject matter further including means or steps for interfacing with an operator for fault locating.

SEE OR SEARCH CLASS:

715, Data Processing: Presentation Processing of Document, Operator Interface Processing, and Screen Saver Display Processing, subclasses 700 through 866 for computer graphics operator interface.

47.1 Performance monitoring for fault avoidance:

This subclass is indented under subclass 1. Subject matter further including means or steps for monitoring event duration and event counts for anticipating or recognizing faults.

(1) Note. This subclass relates to the fault avoidance species of reliability.

(2) Note. This subclass includes event duration and counting arrangements for statistical analysis of system operations and predictive methods of fault avoidance.

SEE OR SEARCH CLASS:

368, Horology: Time Measuring Systems or Devices, subclasses 1 through 327 for time measurement.

377, Electrical Pulse Counters, Pulse Dividers, or Shift Registers: Circuits and Systems, subclasses 64 through 81 for shift registers, and subclasses 107-111 for counters.

702, Data Processing: Measuring, Calibrating, or Testing, subclasses 182 through 186 for performance or efficiency evaluation in a computer data processing system for measuring, calibrating, or testing purposes.

705, Data Processing: Financial, Business Practice, Management, or Cost/Price Determination, subclasses 7.11 through 7.42 for operations research.

708, Electrical Computers: Arithmetic Processing and Calculating, subclasses 200 through 714 for various arithmetic data processing operations performed by digital calculating computers.

709, Electrical Computers and Digital Processing Systems: Multicomputer Data Transferring, subclass 224 for computer network managing including monitoring.

47.2 Threshold:

This subclass is indented under subclass 47.1. Subject matter further including means or steps for establishing the minimum value of a signal that can be detected by the system for monitoring event duration and event counts for anticipating or recognizing faults.

47.3 Trends (i.e., expectancy):

This subclass is indented under subclass 47.1. Subject matter further including means or steps that use the data from measured characteristics, events, or conditions to calculate the length of time to a potential future failure.

48 Error detection or notification:

This subclass is indented under subclass 1. Subject matter further including means or steps for automated on-line sensing of errors, or for storing or propagating such error information (e.g., error logging).

SEE OR SEARCH THIS CLASS, SUBCLASS:

1+, for fault recovery in combination with error detecting or notifying.

25+, for fault locating combined with error detecting or notifying.

47.1 through 47.3, for performance monitoring for fault avoidance in combination with error detecting or notifying.

SEE OR SEARCH CLASS:

707, Data Processing: Database, Data Mining, and File Management or Data Structures, subclass 699 for use of CRC for data integrity in database and file management.

49 State error (i.e., content of instruction, data, or message):

This subclass is indented under subclass 48. Subject matter further including means or steps for detecting an error based on the information content of an instruction, a message, or data.

50 State out of sequence:

This subclass is indented under subclass 49. Subject matter wherein an ordering of state information related to a succession of data, instructions etc., is the basis for state analysis.

SEE OR SEARCH CLASS:

710, Electrical Computers and Digital Data Processing Systems: Input/Output, subclasses 260+ for Input/Output device interrupt processing.

711, Electrical Computers and Digital Processing Systems: Memory, subclass 204 for virtual address branch or jump address predicting; and subclass 213 for generalized prefetch, look-ahead, jump, or predictive address generating.

712, Electrical Computers and Digital Processing Systems: Processing Architecture and Instruction Processing (e.g., Processors), appropriate subclasses for instruction fetching and prefetching and for branching instruction processing and for task management and control, per se.

51 Control flow state sequence monitored (e.g., watchdog processor for control-flow checking):

This subclass is indented under subclass 50. Subject matter to detect state errors in an instruction data sequence.

52 Error checking code:

This subclass is indented under subclass 50. Subject matter for detecting consistency of information by using a code (e.g., parity, etc.) which is generated from the information.

(1) Note. Error checking codes are a function of the actual data of concern, as exemplified in one simple form by parity data.

SEE OR SEARCH THIS CLASS, SUBCLASS:

763+, for memory access block coding, and subclass 805 for storage accessing.

SEE OR SEARCH CLASS:

711, Electrical Computers and Digital Processing Systems: Memory, subclasses 161+ for preventing the corruption, loss, alteration, or disclosure of data by storing, as in making backup copies.

53 Address error:

This subclass is indented under subclass 49. Subject matter further including means or steps for detection or notification of error of address state.

54 Storage content error:

This subclass is indented under subclass 49. Subject matter further including means or steps for detection or notification of error of storage state.

SEE OR SEARCH CLASS:

711, Electrical Computers and Digital Processing Systems: Memory, subclass 144 for cache status data bits (e.g., bits indicating modified, valid, dirty data), wherein coherency for each unit or block of data includes associated identifier bit(s) to indicate the validity status of an associated cached location; subclass 156 for status storage control techniques including provisions for storing status data (e.g., control status words, program status words, etc.) associated with memory accessing and control; and subclass 165 for movement/transfers of data amongst locations within a same memory level.

55 Timing error (e.g., watchdog timer timeout):

This subclass is indented under subclass 48. Subject matter further including means or steps for detection or notification of error of timing.

SEE OR SEARCH CLASS:

713, Electrical Computers and Digital Processing Systems: Support, subclass 375 for synchronization maintenance of plural processors, subclasses 400-401 for clock synchronization, per se, and subclasses 500-503 for digital data processing system clock, pulse and timing interval generation, per se.

718, Electrical Computers and Digital Processing Systems: Virtual Machine Task or Process Management or Task Management/Control, subclass 1 for virtual machine task or process management and 100-108 for task management or control, in general.

56 Bus or I/O channel device fault:
This subclass is indented under subclass 55. Subject matter further including means or steps for detecting errors related to a flaw in a bus, peripheral, or I/O channel device.

SEE OR SEARCH CLASS:
710, Electrical Computers and Digital Data Processing Systems: Input/Output, appropriate subclasses for system intraconnecting and bus processing, per se.

57 Error forwarding and presentation (e.g., operator console, error display):
This subclass is indented under subclass 48. Subject matter further including means or steps for propagating error information so as to make notification of detected error.

SEE OR SEARCH CLASS:
345, Computer Graphics Processing and Selective Visual Display Systems, appropriate subclasses for information displaying.

100 DATA PROCESSING SYSTEM ERROR OR FAULT HANDLING
This subclass is indented under the class definition. Subject matter for enhancing the ability of a system, which is programmed for organization or manipulation of data, to respond to an unexpected hardware or software failure.

(1) Note. Classification herein requires more than nominal recitation of data processing components in combination with means or steps for furthering correct data processing operations by mechanisms including error detecting, performance monitoring, fault locating, and fault recovery.

(2) Note. The species of reliability and availability directed to memory accessing and control with data archiving, backups, device access limiting, and security are classified elsewhere, see the SEE OR SEARCH CLASS notes below, other species of reliability and availability in memory accessing and control such as isolating failed memory and storing redundant data are classified herein.

SEE OR SEARCH CLASS:
380, Cryptography, subclasses 3+ for stored information access or copy prevention (e.g., software program protection or computer virus protection) in combination with data encryption, and subclasses 22 - 25 and 50 for electric signal modification and other appropriate subclasses.
707, Data Processing: Database, Data Mining, and File Management or Data Structures, subclass 699 for use of CRC for data integrity in database and file management.
726, Information Security, subclasses 1 through 36 for information security in computers or digital processing system.

699 PULSE OR DATA ERROR HANDLING
This subclass is indented under the class definition. Subject matter further including means or steps for detecting and/or correcting errors in electrical pulse or pulse coded data, in addition, electrical based systems or devices which utilize techniques for detecting an error or fault condition, without recitation of specific data processing system components, are classified herein, said techniques include testing and diagnosis at the logic/component level.

(1) Note. Fault detection herein excludes processes and apparatus wherein there is no actual testing using digital data containing intelligence.

(2) Note. This class does not include detecting the distortion or degradation of pulse coded data per se, but rather includes detecting and/or correcting of errors in the information content of pulse or pulse coded data which may have occurred due to distortion or degradation of the coded data, thereby changing the state or value of the information content to such an extent as to comprise an error by definition.

(3) Note. Nominally recited art devices or systems external to this class, claimed in combination with subject matter under the class definition, are classified in this class, for example, static memory

devices claimed in combination with error correcting encoding/decoding apparatus are classified herein, and a nominally recited telecommunications switching system claimed in combination with fault diagnostic and/or recovery apparatus would also be classified herein.

(4) Note. Significantly claimed apparatus external to this class claimed in combination with apparatus under the class definition, which perform fault detection/correction techniques, are classified with the external apparatus, for example, a significantly claimed multiplex communication apparatus that performs general testing of its components would be found elsewhere, see SEE OR SEARCH CLASS below.

SEE OR SEARCH CLASS:

341, Coded Data Generation or Conversion, various subclasses for systems related to generic systems for either (a) originating or emitting a coded set of discrete signals or (b) translating one code into another code wherein the information signal content remains the same but the formats may differ.

358, Facsimile and Static Presentation Processing, subclasses 406 and 504 for systems where a facsimile apparatus is monitored, measured, calibrated, or tested.

360, Dynamic Magnetic Information Storage or Retrieval, subclasses 26, 36, 38, 47, and 53 for testing dynamic magnetic memory systems.

370, Multiplex Communications, subclasses 13+ and 100+ for subject matter wherein part of a multiplex system is monitored and tested to evaluate its performance, including circuit continuity checking, repeater testing, loopback testing, and alternate routing due to failure.

375, Pulse or Digital Communications, subclasses 213 and 224 - 228 for testing pulse or digital communication systems.

379, Telephonic Communications, subclasses 1 through 33 for testing of telephone circuits.

700 SKEW DETECTION/CORRECTION:

This subclass is indented under subclass 699. Subject matter in which an error caused by the time delay between plural parallel bits forming a byte or data word is detected or corrected.

SEE OR SEARCH CLASS:

360, Dynamic Magnetic Information Storage or Retrieval, subclass 26 for electronically correcting phasing errors between related information signals.

701 DATA FORMATTING TO IMPROVE ERROR DETECTION/CORRECTION CAPABILITY:

This subclass is indented under the class definition. Subject matter in which a change in data format or sequence is utilized to improve the error detection/correction capability of a coding scheme.

702 Memory access (e.g., address permutation):

This subclass is indented under subclass 701. Subject matter which changes the format of digital data by having the signal with the data written into or read out of a storage device.

(1) Note. Address permutation arrangements are included in this subclass.

SEE OR SEARCH THIS CLASS, SUBCLASS:

718, for diagnostic testing of a memory.

703 TESTING OF ERROR-CHECK SYSTEM:

This subclass is indented under the class definition. Subject matter in which the proper operation of the error detection/correction or fault detection/recovery apparatus itself is verified.

704 Error count or rate:

This subclass is indented under the class definition. Subject matter which determines the number of bits in error or the number of bits in error per unit of time.

SEE OR SEARCH THIS CLASS, SUBCLASS:

798, for this subject matter combined with control of synchronization in response to an error detection signal.

705 Pseudo-Error rate:

This subclass is indented under subclass 704. Subject matter having a main data path and a secondary data path having intentionally degraded performance connected in parallel, the secondary path having a decision device to compare and evaluate the disagreement between the paths.

(1) Note. Each disagreement is called a pseudo-error.

706 Up-down counter:

This subclass is indented under subclass 704. Subject matter including an reversible accumulating register which counts up in response to an error and counts down in response to an error-free increment of time.

SEE OR SEARCH CLASS:

377, Electrical Pulse Counters, Pulse Dividers, or Shift Registers: Circuits and Systems, appropriate subclasses for up-down counters per se.

707 Synchronization control:

This subclass is indented under subclass 704. Subject matter in which a determination of the error rate is used to control synchronization between devices.

SEE OR SEARCH THIS CLASS, SUBCLASS:

798+, for error detection controlled synchronization control other than by error rate.

708 Shutdown or establishing system parameter (e.g., transmission rate):

This subclass is indented under subclass 704. Subject matter including control of system operation by either deactivation of the system, or controls a parameter related to normal system operation, in response to error count or error rate.

709 DATA PULSE EVALUATION/BIT DECISION:

This subclass is indented under subclass 699. Subject matter in which the information bearing parameter (amplitude, pulse position, etc.) of a data pulse is evaluated to determine the proper logic state or value.

(1) Note. Subject matter in this subclass relates to determining if a data pulse represents a particular given logic state, e.g., logic one as opposed to logic zero.

SEE OR SEARCH CLASS:

327, Miscellaneous Active Electrical Nonlinear Devices, Circuits, and Systems, subclasses 1+ for pulse selecting means.

329, Demodulators, subclasses 311+ for pulse demodulation or detection, per se.

710 REPLACEMENT OF MEMORY SPARE LOCATION, PORTION, OR SEGMENT:

This subclass is indented under subclass 699. Subject matter in which the spare apparatus comprises only a location, or a contiguous group of locations of memory.

SEE OR SEARCH CLASS:

365, Static Information Storage and Retrieval, subclasses 200 and 201 for bad bit and testing read/write circuits, respectively.

711 Spare row or column:

This subclass is indented under subclass 710. Subject matter spare apparatus comprises only a column or row within a memory device or element.

712 TRANSMISSION FACILITY TESTING:

This subclass is indented under subclass 699. Subject matter in which the diagnostic testing is performed upon a channel of a transmission medium with a device for supplying digital data thereto.

(1) Note. The transmission facility includes the transmission medium and all associated equipment required to transmit a message.

SEE OR SEARCH CLASS:

370, Multiplex Communications, subclasses 241+ for testing of multiplex communication systems.

375, Pulse or Digital Communications, subclasses 224+ for testing of pulse or digital communications system.

379, Telephonic Communications, 1.01-33 for diagnostic testing of telephone equipment.

713 For channel having repeater:

This subclass is indented under subclass 712. Subject matter wherein a transmission channel has a repeating amplifier.

714 By tone signal:

This subclass is indented under subclass 712. Subject matter which includes application of a test signal composed of one or more tone signals.

715 Test pattern with comparison:

This subclass is indented under subclass 712. Subject matter in which the transmission facility is tested by applying a test pattern to the device under test and comparing the output to a reference test pattern.

716 Loop-back:

This subclass is indented under subclass 715. Subject matter in which the transmission facility is configured so that the receiver shunts the test pattern back to transmitter for comparison at the transmitter.

717 Loop or ring configuration:

This subclass is indented under subclass 712. Subject matter in which a plurality of transmission stations or devices are configured in a serial fashion to form a loop or ring.

718 MEMORY TESTING:

This subclass is indented under subclass 699. Subject matter in which the diagnostic testing is performed upon an information signal storage device.

SEE OR SEARCH THIS CLASS, SUBCLASS:

710+, for fault recovery of memory devices.

SEE OR SEARCH CLASS:

324, Electricity: Measuring and Testing, subclasses 210+ for testing of magnetic memory elements, per se.

360, Dynamic Magnetic Information Storage or Retrieval, subclasses 26, 47, and 53 for testing of dynamic magnetic memory systems.

365, Static Information Storage and Retrieval, subclass 200 a bad bit memory used to store information; and subclass 201 for specifics of a memory which is tested but doesn't include data processing techniques.

386, Motion Video Signal Processing for Recording or Reproducing, subclasses 263 through 277 for video error or fault detection and/or correction during recording or reproduction operation.

719 Read-in with read-out and compare:

This subclass is indented under subclass 718. Subject matter in which the testing is done by reading in a test pattern, reading out the contents of the memory and comparing the output with the test pattern read in.

720 Special test pattern (e.g., checkerboard, walking ones):

This subclass is indented under subclass 719. Subject matter in which the test patterns are selected to exercise the memory by transferring a combination of logic zeroes and ones through the memory, e.g., alternating zeroes and ones-checkerboard pattern.

721 Electrical parameter (e.g., threshold voltage):

This subclass is indented under subclass 718. Subject matter in which the diagnostic test measures an electrical parameter of the memory device, e.g., threshold voltage.

722 Performing arithmetic function on memory contents:

This subclass is indented under subclass 718. Subject matter in which the diagnostic test consists of performing an arithmetic function, such as addition, on the contents of the memory and comparing the results to a reference value.

723 Error mapping or logging:
This subclass is indented under subclass 718. Subject matter in which the detected error or fault is registered or recorded to present a history for diagnostic purposes.

SEE OR SEARCH THIS CLASS, SUBCLASS:
42, for such subject matter used with data processor testing.

724 DIGITAL LOGIC TESTING:
This subclass is indented under subclass 699. Subject matter in which the diagnostic test is performed upon a system or element performing a binary logic operation upon a signal having plural distinct discrete states.

(1) Note. Testing or measuring of electrical properties are classified elsewhere unless the testing device includes analysis of the information content of a digital signal. Control signals are not data signals.

SEE OR SEARCH CLASS:
324, Electricity: Measuring and Testing, appropriate subclass, particularly subclass 73 for measuring and testing of electrical device parameters under controlled conditions.
326, Electronic Digital Logic Circuitry, subclass 16 for electronic digital logic circuitry with test facilitating feature and subclasses 21+ for electronic digital logic circuitry maintaining signal integrity.

725 Programmable logic array (PLA) testing:
This subclass is indented under subclass 724. Subject matter for testing an array of logical elements selectively configurable to sequentially perform various binary logic functions.

(1) Note. Examples of such binary logic functions are AND, OR, NAND, NOR, and NOT.

SEE OR SEARCH CLASS:
324, Electricity: Measuring and Testing, appropriate subclass, particularly subclass 73.1 for measuring and testing of electrical device parameters under controlled conditions.
326, Electronic Digital Logic Circuitry, subclass 16 for electronic digital logic circuitry with test facilitating feature, subclasses 21+ for electronic digital logic circuitry maintaining signal integrity, and subclasses 37+ for a programmable or multifunctional logic array circuit, per se.

726 Scan path testing (e.g., level sensitive scan design (LSSD)):
This subclass is indented under subclass 724. Subject matter in which digital logic is designed for improved testability by including shift register latches (SRL) to enable the configuring of the circuitry into combinational logic form.

(1) Note. Test data is clocked (scanned) through the combinational logic forms and then compared to a reference.

SEE OR SEARCH THIS CLASS, SUBCLASS:
738+, for digital logic testing including test pattern generation in general.

SEE OR SEARCH CLASS:
326, Electronic Digital Logic Circuitry, subclass 16 for logic circuitry with test feature.
377, Electrical Pulse Counters, Pulse Dividers, or Shift Registers: Circuits and Systems, appropriate subclasses for shift register latches, per se.

727 Boundary scan:
This subclass is indented under subclass 726. Subject matter where selected components in a circuit are each provided with one or more cells, comprising a single-bit register, coupled to a node of a component, such as an input, output, input/output or control node, and where said cells are serially coupled in a single chain, usually referred to as a boundary-scan chain.

728 Random pattern generation (includes pseudorandom pattern)

This subclass is indented under subclass 726. Subject matter where a series of digits is generated in an unpredictable, incoherent, or arbitrary pattern.

(1) Note. Included herein is generation of a series of digits which simulates a random pattern.

SEE OR SEARCH THIS CLASS, SUBCLASS:

715, for test pattern with comparison in testing a transmission facility.

720, for use of special test patterns in memory testing.

739, for random test pattern generation in general.

SEE OR SEARCH CLASS:

708, Electrical Computers: Arithmetic Processing and Calculating, subclasses 250+ for random number generation.

729 Plural scan paths:

This subclass is indented under subclass 726. Subject matter having more than one group of shift register latches connected in series, and which groups form a plurality of shift paths (scan paths) along which data can be transmitted.

730 Addressing:

This subclass is indented under subclass 726. Subject matter including data which specifies a location.

SEE OR SEARCH THIS CLASS, SUBCLASS:

743, for addressing in digital logic testing using a test pattern generator.

SEE OR SEARCH CLASS:

365, Static Information Storage and Retrieval, subclasses 230.01+ for addressing memories.

711, Electrical Computers and Digital Processing Systems: Memory, subclasses 200+ for address formation in data processing systems.

731 Clock or synchronization:

This subclass is indented under subclass 726. Subject matter including a reference timing function or a clock-pulse generator for causing the various parts of the device to operate on a common time base.

SEE OR SEARCH THIS CLASS, SUBCLASS:

744, for clock or synchronization in digital logic testing using a test pattern generator.

SEE OR SEARCH CLASS:

326, Electronic Digital Logic Circuitry, subclasses 93+ for clocking or synchronization of logic stages or gates.

327, Miscellaneous Active Electrical Nonlinear Devices, Circuits, and Systems, subclasses 141+ for synchronizing electrical nonlinear devices.

713, Electrical Computers and Digital Processing Systems: Support, subclasses 400 through 503 for synchronization in computer systems.

732 Signature analysis:

This subclass is indented under subclass 724. Subject matter controlled including monitoring of controlled conditions of execution test points or nodes within the digital logic device and the measured output (signature) is compared to a known good signature.

733 Built-in test circuit (BILBO):

This subclass is indented under subclass 724. Subject matter in which the digital logic testing equipment includes a selectively configurable shift register, structurally a part of the device being tested.

(1) Note. Some selective configurations of the shift register include a latch, linear shift register, multiple input signature register, and a forced reset.

(2) Note. Included herein are built-in logic block observation (BILBO) devices.

SEE OR SEARCH CLASS:

324, Electricity: Measuring and Testing, appropriate subclass, particularly subclass 73.1 for measuring and testing of electrical device parameters under controlled conditions.

377, Electrical Pulse Counters, Pulse Dividers, or Shift Registers: Circuits and Systems, subclasses 19+ for a shift register used for measuring or testing; and subclass 28 for error checking or correction in a shift register system.

734 Structural (in-circuit test):

This subclass is indented under subclass 724. Subject matter in which each component of the logic circuit is tested individually while physically connected to the circuit.

(1) Note. Generally, the test instrument is connected to nodes of the logic circuit under test in a unique way for each component.

SEE OR SEARCH CLASS:

324, Electricity: Measuring and Testing, appropriate subclass, particularly subclass 73.1 for measuring and testing of electrical device parameters (other than by information signal content) under controlled conditions.

735 Device response compared to input pattern:

This subclass is indented under subclass 724. Subject matter in which the operational condition of a system or device is determined by comparing the system or device response to a test signal input pattern.

736 Device response compared to expected fault-free response:

This subclass is indented under subclass 724. Subject matter in which the operational condition of a system or device is determined by comparing the system or device response to a predetermined fault-free response.

737 Device response compared to fault dictionary/truth table:

This subclass is indented under subclass 724. Subject matter in which the operational condition and identification of an actual or potential fault is determined by comparing the system response to a predetermined fault dictionary or truth table.

738 Including test pattern generator:

This subclass is indented under subclass 724. Subject matter in which the specific means or method of generating a test pattern for a digital logic testing system is claimed.

SEE OR SEARCH CLASS:

327, Miscellaneous Active Electrical Nonlinear Devices, Circuits, and Systems, subclasses 100+ for miscellaneous waveform generation or conversion.

345, Computer Graphics Processing and Selective Visual Display Systems, subclass 26, 345, 551 for character generator in a visual display system with selective electrical control.

708, Electrical Computers: Arithmetic Processing and Calculating, subclasses 250+ for random number generators, and subclasses 270+ for digital function generators.

739 Random pattern generation (includes pseudorandom pattern):

This subclass is indented under subclass 738. Subject matter where a series of digits is generated in an unpredictable, incoherent or arbitrary pattern.

(1) Note. Included herein is generation of a series of digits which simulates a random pattern.

SEE OR SEARCH THIS CLASS, SUBCLASS:

715, for testing a transmission facility using a test pattern with comparison

720, for use of special test patterns in memory testing.

728, for random test pattern generation in boundary scanning.

SEE OR SEARCH CLASS:

708, Electrical Computers: Arithmetic Processing and Calculating, subclasses 250+ for random number generation.

740 Having analog signal:
This subclass is indented under subclass 738. Subject matter including an electrical signal, the amplitude or frequency of which varies continuously in value over time.

741 Simulation:
This subclass is indented under subclass 738. Subject matter having an electrical model or a computer program which imitates the operation of a device under test.

SEE OR SEARCH CLASS:
703, Data Processing: Structural Design, Modeling, Simulation, and Emulation, subclasses 3 through 5 for electrical analog simulator, subclasses 6-12 for simulating nonelectrical device or system, and subclasses 13-22 for simulating electronic device and electrical system.

742 Testing specific device:
This subclass is indented under subclass 738. Subject matter where the test pattern is applied to a distinctive named means to carry out a special function.

(1) Note. Examples of things that are not specific devices include "logic device," "circuit," "device under test," etc.

(2) Note. See sections D and E of the class definition for the distinction between this class and classes having the specific device.

SEE OR SEARCH THIS CLASS, SUBCLASS:
718+, for testing an information signal storage device.

743 Addressing:
This subclass is indented under subclass 738. Subject matter including data which specifies a location.

SEE OR SEARCH THIS CLASS, SUBCLASS:
730, for scan path testing with addressing.

SEE OR SEARCH CLASS:
365, Static Information Storage and Retrieval, subclasses 230.01+ for addressing memories.
711, Electrical Computers and Digital Processing Systems: Memory, subclasses 1+ and 200+ for memory address formation in data processing systems.

744 Clock or synchronization:
This subclass is indented under subclass 738. Subject matter including a reference timing function or a clock pulse generator for causing the various parts of the device to operate on a common time base.

SEE OR SEARCH THIS CLASS, SUBCLASS:
731, for clocking or synchronizing in scan path testing.

SEE OR SEARCH CLASS:
326, Electronic Digital Logic Circuitry, subclasses 93+ for clocking or synchronizing of logic stages or gates.
327, Miscellaneous Active Electrical Nonlinear Devices, Circuits, and Systems, subclasses 141+ for synchronizing nonlinear devices, circuits, or systems.
713, Electrical Computers and Digital Processing Systems: Support, subclasses 400 through 503 for synchronization in computer systems.

745 Determination of marginal operation limits:
This subclass is indented under subclass 724. Subject matter in which the device or system is tested under controlled and varying circuit parameters, such as input voltage, to determine the range of circuit parameter values within which the device or system operates without error or malfunction.

746 DIGITAL DATA ERROR CORRECTION:
This subclass is indented under the class definition. Subject matter in which the error in information content of pulse or pulse coded data is corrected.

SEE OR SEARCH THIS CLASS, SUBCLASS:

799, for error detection which does not include correction of the error signal.

747 Substitution of previous valid data:

This subclass is indented under subclass 746. Subject matter in which a previously validated data state or value is substituted for data state or value determined to be erroneous.

748 Request for retransmission:

This subclass is indented under subclass 746. Subject matter in which the digital data error correction is achieved by retransmission of data responsive to a request.

749 Retransmission if no ACK returned:

This subclass is indented under subclass 748. Subject matter in which a retransmission of data is initiated upon the condition that no acknowledgment (ACK) signal is returned from the receiver.

750 Feedback to transmitter for comparison:

This subclass is indented under subclass 748. Subject matter in which the digital data is returned to the transmitter for comparison to detect an error.

751 Including forward error correcting capability:

This subclass is indented under subclass 748. Subject matter in which the digital data is encoded to enable error correction at the receiver and retransmission is requested only if the error rate exceeds the forward error correcting capability.

752 Forward correction by block code:

This subclass is indented under subclass 746. Subject matter in which a grouping of symbols (i.e., a block of data or a data word) is transformed into a code word having an increased number of symbols in order to provide an increased minimum distance between code words relative to the minimum distance of the corresponding data words in order to provide for forward correction of the encoded data in the event that an error or erasure is subsequently imposed on the encoded data.

(1) Note. This subclass includes both forward error correction, per se, (i.e., the receiver corrects the error without requiring any further information from the sender, which requires a minimum amount of redundancy in the transmission since not only must an error be detected, but its location must be determined) and forward error correction with the assistance of symbol reliability information.

(2) Note. Forward error correction (FEC) is an error-correcting technique that avoids the need for any reverse channel by enabling self-correction of errors at the receiver by adding information (at the expense of throughput) to enable the receiver to determine what the error was and the correct information to substitute for said error.

SEE OR SEARCH THIS CLASS, SUBCLASS:

786, for convolutional codes in which each check bit is generated as a function of a different plurality of information bits and is interspersed among the information bits at predetermined intervals with no natural beginning point or ending point.

753 Double error correcting with single error correcting code:

This subclass is indented under subclass 752. Subject matter in which a single bit error correcting code arrangement corrects double bit errors by successively correcting consecutive single bit errors.

754 Error correction during refresh cycle:

This subclass is indented under subclass 752. Subject matter including a digital data storage device having a refresh cycle in which decaying information is read before it becomes unrecognizable, and rewritten in original form, and decoding a stored block data code signal for error correction during the refresh cycle.

755 Double encoding codes (e.g., product, concatenated):
This subclass is indented under subclass 752. Subject matter including calculation and independent decoding of two independent sets of check words for enhancement of error correction.

756 Cross-interleave Reed-Solomon code (CIRC):
This subclass is indented under subclass 755. Subject matter doubly encoded with Reed-Solomon codes and interleaved to enable the correction of burst errors.

757 Parallel generation of check bits:
This subclass is indented under subclass 752. Subject matter having plural check bit calculating elements connected in parallel.

758 Error correcting code with additional error detection code (e.g., cyclic redundancy character, parity):
This subclass is indented under subclass 752. Subject matter which encodes digital data with both an error correcting code (ECC) for error correction and detection, and an additional error detection code to detect uncorrected errors.

(1) Note. Such additional codes include a cyclic redundancy code (CRC) and a parity bit code.

759 Look-up table encoding or decoding:
This subclass is indented under subclass 752. Subject matter having an encoder or decoder which contains a table of all possible error patterns in a corrupted received code word and compares the computed syndrome to these patterns to determine the position of erroneous bits.

760 Threshold decoding (e.g., majority logic):
This subclass is indented under subclass 752. Subject matter the decoder operates upon a corrupted received code word to compute the parity check sums which are applied to a threshold or majority gate and an error indicated if the sums exceed a certain value.

761 Random and burst error correction:
This subclass is indented under subclass 752. Subject matter in which the block code is capable of correcting both random and burst errors.

(1) Note. Random errors are of the type where each data bit is affected independently by noise. Burst errors are of the type where disturbances introduce errors of unspecified time duration and thus cause a cluster of multiple consecutive data bits in error.

(2) Note. Interlacing or interleaving techniques may be used to give a random error correcting code the capability of correcting both random and burst errors. A product code or concatenated code may be formed from two codes to provide both random and burst error correction capability.

762 Burst error correction:
This subclass is indented under subclass 752. Subject matter in which the block code is derived to be most effective in correcting burst errors.

(1) Note. An example of a block code with good burst-correcting capability is the Reed-Solomon code. Interleaving techniques are also utilized to improve the burst-correcting capability of a code.

763 Memory access:
This subclass is indented under subclass 752. Subject matter in which digital data being written into or read out of a storage device is encoded in a block code format.

SEE OR SEARCH THIS CLASS, SUBCLASS:
710+, for memory fault recovery systems.
718+, for diagnostic testing of a memory.

SEE OR SEARCH CLASS:
360, Dynamic Magnetic Information Storage or Retrieval, subclasses 26, 36.1+, 47, and 53 for error detection combined with a magnetic, dynamic memory system.

365, Static Information Storage and Retrieval, subclasses 200 and 201 for bad bit and testing read/write circuits, respectively.

369, Dynamic Information Storage or Retrieval, appropriate subclasses for a dynamic, nonmagnetic memory device.

764 Error correct and restore:
This subclass is indented under subclass 763. Subject matter which corrects the errors upon readout of the data and the corrected data in written into memory as a substitute for the erroneous data.

765 Error pointer:
This subclass is indented under subclass 763. Subject matter which generates a signal (pointer) upon the occurrence of a particular type of error or failure.

(1) Note. In many error correcting systems accessing data from a memory or storage device, the error pointer identifies the track or channel with which the error or failure is associated.

766 Check bits stored in separate area of memory:
This subclass is indented under subclass 763. Subject matter including a section of memory for storage of the check bits separate from that the section of memory storing data information.

767 Code word for plural n-bit (n>1) storage units (e.g., x 4 DRAM's):
This subclass is indented under subclass 763. Subject matter in which there is more than one storage device, each storing more than a single digit of data.

768 Error correction code for memory address:
This subclass is indented under subclass 763. Subject matter where the block code includes a memory address as part of the encoded data.

769 Dynamic data storage:
This subclass is indented under subclass 763. Subject matter where there is relative motion between a transducer and an information storage medium.

SEE OR SEARCH CLASS:

360, Dynamic Magnetic Information Storage or Retrieval, for dynamic magnetic data storage and retrieval.

369, Dynamic Information Storage or Retrieval, for dynamic data storage and retrieval.

770 Disk array:
This subclass is indented under subclass 769. Subject matter where the storage medium is a plurality of interconnected disks.

771 Tape:
This subclass is indented under subclass 769. Subject matter where the storage medium is essentially of a two dimensional shape with one dimension being very long in relation to the other.

772 Code word parallel access:
This subclass is indented under subclass 763. Subject matter in which the bits of the code word are created from parallel data digits.

773 Solid state memory:
This subclass is indented under subclass 763. Subject matter where the storage device is or contains a solid state device (e.g., an integrated circuit or transistor).

SEE OR SEARCH THIS CLASS, SUBCLASS:

718+, for memory testing.

SEE OR SEARCH CLASS:

65, Glass Manufacturing, subclasses 174+ for solid state memories.

774 Adaptive error-correction capability:
This subclass is indented under subclass 752. Subject matter in which the error-correction capability of the system is adapted to the existing error rate by selection of encoding format.

775 Synchronization:
This subclass is indented under subclass 752. Subject matter in which a lack of synchronization between encoder and decoder is detected and/or corrected.

776 For packet or frame multiplexed data:
This subclass is indented under subclass 752. Subject matter where plural encoded data streams are simultaneously transmitted over a common transmission medium in such a manner that the information signals may be discretely recovered, wherein each data stream contains one or more bytes preceded by an address header or where the simultaneously transmitted plurality of data streams include synchronization or other control information.

SEE OR SEARCH CLASS:
370, Multiplex Communications, subclasses 351+ for multiplex switching such as packet or frame switching.

777 Hamming code:
This subclass is indented under subclass 752. Subject matter where there are m information code elements and k error check code elements such that there are sufficient check elements to correct a single error and the k check elements are determined by even parity checks in conjunction with element values appearing in certain selected information positions where each of the elements of the code group must be in a parity check subgroup with one or more of the check elements and no two different code elements having exactly the same set of check elements associated with it.

(1) Note. See U.S. Patent RE23601, columns 5-9, for a more rigorous definition.

778 Nonbinary data (e.g., ternary):
This subclass is indented under subclass 752. Subject matter where each bit of a data word can assume more than two values.

SEE OR SEARCH CLASS:
326, Electronic Digital Logic Circuitry, subclasses 59+ for nonbinary logic circuits.

779 Variable length data:
This subclass is indented under subclass 752. Subject matter where the number of bits in a data word is not fixed, but can vary from word to word.

780 Using symbol reliability information (e.g., soft decision):
This subclass is indented under subclass 752. Subject matter where, during error correction, in addition to an error correcting code, use is made of information about the reliability of the decoding of a particular bit.

781 Code based on generator polynomial:
This subclass is indented under subclass 752. Subject matter where a code word c(x), where x is a unit delay operator, is generated by dividing a delayed version of the data polynomial d(x), i.e.,. xnd(x), by a generator polynomial, g(x), and subtracting the remainder from the delayed version of the data polynomial, thereby producing a code word that is a multiple of the generator polynomial, and where the data polynomial d(x) is such that positions within the block correspond to powers of x and data values at the positions correspond to polynomial coefficient values.

782 Bose-Chaudhuri-Hocquenghem code:
This subclass is indented under subclass 781. Subject matter where the block code is a t error correcting code which is the set of all polynomials [a(c)] over the Galois field GF(2m) of degree n-1 or less, such that a(ai)=0, for i=1,3,5,..., 2t-1 where a is a primitive element of the finite field GF(2m), and where c is the radix 2 for binary data, a(c)=a0+a1c+a2c2+...+an-1cn - 1, and aj=0,1 (j=0,1,2,..., n-1).

783 Golay code:
This subclass is indented under subclass 781. Subject matter where the block code is an (n, k, t) type polynomial code in which each code word is n=23 bits long, contains k=13 data or information bits, corrects up to t=3 errors, and the code word also contains (n-k)=10 redundant check bits.

784 Reed-Solomon code:
This subclass is indented under subclass 781. Subject matter where the block code consists of K data and N-K check symbols, where N is an arbitrary number and K is less than N, and where each symbol is made of J binary bits encoded with a generator polynomial g(x) for the code and a field generating polynomial M(x) which defines the Galois field.

SEE OR SEARCH THIS CLASS, SUBCLASS:

756, for cross-interleave Reed-Solomon codes.

762, for burst error correction using Reed-Solomon codes.

785 Syndrome computed:

This subclass is indented under subclass 781. Subject matter where decoded data is divided by an inverse of the generator polynomial to obtain a data word of 1 bit which indicate which bits of the decoded data are in error.

786 Forward error correction by tree code (e.g., convolutional):

This subclass is indented under subclass 746. Subject matter in which information bits are encoded to generate a plurality of check bits, each check bit is generated as a function of a different plurality of information bits and is interspersed among the information bits at predetermined intervals with no natural beginning point or ending point (i.e., there is no length restriction for the encoded data).

(1) Note. Convolutional coding means adding to the information a repeating sequence that is known to the receiver. By subtracting this repeating sequence and performing other tests, the receiver can determine what should have been received with a high degree of accuracy.

(2) Note. This subclass includes forward error correction, per se, (i.e., the receiver corrects the error without requiring any further information from the sender, which requires a minimum amount of redundancy in the transmission since not only must an error be detected, but its location must be determined) and forward error correction with the assistance of symbol reliability information.

(3) Note. This subclass does not include demodulation decisions based upon oversampling or on intersymbol interference alone.

(4) Note. This subclass does not include channel equalization or predistortion control based on correction results (e.g., decision feedback equalization).

(5) Note. This subclass does not include detection or correction of errors produced by trial values, perturbations, predictions, quantizations, estimations or approximations, which errors are used as feedback for control of signal generation or coding (e.g., PID controlling, source calibration, successive approximation A/D conversion, DSV constrained encoding, predictive encoding).

(6) Note. Forward error correction (FEC) is an error-correcting technique that avoids the need for any reverse channel by enabling self-correction of errors at the receiver by adding information (at the expense of throughput) to enable the receiver to determine what the error was and the correct information to substitute for said error.

SEE OR SEARCH THIS CLASS, SUBCLASS:

746 and 797, for various types of data correction such as trial values, perturbations, predictions, quantizations, estimations or approximations, which errors are used as feedback for control of signal generation or coding.

752+, for block codes wherein the information bits and associated bits form independent and distinct blocks of data bits.

799+, for various error/fault detection techniques such as those based on oversampling or intersymbol interference.

SEE OR SEARCH CLASS:

341, Coded Data Generation or Conversion, subclasses 50+ for digital data conversion and subclasses 126+ for analog to or from digital conversion.

375, Pulse or Digital Communications, subclasses 229+ for pulse or digital equalizers.

787 Random and burst errors:

This subclass is indented under subclass 786. Subject matter in which the convolutional code is capable of correcting both random and burst errors.

SEE OR SEARCH THIS CLASS, SUBCLASS:

761, for block code correction of both random and burst errors.

788 Burst error:

This subclass is indented under subclass 786. Subject matter in which the convolutional code corrects for burst error.

SEE OR SEARCH THIS CLASS, SUBCLASS:

762, for block code correcting of burst errors.

789 Synchronization:

This subclass is indented under subclass 786. Subject matter in which a lack of synchronization between the encoder and decoder is detected and/or corrected.

790 Puncturing:

This subclass is indented under subclass 786. Subject matter where single bits are periodically deleted at intervals from a low-rate convolutional code.

791 Sequential decoder (e.g., Fano or stack algorithm):

This subclass is indented under subclass 786. Subject matter where a tree structure of the convolutional code is used for searching locally a path which is considered to be the most likely to produce a correct data sequence.

SEE OR SEARCH THIS CLASS, SUBCLASS:

794, for maximum likelihood decoding in general.

796, for branch metric calculation in general.

792 Trellis code:

This subclass is indented under subclass 786. Subject matter where, for a convolutional code of k bits length, an inverse coding operation is performed in which 2k-1 decision bits are used to select an output bit and where after many branches, the most probable path will be selected with a high degree of certainty, and where the branches form a mesh pattern (i.e., branches start at a plurality of points and intersect other branches).

SEE OR SEARCH CLASS:

375, Pulse or Digital Communications, subclass 265 for trellis coders and decoders in pulse or digital communication.

704, Data Processing: Speech Signal Processing, Linguistics, Language Translation, and Audio Compression/Decompression, subclass 242 for Viterbi trellis speech recognition.

793 Syndrome decodable (e.g., self orthogonal):

This subclass is indented under subclass 786. Subject matter where decoded data is divided by an inverse of the generator polynomial to obtain a data word of 1 bit which indicate which bits of the decoded data are in error.

SEE OR SEARCH THIS CLASS, SUBCLASS:

785, for syndrome decodable block codes.

794 Maximum likelihood:

This subclass is indented under subclass 786. Subject matter where a decoder selects the sequence out of all the possible transmitted sequences which is most likely to match the received data sequence and determines corresponding digital (data) information.

SEE OR SEARCH THIS CLASS, SUBCLASS:

791, for a sequential decoder.

795, for Viterbi decoding.

SEE OR SEARCH CLASS:

375, Pulse or Digital Communications, subclasses 262 and 341 for maximum likelihood decoding (other than for error correction) in pulse or digital communication.

795 Viterbi decoding:

This subclass is indented under subclass 786. Subject matter where data is not decoded as soon as it is received, instead, a sequence of data, having a predetermined decoding depth, following the digit to be decoded is first collected, then, by computing what are known as path metrics, a limited number of possible messages are selected, each extending throughout the decoding depth far beyond the digit pres-

ently to be decoded, with one such survivor sequence ending in each of the data states.

SEE OR SEARCH THIS CLASS, SUBCLASS:
794, for maximum likelihood decoding.
796, for branch metric calculation decoding.

SEE OR SEARCH CLASS:
375, Pulse or Digital Communications, subclasses 262 and 341 for Viterbi decoding (other than for error correction) in pulse or digital communication.
704, Data Processing: Speech Signal Processing, Linguistics, Language Translation, and Audio Compression/Decompression, subclass 242 for Viterbi trellis speech recognition.

796 Branch metric calculation:
This subclass is indented under subclass 786. Subject matter where a tree of possible data sequences is constructed identifying the possible data sequences in terms of data states, and from which correlations are computed for selecting the paths which are to survive to the next stage of decoding received data.

SEE OR SEARCH THIS CLASS, SUBCLASS:
791, for sequential decoding.
795, for Viterbi decoding.

797 Majority decision/voter circuit:
This subclass is indented under subclass 746. Subject matter in which error correction is effectively achieved by error masking (making error invisible at output) through majority logic or voting techniques.

SEE OR SEARCH CLASS:
326, Electronic Digital Logic Circuitry, subclasses 35+ for threshold (e.g., majority) logic.

798 ERROR DETECTION FOR SYNCHRONIZATION CONTROL:
This subclass is indented under the class definition. Subject matter in which error detecting techniques are utilized to detect an out-of-synch condition or to control synchronization between devices.

SEE OR SEARCH THIS CLASS, SUBCLASS:
775, for block code synchronization error correction.
789, for convolutional code synchronization error correction.

SEE OR SEARCH CLASS:
370, Multiplex Communications, subclasses 503+ for synchronization of time multiplex information which may include error detecting techniques.
375, Pulse or Digital Communications, subclass 357 for synchronization failure prevention in pulse or digital communication.

799 ERROR/FAULT DETECTION TECHNIQUE:
This subclass is indented under the class definition. Subject matter in which a specific technique is recited for detecting an error or fault condition.

SEE OR SEARCH THIS CLASS, SUBCLASS:
100+, for reliability and availability, fault recovery, locating, and avoidance in digital data processing systems.
746+, for digital data error correction which include error/fault detection techniques.

800 Parity bit:
This subclass is indented under subclass 799. Subject matter in which a redundant bit is added to a block of data bits.

(1) Note. This redundant bit or parity bit is of a logic state to make the total number of bits having a predetermined logic state within the block odd or even.

801 Parity generator or checker circuit detail:
This subclass is indented under subclass 800. Subject matter which specify the particular elements of a parity signal source or comparator circuit.

802 Even and odd parity:
This subclass is indented under subclass 800. Subject matter wherein the parity scheme in the system includes the generation of parity bits on both an even and odd basis.

803 Parity prediction:
This subclass is indented under subclass 800. Subject matter which calculates an expected parity value prior to execution of an operation and is subsequently compared to the actual parity value to detect an error.

804 Plural dimension parity check:
This subclass is indented under subclass 800. Subject matter in which a single parity bit is derived from data bits taken over each of two or more dimensions, such as horizontal and vertical parity.

805 Storage accessing (e.g., address parity check):
This subclass is indented under subclass 800. Subject matter in which the parity bit is calculated for data bits read into or read out of an information signal storage device. (1) Note. Address parity check arrangements are included in this subclass.

806 Constant-ratio code (m/n):
This subclass is indented under subclass 799. Subject matter in which a code constraint of a constant-ratio between bits of a first logic state and a second logic state is utilized to enable error/fault detection.

807 Check character:
This subclass is indented under subclass 799. Subject matter in which a check character, derived as a predetermined function of a group of data bits, is associated with the group of data bits for error detection purposes.

808 Modulo-n residue check character:
This subclass is indented under subclass 807. Subject matter in which a check character, calculated as the remainder after the value of the digital data is divided by a modulus-n, is associated with the digital data to enable error/fault detection.

SEE OR SEARCH CLASS:
708, Electrical Computers: Arithmetic Processing and Calculating, subclass 532 for residue code checking in arithmetic operations.

809 Code constraint monitored:
This subclass is indented under subclass 799. Subject matter in which the digital data encoding scheme provides inherent constrained conditions which are monitored to enable error/fault detection.

810 Multilevel coding (n>2):
This subclass is indented under subclass 809. Subject matter in which the digital data is encoded in a multilevel or multistate format where the number of levels or states is greater than 2.

SEE OR SEARCH CLASS:
375, Pulse or Digital Communications, subclass 292 for disparity reduction in multilevel digital communications.

811 Forbidden combination or improper condition:
This subclass is indented under subclass 799. Subject matter in which a forbidden combination of digital data or improper condition of a device is monitored to enable error or fault detection.

812 Specified digital signal pattern or pulse count:
This subclass is indented under subclass 811. Subject matter in which the forbidden combination is either a specified pattern of digital data or a count of one or more types of digital pulses.

813 Two key-down detector:
This subclass is indented under subclass 811. Subject matter in which the improper condition is the simultaneous activation of two or more keys on a data input device.

814 Data timing/clocking:
This subclass is indented under subclass 811. Subject matter in which the timing or clocking of digital data is monitored to detect a predetermined forbidden combination or condition.

815 Time delay/interval monitored:
This subclass is indented under subclass 811. Subject matter in which the time delay between events or data is detected to determine a predetermined forbidden condition.

816 Two-rail logic:
This subclass is indented under subclass 811. Subject matter in which both the true and complement state of each logic function is provided and the simultaneous occurrence of both states indicates a forbidden combination.

817 Noise level:
This subclass is indented under subclass 811. Subject matter in which the forbidden condition is the presence of noise exceeding a predetermined level.

818 Missing-bit/drop-out detection:
This subclass is indented under subclass 811. Subject matter in which the improper combination is a missing bit or dropout of a bit within a data character.

SEE OR SEARCH CLASS:
327, Miscellaneous Active Electrical Nonlinear Devices, Circuits, and Systems, subclasses 18+ for missing pulse detecting means.
386, Motion Video Signal Processing for Recording or Reproducing, subclasses 270 through 271 for video drop-out detection and/or correction during recording or reproduction operation.

819 Comparison of data:
This subclass is indented under subclass 799. Subject matter in which an error or fault is detected by the comparison of data.

SEE OR SEARCH THIS CLASS, SUBCLASS:
735, for diagnostic apparatus testing which include error detection by comparison of data.

SEE OR SEARCH CLASS:
340, Communications: Electrical, subclass 146.2 for digital comparator devices, per se.

820 Plural parallel devices or channel:
This subclass is indented under subclass 819. Subject matter in which the data from plural parallel devices or channels is compared to detect an error or fault.

821 Transmission facility:
This subclass is indented under subclass 820. Subject matter which detects an error or fault in a device including a channel of a transmission medium with a device for supplying a digital signal thereto.

822 Sequential repetition:
This subclass is indented under subclass 819. Subject matter in which an error or fault is detected by comparison of repetitive data.

(1) Note. Included herein is majority logic or voter circuitry in which the most frequently occurring data is presumed to be correct.

823 True and complement data:
This subclass is indented under subclass 822. Subject matter in which the data being transferred and compared comprises both the true and complement bit states of the data.

824 Device output compared to input:
This subclass is indented under subclass 819. Subject matter in which the error/fault detection is enabled by comparing the device output with the device input.

SEE OR SEARCH THIS CLASS, SUBCLASS:
735, for diagnostic apparatus testing which includes comparison of the device output with the device input.

E-SUBCLASSES

E-subclasses in USPC Class 714/E11.001-E11.22 were created as duplicates of EPO groups in G06F 11/00 and its indents. With the implementation of CPC, these E-subclasses should no longer be used. Instead, use CPC groups in G06F 11/00 and its indents.

The E-subclasses in U. S. Class 714 provide for processes and apparatus for detecting errors in data-processing including processes and apparatus for monitoring and evaluating data-processing equipment;

processes and apparatus for correcting data-processing errors or for responding to faults in data-processing equipment; and processes and apparatus for avoiding data-processing errors and faults in data-processing equipment.

E11.001 ERROR DETECTION; ERROR CORRECTION; MONITORING :

This main group provides for processes and apparatus for the detection or correction of data-processing errors including the monitoring and evaluation of data-processing equipment. This subclass is substantially the same in scope as ECLA classification G06F11/00.

E11.002 Error detection other than by redundancy in data representation, operation, or hardware, or by checking the order of processing:

This subclass is indented under subclass E11.001. This subclass is substantially the same in scope as ECLA classification G06F11/00B.

E11.003 By time limit, i.e., time-out:

This subclass is indented under subclass E11.002. This subclass is substantially the same in scope as ECLA classification G06F11/00B1.

E11.004 By count or rate limit, e.g., word- or bit count limit, etc.:

This subclass is indented under subclass E11.002. This subclass is substantially the same in scope as ECLA classification G06F11/00B2.

E11.005 By other limits, e.g., analog values, etc. :

This subclass is indented under subclass E11.002. This subclass is substantially the same in scope as ECLA classification G06F11/00B3.

E11.006 By bit configuration check, e.g., of formats or tags, etc.:

This subclass is indented under subclass E11.002. This subclass is substantially the same in scope as ECLA classification G06F11/00B5.

E11.007 Error correction, recovery or fault tolerance using at least two different redundancy techniques and at least one technique not involving redundancy:

This subclass is indented under subclass E11.001. This subclass is substantially the same in scope as ECLA classification G06F11/00C.

E11.008 Fault tolerant software:

This subclass is indented under subclass E11.007. This subclass is substantially the same in scope as ECLA classification G06F11/00C1.

E11.009 In regular structures, i.e., all of the systems nodes have the same number of connections per node:

This subclass is indented under subclass E11.007. This subclass is substantially the same in scope as ECLA classification G06F11/00C4.

SEE OR SEARCH THIS CLASS, SUBCLASS:

E11.074, for redundancy techniques in regular structures involving fault masking by switching in spares.

E11.01 Interconnection networks, i.e., comprising interconnecting link and switching elements:

This subclass is indented under subclass E11.009. This subclass is substantially the same in scope as ECLA classification G06F11/00C4A.

E11.011 Fault-tolerant routing:

This subclass is indented under subclass E11.009. This subclass is substantially the same in scope as ECLA classification G06F11/00C4B.

E11.012 In rings and buses:

This subclass is indented under subclass E11.009. This subclass is substantially the same in scope as ECLA classification G06F11/00C4D.

E11.013 In n-dimensional structures, e.g., arrays, trees, cubes, etc.:

This subclass is indented under subclass E11.009. This subclass is substantially the same in scope as ECLA classification G06F11/00C4C.

E11.014 Neural networks:

This subclass is indented under subclass E11.009. This subclass is substantially the same in scope as ECLA classification G06F11/00C4E.

E11.015 By degradation, i.e., a slow-down occurs but full processing capability is maintained, e.g., discarding a faulty element or unit, etc. :

This subclass is indented under subclass E11.007. This subclass is substantially the same in scope as ECLA classification G06F11/00C2.

E11.016 In systems, e.g., multiprocessors, etc.:

This subclass is indented under subclass E11.007. This subclass is substantially the same in scope as ECLA classification G06F11/00C3.

SEE OR SEARCH THIS CLASS, SUBCLASS:

E11.072, for redundancy techniques in systems involving switching in spares.

E11.017 Security measures, i.e., ensuring safe condition in the event of error, e.g., for controlling element, etc.:

This subclass is indented under subclass E11.001. This subclass is substantially the same in scope as ECLA classification G06F11/00D.

E11.018 Protecting against parasitic influences, e.g., noise, temperature etc.:

This subclass is indented under subclass E11.001. This subclass is substantially the same in scope as ECLA classification G06F11/00F.

E11.019 Identification, e.g., of a performed repair, of a defined circuit, etc.:

This subclass is indented under subclass E11.001. This subclass is substantially the same in scope as ECLA classification G06F11/00K.

E11.02 Reliability or availability analysis:

This subclass is indented under subclass E11.001. This subclass is substantially the same in scope as ECLA classification G06F11/00M.

E11.021 Responding to the occurrence of a fault, e.g., fault tolerance, etc.:

This subclass is indented under subclass E11.001. This subclass is substantially the same in scope as ECLA classification G06F11/07.

E11.022 Error or fault processing without redundancy, i.e., by taking additional measures to deal with the error/fault:

This subclass is indented under subclass E11.021. This subclass is substantially the same in scope as ECLA classification G06F11/07P.

SEE OR SEARCH THIS CLASS, SUBCLASS:

E11.113, for retrying.

E11.023 Error or fault handling:

This subclass is indented under subclass E11.022. This subclass is substantially the same in scope as ECLA classification G06F11/07P10.

E11.024 Error or fault detection or monitoring:

This subclass is indented under subclass E11.022. This subclass is substantially the same in scope as ECLA classification G06F11/07P2.

SEE OR SEARCH THIS CLASS, SUBCLASS:

E11.179, for monitoring per se.

E11.025 Error or fault reporting or logging:

This subclass is indented under subclass E11.022. This subclass is substantially the same in scope as ECLA classification G06F11/07P4.

SEE OR SEARCH THIS CLASS, SUBCLASS:

E11.147, for logging of test results.

E11.026 Error or fault localization:

This subclass is indented under subclass E11.022. This subclass is substantially the same in scope as ECLA classification G06F11/07P6.

E11.027 By collation, i.e., correlating different errors:
This subclass is indented under subclass E11.026. This subclass is substantially the same in scope as ECLA classification G06F11/07P6C.

E11.028 By identifying the faulty software code:
This subclass is indented under subclass E11.026. This subclass is substantially the same in scope as ECLA classification G06F11/07P6S.

E11.029 Error or fault analysis:
This subclass is indented under subclass E11.022. This subclass is substantially the same in scope as ECLA classification G06F11/07P8.

E11.03 Error detection or correction by redundancy in data representation, e.g., by using checking codes, etc.:
This subclass is indented under subclass E11.021. This subclass is substantially the same in scope as ECLA classification G06F11/08

E11.031 Using codes with inherent redundancy, e.g., n-out-of-m codes, etc.:
This subclass is indented under subclass E11.03. This subclass is substantially the same in scope as ECLA classification G06F11/08N.

E11.032 Adding special bits or symbols to the coded information, e.g., parity check, casting out 9"s or 11"s, etc.:
This subclass is indented under subclass E11.03. This subclass is substantially the same in scope as ECLA classification G06F11/10.

E11.033 Using arithmetic codes i.e. codes which are preserved during operation, e.g., modulo 9 or 11 check, etc.:
This subclass is indented under subclass E11.032. This subclass is substantially the same in scope as ECLA classification G06F11/10C.

E11.034 In memories:
This subclass is indented under subclass E11.032. This subclass is substantially the same in scope as ECLA classification G06F11/10M.

E11.035 In static stores:
This subclass is indented under subclass E11.034. This subclass is substantially the same in scope as ECLA classification G06F11/10M2.

E11.036 Integrated on a chip:
This subclass is indented under subclass E11.035. This subclass is substantially the same in scope as ECLA classification G06F11/10M2A.

E11.037 In cache or content addressable memories:
This subclass is indented under subclass E11.036. This subclass is substantially the same in scope as ECLA classification G06F11/10M2A1.

E11.038 In sector programmable memories, e.g., flash disk:
This subclass is indented under subclass E11.036. This subclass is substantially the same in scope as ECLA classification G06F11/10M2A3.

E11.039 In multilevel memories:
This subclass is indented under subclass E11.036. This subclass is substantially the same in scope as ECLA classification G06F11/10M2A5.

E11.04 To protect a block of data words, e.g., CRC, checksum, etc.:
This subclass is indented under subclass E11.035. This subclass is substantially the same in scope as ECLA classification G06F11/10M2B.

E11.041 To protect individual data words written into, or read out of, the addressable memory subsystem of data processing equipment:
This subclass is indented under subclass E11.035. This subclass is substantially the same in scope as ECLA classification G06F11/10M2D.

E11.042 Codes or arrangements adapted for a specific type of error:
This subclass is indented under subclass E11.041. This subclass is substantially the same in scope as ECLA classification G06F11/10M2D1.

E11.043 Error in accessing a memory location, i.e., addressing error:

This subclass is indented under subclass E11.042. This subclass is substantially the same in scope as ECLA classification G06F11/10M2D1A.

E11.044 Error in check bits:

This subclass is indented under subclass E11.042. This subclass is substantially the same in scope as ECLA classification G06F11/10M2D1C.

E11.045 Identification of the type of error:

This subclass is indented under subclass E11.042. This subclass is substantially the same in scope as ECLA classification G06F11/10M2D1D.

E11.046 Adjacent error, e.g., error in n-bit (n>1) wide storage units, i.e., package error, etc.:

This subclass is indented under subclass E11.042. This subclass is substantially the same in scope as ECLA classification G06F11/10M2D1P.

E11.047 Simple parity:

This subclass is indented under subclass E11.042. This subclass is substantially the same in scope as ECLA classification G06F11/10M2D1S.

E11.048 Unidirectional errors:

This subclass is indented under subclass E11.042. This subclass is substantially the same in scope as ECLA classification G06F11/10M2D1U.

E11.049 Arrangements adapted for a specific error detection or correction feature:

This subclass is indented under subclass E11.041. This subclass is substantially the same in scope as ECLA classification G06F11/10M2D3.

E11.05 Bypassing or disabling error detection or correction:

This subclass is indented under subclass E11.049. This subclass is substantially the same in scope as ECLA classification G06F11/10M2D3B.

E11.051 Updating check bits on partial write, i.e., read/modify/write:

This subclass is indented under subclass E11.049. This subclass is substantially the same in scope as ECLA classification G06F11/10M2D3R.

E11.052 Correcting systematically all correctable errors, i.e., scrubbing:

This subclass is indented under subclass E11.049. This subclass is substantially the same in scope as ECLA classification G06F11/10M2D3S.

E11.053 Using single parity bit:

This subclass is indented under subclass E11.032. This subclass is substantially the same in scope as ECLA classification G06F11/10B.

E11.054 Error detection or correction of the data by redundancy in hardware:

This subclass is indented under subclass E11.021. This subclass is substantially the same in scope as ECLA classification G06F11/16.

E11.055 Error detection by comparing the output signals of redundant hardware:

This subclass is indented under subclass E11.054. This subclass is substantially the same in scope as ECLA classification G06F11/16B.

E11.056 In static storage, e.g., matrix, registers, etc.:

This subclass is indented under subclass E11.055. This subclass is substantially the same in scope as ECLA classification G06F11/16B1.

E11.057 In coding, decoding circuits, e.g., parity circuits, etc.:

This subclass is indented under subclass E11.055. This subclass is substantially the same in scope as ECLA classification G06F11/16B10.

E11.058 In communications, e.g., transmission, interfaces, etc.:

This subclass is indented under subclass E11.055. This subclass is substantially the same in scope as ECLA classification G06F11/16B12.

E11.059 Control processors, e.g., for sensors, actuator, etc.:

This subclass is indented under subclass E11.055. This subclass is substantially the same in scope as ECLA classification G06F11/16B14.

SEE OR SEARCH THIS CLASS, SUBCLASS:

E11.081, for similar subject matter using active fault-masking.

E11.06 With exchange of data between units:

This subclass is indented under subclass E11.055. This subclass is substantially the same in scope as ECLA classification G06F11/16B16.

SEE OR SEARCH THIS CLASS, SUBCLASS:

E11.08, for similar subject matter using active fault-masking.

E11.061 With data processors, i.e., data processors compare their computations:

This subclass is indented under subclass E11.055. This subclass is substantially the same in scope as ECLA classification G06F11/16B18.

E11.062 In storage with relative movement between record carrier and transducer, e.g., tapes, disks, etc.:

This subclass is indented under subclass E11.055. This subclass is substantially the same in scope as ECLA classification G06F11/16B2.

E11.063 In systems, i.e., comprising a multiplicity of resources, e.g., cpu with its memory and I/O, etc.:

This subclass is indented under subclass E11.055. This subclass is substantially the same in scope as ECLA classification G06F11/16B20.

E11.064 In arithmetic, logic or counter circuits or a combination thereof, e.g., alu, adder:

This subclass is indented under subclass E11.055. This subclass is substantially the same in scope as ECLA classification G06F11/16B4.

E11.065 In I/O devices or adapters therefor:

This subclass is indented under subclass E11.055. This subclass is substantially the same in scope as ECLA classification G06F11/16B8.

E11.066 Displays:

This subclass is indented under subclass E11.065. This subclass is substantially the same in scope as ECLA classification G06F11/16B8D.

E11.067 Timing and synchronization therein:

This subclass is indented under subclass E11.054. This subclass is substantially the same in scope as ECLA classification G06F11/16S.

SEE OR SEARCH THIS CLASS, SUBCLASS:

E11.07, for similar subject matter using passive fault masking.

E11.068 By using fault tolerant clocks:

This subclass is indented under subclass E11.067. This subclass is substantially the same in scope as ECLA classification G06F11/16S2.

SEE OR SEARCH THIS CLASS, SUBCLASS:

E11.07, for voting schemes.

E11.069 Using passive fault-masking of the redundant circuits, e.g., by quad ding or by majority decision circuits, etc.:

This subclass is indented under subclass E11.054. This subclass is substantially the same in scope as ECLA classification G06F11/18.

E11.07 Synchronization therefor:

This subclass is indented under subclass E11.069. This subclass is substantially the same in scope as ECLA classification G06F11/18S.

E11.071 Using active fault-masking, e.g., by switching out faulty elements or by switching in spare elements, etc.:

This subclass is indented under subclass E11.054. This subclass is substantially the same in scope as ECLA classification G06F11/20.

E11.072 In systems, e.g., multiprocessors, etc.:

This subclass is indented under subclass E11.071. This subclass is substantially the same in scope as ECLA classification G06F11/20D.

E11.073 In distributed systems:

This subclass is indented under subclass E11.072. This subclass is substantially the same in scope as ECLA classification G06F11/20D1.

E11.074 In regular structures:

This subclass is indented under subclass E11.073. This subclass is substantially the same in scope as ECLA classification G06F11/20D1A.

E11.075 Array of processors, e.g., systolic arrays, etc.:

This subclass is indented under subclass E11.074. This subclass is substantially the same in scope as ECLA classification G06F11/20D1A1.

E11.076 Hypercubes:

This subclass is indented under subclass E11.074. This subclass is substantially the same in scope as ECLA classification G06F11/20D1A2.

E11.077 Trees:

This subclass is indented under subclass E11.074. This subclass is substantially the same in scope as ECLA classification G06F11/20D1A3.

E11.078 In interconnections, e.g., rings, etc.:

This subclass is indented under subclass E11.071. This subclass is substantially the same in scope as ECLA classification G06F11/20E.

E11.079 Bus:

This subclass is indented under subclass E11.078. This subclass is substantially the same in scope as ECLA classification G06F11/20E1.

E11.08 Data exchange between units, e.g., for updating backup units, etc.:

This subclass is indented under subclass E11.071. This subclass is substantially the same in scope as ECLA classification G06F11/20F.

SEE OR SEARCH THIS CLASS, SUBCLASS:

E11.113, for retrying.

E11.067, for synchronization between units.

E11.081 For control, e.g., actuators, etc.:

This subclass is indented under subclass E11.071. This subclass is substantially the same in scope as ECLA classification G06F11/20G.

E11.082 In arithmetic units:

This subclass is indented under subclass E11.071. This subclass is substantially the same in scope as ECLA classification G06F11/20H.

E11.083 Redundant power supplies:

This subclass is indented under subclass E11.071. This subclass is substantially the same in scope as ECLA classification G06F11/20K.

E11.084 Masking faults in storage systems using spares and/or by reconfiguring:

This subclass is indented under subclass E11.071. This subclass is substantially the same in scope as ECLA classification G06F11/20L.

E11.085 Removing defective units from operation:

This subclass is indented under subclass E11.084. This subclass is substantially the same in scope as ECLA classification G06F11/20L10.

E11.086 Bypassing defective units on a serial bus:
This subclass is indented under subclass E11.085. This subclass is substantially the same in scope as ECLA classification G06F11/20L10S.

E11.087 With address translations and modifications:
This subclass is indented under subclass E11.084. This subclass is substantially the same in scope as ECLA classification G06F11/20L2.

E11.088 Handling defects in a Redundant Array of Inexpensive Disks (RAID) by remapping:
This subclass is indented under subclass E11.087. This subclass is substantially the same in scope as ECLA classification G06F11/20L2R.

E11.089 Managing spare storage units:
This subclass is indented under subclass E11.084. This subclass is substantially the same in scope as ECLA classification G06F11/20L6.

E11.09 Hot spares:
This subclass is indented under subclass E11.089. This subclass is substantially the same in scope as ECLA classification G06F11/20L6H.

E11.091 Via redundancy in hardware accessing the storage components:
This subclass is indented under subclass E11.084. This subclass is substantially the same in scope as ECLA classification G06F11/20L8.

E11.092 Using redundant I/O processors, storage control units or array controllers:
This subclass is indented under subclass E11.091. This subclass is substantially the same in scope as ECLA classification G06F11/20L8F.

E11.093 With serial buses:
This subclass is indented under subclass E11.092. This subclass is substantially the same in scope as ECLA classification G06F11/20L8F2.

E11.094 To file servers:
This subclass is indented under subclass E11.092. This subclass is substantially the same in scope as ECLA classification G06F11/20L8F4.

E11.095 Connection redundancy between storage system components:
This subclass is indented under subclass E11.091. This subclass is substantially the same in scope as ECLA classification G06F11/20L8C.

E11.096 With serial buses:
This subclass is indented under subclass E11.095. This subclass is substantially the same in scope as ECLA classification G06F11/20L8C2.

E11.097 To file servers:
This subclass is indented under subclass E11.095. This subclass is substantially the same in scope as ECLA classification G06F11/20L8C4.

E11.098 Using the replication of data, e.g., with two or more copies, etc.:
This subclass is indented under subclass E11.084. This subclass is substantially the same in scope as ECLA classification G06F11/20L4.

E11.099 Duplex memories, e.g., twin boot ROMs, etc.:
This subclass is indented under subclass E11.098. This subclass is substantially the same in scope as ECLA classification G06F11/20L4D.

E11.1 Duplexed caches, e.g., cashe paired with nonvolatile storage, etc.:
This subclass is indented under subclass E11.099. This subclass is substantially the same in scope as ECLA classification G06F11/20L4D2.

E11.101 Mirroring, i.e., the concept of maintaining data on two or more units in the same state at all times:
This subclass is indented under subclass E11.098. This subclass is substantially the same in scope as ECLA classification G06F11/20L4M.

SEE OR SEARCH THIS CLASS, SUBCLASS:
E11.118, for backing up data periodically.

E11.102 Resynchronization of failed mirrors:
This subclass is indented under subclass E11.101. This subclass is substantially the same in scope as ECLA classification G06F11/20L4M10.

SEE OR SEARCH THIS CLASS, SUBCLASS:
E11.112, for restoring data from a backup G06F11/14.

E11.103 Mirror management, e.g., pairing of units, etc.:
This subclass is indented under subclass E11.101. This subclass is substantially the same in scope as ECLA classification G06F11/20L4M2.

E11.104 Mirroring on the same storage unit:
This subclass is indented under subclass E11.101. This subclass is substantially the same in scope as ECLA classification G06F11/20L4M4.

E11.105 Mirroring on different storage units with a common controller (RAID 1):
This subclass is indented under subclass E11.101. This subclass is substantially the same in scope as ECLA classification G06F11/20L4M6.

E11.106 Mirroring with multiple controllers:
This subclass is indented under subclass E11.101. This subclass is substantially the same in scope as ECLA classification G06F11/20L4M8.

E11.107 Asynchronous mirroring:
This subclass is indented under subclass E11.106. This subclass is substantially the same in scope as ECLA classification G06F11/20L4M8A.

E11.108 Synchronous mirroring:
This subclass is indented under subclass E11.106. This subclass is substantially the same in scope as ECLA classification G06F11/20L4M8S.

E11.109 De-clustering of replicated data:
This subclass is indented under subclass E11.098. This subclass is substantially the same in scope as ECLA classification G06F11/20L4R.

E11.11 Using more than two copies:
This subclass is indented under subclass E11.098. This subclass is substantially the same in scope as ECLA classification G06F11/20L4S.

E11.111 In Logic Arrays, e.g., programmable or iterative logic arrays, etc.:
This subclass is indented under subclass E11.071. This subclass is substantially the same in scope as ECLA classification G06F11/20P.

E11.112 Error detection or correction of the data by redundancy in operation:
This subclass is indented under subclass E11.021. This subclass is substantially the same in scope as ECLA classification G06F11/14.

E11.113 Saving, restoring, recovering or retrying:
This subclass is indented under subclass E11.112. This subclass is substantially the same in scope as ECLA classification G06F11/14A.

E11.114 At machine instruction level:
This subclass is indented under subclass E11.113. This subclass is substantially the same in scope as ECLA classification G06F11/14A2.

E11.115 Checkpointing the instruction stream:
This subclass is indented under subclass E11.114. This subclass is substantially the same in scope as ECLA classification G06F11/14A2C.

E11.116 For bus or memory accesses:
This subclass is indented under subclass E11.114. This subclass is substantially the same in scope as ECLA classification G06F11/14A2M.

E11.117 Of application data:

This subclass is indented under subclass E11.113. This subclass is substantially the same in scope as ECLA classification G06F11/14A4.

E11.118 Backing up, restoring or mirroring files or drives:

This subclass is indented under subclass E11.117. This subclass is substantially the same in scope as ECLA classification G06F11/14A4B.

E11.119 Backing up, i.e., point-in-time backup:

This subclass is indented under subclass E11.118. This subclass is substantially the same in scope as ECLA classification G06F11/14A4B1.

E11.12 Hardware arrangements for backup:

This subclass is indented under subclass E11.119. This subclass is substantially the same in scope as ECLA classification G06F11/14A4B1H.

E11.121 Backup Management techniques:

This subclass is indented under subclass E11.119. This subclass is substantially the same in scope as ECLA classification G06F11/14A4B1M.

E11.122 Recovery techniques:

This subclass is indented under subclass E11.121. This subclass is substantially the same in scope as ECLA classification G06F11/14A4B1M10.

E11.123 Selection of contents:

This subclass is indented under subclass E11.121. This subclass is substantially the same in scope as ECLA classification G06F11/14A4B1M2.

E11.124 Scheduling policy:

This subclass is indented under subclass E11.121. This subclass is substantially the same in scope as ECLA classification G06F11/14A4B1M4.

E11.125 For networked environments:

This subclass is indented under subclass E11.121. This subclass is substantially the same in scope as ECLA classification G06F11/14A4B1M6.

E11.126 Nondisruptive backup:

This subclass is indented under subclass E11.121. This subclass is substantially the same in scope as ECLA classification G06F11/14A4B1M8.

E11.127 Mirroring:

This subclass is indented under subclass E11.118. This subclass is substantially the same in scope as ECLA classification G06F11/14A4B3.

E11.128 Distributed database systems; Replica control:

This subclass is indented under subclass E11.118. This subclass is substantially the same in scope as ECLA classification G06F11/14A4B5.

E11.129 Synchronization between mobile agents and networked agents:

This subclass is indented under subclass E11.128. This subclass is substantially the same in scope as ECLA classification G06F11/14A4B5M.

E11.13 Using logs or checkpoints:

This subclass is indented under subclass E11.117. This subclass is substantially the same in scope as ECLA classification G06F11/14A4C.

E11.131 In transactions:

This subclass is indented under subclass E11.117. This subclass is substantially the same in scope as ECLA classification G06F11/14A4T.

E11.132 At operating system level:

This subclass is indented under subclass E11.113. This subclass is substantially the same in scope as ECLA classification G06F11/14AB.

E11.133 Boot up procedures:

This subclass is indented under subclass E11.132. This subclass is substantially the same in scope as ECLA classification G06F11/14A8B.

E11.134 Reconfiguring to eliminate the error:

This subclass is indented under subclass E11.132. This subclass is substantially the same in scope as ECLA classification G06F11/14A8C.

E11.135 During software upgrading:

This subclass is indented under subclass E11.132. This subclass is substantially the same in scope as ECLA classification G06F11/14A8E.

E11.136 At file system or disk access level:

This subclass is indented under subclass E11.132. This subclass is substantially the same in scope as ECLA classification G06F11/14A8F.

E11.137 Restarting or rejuvenating:

This subclass is indented under subclass E11.132. This subclass is substantially the same in scope as ECLA classification G06F11/14A8L.

E11.138 Resetting or repowering:

This subclass is indented under subclass E11.132. This subclass is substantially the same in scope as ECLA classification G06F11/14A8P.

E11.139 Cleaning up resources:

This subclass is indented under subclass E11.132. This subclass is substantially the same in scope as ECLA classification G06F11/14A8R.

E11.14 Suspending and resuming a running system:

This subclass is indented under subclass E11.132. This subclass is substantially the same in scope as ECLA classification G06F11/14A8S.

E11.141 Transmit or communication errors:

This subclass is indented under subclass E11.132. This subclass is substantially the same in scope as ECLA classification G06F11/14A8T.

E11.142 Error detection:

This subclass is indented under subclass E11.112. This subclass is substantially the same in scope as ECLA classification G06F11/14B.

E11.143 By time redundancy:

This subclass is indented under subclass E11.142. This subclass is substantially the same in scope as ECLA classification G06F11/14B2.

E11.144 Error avoidance, e.g., error spreading countermeasures, fault avoidance, etc.:

This subclass is indented under subclass E11.001. This subclass is substantially the same in scope as ECLA classification G06F11/00H.

E11.145 Detection or location of defective computer hardware by testing during standby operation or during idle time, e.g., start-up testing, etc.:

This subclass is indented under subclass E11.001. This subclass is substantially the same in scope as ECLA classification G06F11/22.

E11.146 Verification or detection of system hardware configuration:

This subclass is indented under subclass E11.145. This subclass is substantially the same in scope as ECLA classification G06F11/22C.

E11.147 Logging of test results:

This subclass is indented under subclass E11.145. This subclass is substantially the same in scope as ECLA classification G06F11/22L.

E11.148 Test methods:

This subclass is indented under subclass E11.145. This subclass is substantially the same in scope as ECLA classification G06F11/22M.

E11.149 Power-On Test, e.g., POST, etc.:

This subclass is indented under subclass E11.148. This subclass is substantially the same in scope as ECLA classification G06F11/22M1.

E11.15 Configuration test:
This subclass is indented under subclass E11.149. This subclass is substantially the same in scope as ECLA classification G06F11/22M1C.

E11.151 Background testing:
This subclass is indented under subclass E11.148. This subclass is substantially the same in scope as ECLA classification G06F11/22M2.

E11.152 Periodic testing:
This subclass is indented under subclass E11.148. This subclass is substantially the same in scope as ECLA classification G06F11/22M3.

E11.153 Test trigger logic:
This subclass is indented under subclass E11.148. This subclass is substantially the same in scope as ECLA classification G06F11/22M4.

E11.154 Marginal checking:
This subclass is indented under subclass E11.145. This subclass is substantially the same in scope as ECLA classification G06F11/24.

E11.155 Testing of logic operation, e.g., by logic analyzers, etc.:
This subclass is indented under subclass E11.145. This subclass is substantially the same in scope as ECLA classification G06F11/25.

E11.156 Using Fault Dictionaries:
This subclass is indented under subclass E11.155. This subclass is substantially the same in scope as ECLA classification G06F11/25D.

E11.157 Using Expert Systems:
This subclass is indented under subclass E11.155. This subclass is substantially the same in scope as ECLA classification G06F11/25E.

E11.158 Using Neural Networks:
This subclass is indented under subclass E11.155. This subclass is substantially the same in scope as ECLA classification G06F11/25N.

E11.159 Functional testing:
This subclass is indented under subclass E11.145. This subclass is substantially the same in scope as ECLA classification G06F11/26.

E11.16 Reconfiguring circuits for testing, e.g., LSSD, partitioning, etc.:
This subclass is indented under subclass E11.159. This subclass is substantially the same in scope as ECLA classification G06F11/267.

E11.161 Test of buses, lines or interfaces, e.g., stuck-at or open line faults etc.:
This subclass is indented under subclass E11.16. This subclass is substantially the same in scope as ECLA classification G06F11/267B.

E11.162 Test or error correction or detection circuits:
This subclass is indented under subclass E11.16. This subclass is substantially the same in scope as ECLA classification G06F11/267C.

E11.163 Test of input/output devices or peripheral units:
This subclass is indented under subclass E11.16. This subclass is substantially the same in scope as ECLA classification G06F11/267D.

E11.164 Test of ALU:
This subclass is indented under subclass E11.16. This subclass is substantially the same in scope as ECLA classification G06F11/267H.

E11.165 Test of interrupt circuits:
This subclass is indented under subclass E11.16. This subclass is substantially the same in scope as ECLA classification G06F11/267N.

E11.166 Test of CPU or processors:
This subclass is indented under subclass E11.16. This subclass is substantially the same in scope as ECLA classification G06F11/267P.

E11.167 By simulating additional hardware, e.g., fault simulation, etc.:

This subclass is indented under subclass E11.159. This subclass is substantially the same in scope as ECLA classification G06F11/26S.

E11.168 Emulators:

This subclass is indented under subclass E11.167. This subclass is substantially the same in scope as ECLA classification G06F11/26S2.

E11.169 Built-in tests:

This subclass is indented under subclass E11.159. This subclass is substantially the same in scope as ECLA classification G06F11/27.

E11.17 Tester hardware, i.e., output processing circuits:

This subclass is indented under subclass E11.159. This subclass is substantially the same in scope as ECLA classification G06F11/273.

E11.171 Test interface between tester and unit under test:

This subclass is indented under subclass E11.17. This subclass is substantially the same in scope as ECLA classification G06F11/273E.

E11.172 Using a storage for the test inputs, e.g., test-ROM, script files, etc.:

This subclass is indented under subclass E11.17. This subclass is substantially the same in scope as ECLA classification G06F11/273M.

E11.173 Remote test:

This subclass is indented under subclass E11.17. This subclass is substantially the same in scope as ECLA classification G06F11/273R.

E11.174 Using a dedicated service processor for test:

This subclass is indented under subclass E11.17. This subclass is substantially the same in scope as ECLA classification G06F11/273S.

E11.175 With comparison between actual response and known fault-free response, e.g., signature analyzer, etc.:

This subclass is indented under subclass E11.17. This subclass is substantially the same in scope as ECLA classification G06F11/277.

E11.176 In Multi-processor systems, e.g., one processor becoming the test master, etc.:

This subclass is indented under subclass E11.17. This subclass is substantially the same in scope as ECLA classification G06F11/27M.

E11.177 Generation of test inputs, e.g., test vectors, patterns or sequences, etc.:

This subclass is indented under subclass E11.159. This subclass is substantially the same in scope as ECLA classification G06F11/263.

E11.178 By checking the correct order of processing:

This subclass is indented under subclass E11.001. This subclass is substantially the same in scope as ECLA classification G06F11/28.

E11.179 Monitoring:

This subclass is indented under subclass E11.001. This subclass is substantially the same in scope as ECLA classification G06F11/30.

E11.18 With visual or acoustical indication of the functioning of the machine:

This subclass is indented under subclass E11.179. This subclass is substantially the same in scope as ECLA classification G06F11/32.

E11.181 Visualization of programs or trace data:

This subclass is indented under subclass E11.18. This subclass is substantially the same in scope as ECLA classification G06F11/32P.

E11.182 Display for diagnostics, e.g., diagnostic result display, self-test user interface, etc.:

This subclass is indented under subclass E11.18. This subclass is substantially the same in scope as ECLA classification G06F11/32D.

E11.183 Display of waveforms, e.g., of logic analyzers, etc.:

This subclass is indented under subclass E11.182. This subclass is substantially the same in scope as ECLA classification G06F11/32D4.

E11.184 Display of status information:

This subclass is indented under subclass E11.18. This subclass is substantially the same in scope as ECLA classification G06F11/32S.

E11.185 By lamps or LED's:

This subclass is indented under subclass E11.184. This subclass is substantially the same in scope as ECLA classification G06F11/32S2.

E11.186 For error or online/offline status:

This subclass is indented under subclass E11.186. This subclass is substantially the same in scope as ECLA classification G06F11/32S2E.

E11.187 Alarm or error message display:

This subclass is indented under subclass E11.184. This subclass is substantially the same in scope as ECLA classification G06F11/32S4.

E11.188 Computer systems status display:

This subclass is indented under subclass E11.184. This subclass is substantially the same in scope as ECLA classification G06F11/32S6.

E11.189 Recording or statistical evaluation of computer activity, e.g., of down time, of input/output operation, etc.:

This subclass is indented under subclass E11.179. This subclass is substantially the same in scope as ECLA classification G06F11/34.

E11.19 Of interconnections, e.g., interconnecting networks, etc.:

This subclass is indented under subclass E11.189. This subclass is substantially the same in scope as ECLA classification G06F11/34A.

E11.191 Of parallel or distributed programming:

This subclass is indented under subclass E11.189. This subclass is substantially the same in scope as ECLA classification G06F11/34B.

E11.192 Performance measurement:

This subclass is indented under subclass E11.189. This subclass is substantially the same in scope as ECLA classification G06F11/34C.

E11.193 Workload generation, e.g., scripts, playback, etc.:

This subclass is indented under subclass E11.192. This subclass is substantially the same in scope as ECLA classification G06F11/34C2.

E11.194 Benchmarking:

This subclass is indented under subclass E11.193. This subclass is substantially the same in scope as ECLA classification G06F11/34C2B.

E11.195 Time measurement, e.g. response time:

This subclass is indented under subclass E11.192. This subclass is substantially the same in scope as ECLA classification G06F11/34C4.

E11.196 Of active or idle time:

This subclass is indented under subclass E11.195. This subclass is substantially the same in scope as ECLA classification G06F11/34C4A.

E11.197 Performance evaluation by modeling or statistical analysis:

This subclass is indented under subclass E11.189. This subclass is substantially the same in scope as ECLA classification G06F11/34M.

E11.198 Performance evaluation by simulation:

This subclass is indented under subclass E11.189. This subclass is substantially the same in scope as ECLA classification G06F11/34S.

E11.199 Trace driven simulation:

This subclass is indented under subclass E11.198. This subclass is substantially the same in scope as ECLA classification G06F11/34S2.

E11.2 Performance evaluation by tracing or monitoring:

This subclass is indented under subclass E11.189. This subclass is substantially the same in scope as ECLA classification G06F11/34T.

E11.201 For interfaces, buses:

This subclass is indented under subclass E11.2. This subclass is substantially the same in scope as ECLA classification G06F11/34T10.

E11.202 For systems:

This subclass is indented under subclass E11.2. This subclass is substantially the same in scope as ECLA classification G06F11/34T12.

E11.203 Address tracing:

This subclass is indented under subclass E11.2. This subclass is substantially the same in scope as ECLA classification G06F11/34T2.

E11.204 Data logging:

This subclass is indented under subclass E11.2. This subclass is substantially the same in scope as ECLA classification G06F11/34T4.

E11.205 Circuit details, i.e., tracer hardware:

This subclass is indented under subclass E11.2. This subclass is substantially the same in scope as ECLA classification G06F11/34T6.

E11.206 For I/O devices:

This subclass is indented under subclass E11.2. This subclass is substantially the same in scope as ECLA classification G06F11/34T8.

E11.207 Preventing errors by testing or debugging software:

This subclass is indented under subclass E11.001. This subclass is substantially the same in scope as ECLA classification G06F11/36.

E11.208 Software debugging:

This subclass is indented under subclass E11.207. This subclass is substantially the same in scope as ECLA classification G06F11/36D.

E11.209 Compilers or other tools operating on the source text:

This subclass is indented under subclass E11.208. This subclass is substantially the same in scope as ECLA classification G06F11/36D2.

SEE OR SEARCH THIS CLASS, SUBCLASS:

E11.2, for instrumentation for performance monitoring.

E11.21 Debuggers:

This subclass is indented under subclass E11.208. This subclass is substantially the same in scope as ECLA classification G06F11/36D3.

E11.211 Error checking code in the program under test:

This subclass is indented under subclass E11.208. This subclass is substantially the same in scope as ECLA classification G06F11/36D4.

E11.212 Tracing methods or tools:

This subclass is indented under subclass E11.208. This subclass is substantially the same in scope as ECLA classification G06F11/36D5.

SEE OR SEARCH THIS CLASS, SUBCLASS:

E11.2, for performance monitoring.

E11.213 By using additional hardware:

This subclass is indented under subclass E11.208. This subclass is substantially the same in scope as ECLA classification G06F11/36D6.

E11.214 By making modifications to the CPU:

This subclass is indented under subclass E11.213. This subclass is substantially the same in scope as ECLA classification G06F11/36D6C.

E11.215 By monitoring the bus:

This subclass is indented under subclass E11.213. This subclass is substantially the same in scope as ECLA classification G06F11/36D6M.

SEE OR SEARCH THIS CLASS, SUBCLASS:
E11.2, for performance monitoring.

E11.216 By emulating the CPU:

This subclass is indented under subclass E11.213. This subclass is substantially the same in scope as ECLA classification G06F11/36D6E.

SEE OR SEARCH THIS CLASS, SUBCLASS:
E11.168,for testing hardware.

E11.217 User interfaces for testing or debugging software:

This subclass is indented under subclass E11.207. This subclass is substantially the same in scope as ECLA classification G06F11/36G.

SEE OR SEARCH THIS CLASS, SUBCLASS:
E11.18, for hardware monitoring.

E11.218 Methods or tools for writing reliable software and for evaluating software:

This subclass is indented under subclass E11.207. This subclass is substantially the same in scope as ECLA classification G06F11/36M.

SEE OR SEARCH THIS CLASS, SUBCLASS:
E11.008,for fault-tolerant software.

E11.219 Methods or tools to render software testable:

This subclass is indented under subclass E11.218. This subclass is substantially the same in scope as ECLA classification G06F11/36M2.

E11.22 Software metrics:

This subclass is indented under subclass E11.218. This subclass is substantially the same in scope as ECLA classification G06F11/36M3.

FOREIGN ART COLLECTIONS

FOR 100 Scan path testing (LSSD):

Foreign art collections including subject matter in which digital logic is designed for improved test ability by including shift register latches (SRL) to enable the configuring of the circuitry in combinational logic form.

FOR 101 Including test pattern generator:

Foreign art collections including subject matter in which the specific means or method of generating a test pattern for an error checking system is claimed.

FOR 102 Block code:

Foreign art collections including subject matter in which a plurality of information bits are encoded to generate a plurality of check bits as a function of the information bits with the information bits and check bits being associated together to form a block code.

FOR 103 Memory access:

Foreign art collections including subject matter in which digital data being written into or read out of a storage device is encoded in a block code format.

FOR 104 Convolutional code:

Foreign art collections including subject matter in which the information bits are encoded to generate a plurality of check bits, each check bit is generated as a function of a different plurality of information bits and is interspersed among the information bits at predetermined intervals with no natural beginning point or ending point as in block codes.

FOR 288 ERROR/FAULT ANTICIPATION:

Foreign art collection for subject matter in which a signal or circuit parameter is monitored to provide an indication of an imminent error or fault condition prior to its actual occurrence.

FOR 289 Transmission facility or channel:
Foreign art collection for subject matter in which the spare apparatus includes a channel of a transmission medium with a device for supplying digital data thereto.

FOR 290 Memory:
Foreign art collection for subject matter wherein the spare apparatus comprises an information signal storage unit.

FOR 291 Transmission facility:
Foreign art collection for subject matter in which the faulty apparatus is a signal transmission facility.

FOR 292 Data processor or computer:
Foreign art collection for subject matter in which the faulty apparatus includes a device for performing a calculation or arithmetic operation on the data signal.

FOR 293 Programmable processor testing:
Foreign art collection for subject matter in which the diagnostic testing is performed upon a program controlled device for performing a calculation or arithmetic operation on the data signal.

FOR 294 Emulator device:
Foreign art collection for subject matter which tests a system by substituting a microprocessor, to simulate the operation of the system microprocessor to control diagnostic testing of the system.

FOR 295 Watchdog timer (e.g., time-out):
Foreign art collection for subject matter which tests the processor by requiring periodic updating of a time monitoring device within a preset time interval known as a window.

FOR 296 Processor within diverse device (microwave, photocopier):
Foreign art collection for subject matter in which the processor or computer being tested is located within a diverse device (e.g., a microwave oven or photocopier) machine.

FOR 297 Error or fault, logging or tracking:
Foreign art collection for subject matter in which the errors or faults detected are registered or recorded to present a history for diagnostic purposes.

FOR 298 Dedicated maintenance subsystem:
Foreign art collection for subject matter in which the testing is performed under control of a maintenance module or subsystem which independently monitors and performs fault diagnosis of a programmable digital computer.

FOR 299 Testing of external device by programmable digital computer:
Foreign art collection for subject matter in which a programmable digital computer controls the testing of a device external to the computer.

FOR 300 ERROR DETECTION FOR SYNCHRONIZATION CONTROL:
Foreign art collection for subject matter in which error detecting techniques are utilized to detect an out-of-sync condition or to control synchronization between devices.

FOR 306 Of network (714/4):
This foreign art collection is indented under unnumbered placeholder 714/3. Foreign art collection further including means or steps for recovery at a network level (e.g., recovery from nodal failures).

FOR 307 Of memory or peripheral subsystem (714/5):
This foreign art collection is indented unnumbered placeholder 714/3. Foreign art collection further including means or steps for recovery from a fault of a memory function level or the peripheral function level, or for recovery limited to a specialized processor accessing either memory, peripheral, or other I/O device.

(1) Note. “Page faults” are a species of faults peculiar to memory accessing and are classified elsewhere.

FOR 308 Redundant stored data accessed (e.g., duplicated data, error correction coded data, or other parity-type data) (714/6):
This foreign art collection is indented under FOR 307. Foreign art collection further

including means or steps for recovery by accessing redundant stored data.

(1) Note. This and indented subclasses rely on information which is a function of the actual data of concern as exemplified in one simple form by parity data. The species of fault recovery or avoidance concerned with storing archival verbatim copies of data is classified elsewhere.

(2) Note. Parity and error-correction coded storage of general utility in a system without data processing features claimed are classified elsewhere in this class.

FOR 309 Reconfiguration (e.g., adding a replacement storage component) (714/7):
This foreign art collection is indented under FOR 308. Foreign art collection further including means or steps for statically replacing a failed memory component.

(1) Note. Classification here requires more than selecting a correct output from a concurrently active redundant functional unit in place of the output of the failed component.

FOR 310 Isolating failed storage location (e.g., sector remapping) (714/8):
This foreign art collection is indented under FOR 307. Foreign art collection further including means or steps for recovery by disabling access to a failed memory location.

(1) Note. Classification here requires more than selecting a correct output from a concurrently active redundant functional unit in place of the output of the failed component.

FOR 311 Access processor affected (e.g., I/O processor, MMU, DMA processor) (714/9):
This foreign art collection is indented under FOR 307. Foreign art collection further including means or steps for recovery from fault of an access processor (e.g., memory management unit (MMU), direct memory access (DMA) processor, I/O processor, etc.).

FOR 312 Of computer software (714/38):
This foreign art collection is indented unnumbered placeholder 714/37. Subject matter further including means or steps for locating a fault in software or testing software.

(1) Note. This subclass also provides for detecting an error in instruction data in combination with a digital data processing system. Generic coded information error detection is classified elsewhere.

(2) Note. This subclass also provides for fault locating in software analysis by mechanisms such as debugging, automatic code generating, object oriented design, etc.

FOR 313 Performance monitoring for fault avoidance (714/47):
This foreign art collection is indented unnumbered placeholder 714/1. Foreign art collection further including means or steps for monitoring event duration and event counts for anticipating or recognizing faults.

(1) Note. This subclass relates to the fault avoidance species of reliability.

(2) Note. This subclass includes event duration and counting arrangements for statistical analysis of system operations and predictive methods of fault avoidance.

END