HAVING BIOMATERIAL COMPONENT OR INTEGRATED WITH LIVING ORGANISM

HAVING SUPERCONDUCTIVE COMPONENT

HAVING MAGNETIC OR FERROELECTRIC COMPONENT

REPAIR OR RESTORATION

INCLUDING CONTROL RESPONSIVE TO SENSED CONDITION

.Interconnecting plural devices on semiconductor substrate

.Optical characteristic sensed

...Chemical etching

.Electrical characteristic sensed

..Utilizing integral test element

..And removal of defect

..Altering electrical property by material removal

WITH MEASURING OR TESTING

-Packaging (e.g., with mounting, encapsulating, etc.) or treatment of packaged semiconductor

.Optical characteristic sensed

.Electrical characteristic sensed

..Utilizing integral test element

HAVING INTEGRAL POWER SOURCE (E.G., BATTERY, ETC.)

ELECTRON EMITTER MANUFACTURE

MANUFACTURE OF ELECTRICAL DEVICE CONTROLLED PRINthead

MAKING DEVICE OR CIRCUIT EMISSIVE OF NONELECTRICAL SIGNAL

.Having diverse electrical device

..Including device responsive to nonelectrical signal

...Packaging (e.g., with mounting, encapsulating, etc.) or treatment of packaged semiconductor

.Having additional optical element (e.g., optical fiber, etc.)

..Plural emissive devices

.Including integrally formed optical element (e.g., reflective layer, luminescent material, contoured surface, etc.)

..Liquid crystal component

..Optical waveguide structure

..Optical grating structure

.Substrate dicing

..Making emissive array

..Multiple wavelength emissive

.Ordered or disordered

.Graded composition

.Passivating of surface

.Mesa formation

..Tapered etching

..With epitaxial deposition of semiconductor adjacent mesa

.Groove formation

..Tapered etching

..With epitaxial deposition of semiconductor in groove

.Dopant introduction into semiconductor region

.Compound semiconductor

..Heterojunction

MAKING DEVICE OR CIRCUIT RESPONSIVE TO NONELECTRICAL SIGNAL

.Chemically responsive

.Physical stress responsive

..Packaging (e.g., with mounting, encapsulating, etc.) or treatment of packaged semiconductor

.Having cantilever element

.Having diaphragm element

.Thermally responsive

..Packaging (e.g., with mounting, encapsulating, etc.) or treatment of packaged semiconductor

.Responsive to corpuscular radiation (e.g., nuclear particle detector, etc.)

.Responsive to electromagnetic radiation

..Gettering of substrate

..Having diverse electrical device

...Charge transfer device (e.g., CCD, etc.)

..Continuous processing

...Using running length substrate

..Particulate semiconductor component
CLASS 438 SEMICONDUCTOR DEVICE MANUFACTURING: PROCESS

Packaging (e.g., with mounting, encapsulating, etc.) or treatment of packaged semiconductor

Having additional optical element (e.g., optical fiber, etc.)

Plural responsive devices (e.g., array, etc.)

Assembly of plural semiconductor substrates

Including integrally formed optical element (e.g., reflective layer, luminescent layer, etc.)

Color filter

Specific surface topography (e.g., textured surface, etc.)

Having reflective or antireflective component

Making electromagnetic responsive array

Vertically arranged (e.g., tandem, stacked, etc.)

Charge transfer device (e.g., CCD, etc.)

Majority signal carrier (e.g., buried or bulk channel, peristaltic, etc.)

Compound semiconductor

Having structure to improve output signal (e.g., exposure control structure, etc.)

Having blooming suppression structure (e.g., antiblooming drain, etc.)

Lateral series connected array

Specified shape junction barrier (e.g., V-grooved junction, etc.)

Having organic semiconductor component

Forming point contact

Having selenium or tellurium elemental semiconductor component

Having metal oxide or copper sulfide compound semiconductor component

And cadmium sulfide compound semiconductor component

Graded composition

Direct application of electric current

Fusion or solidification of semiconductor region

Including storage of electrical charge in substrate

Avalanche diode

Schottky barrier junction

Compound semiconductor

Heterojunction

Chalcogen (i.e., oxygen (O), sulfur (S), selenium (Se), tellurium (Te)) containing

Amorphous semiconductor

Polycrystalline semiconductor

Contact formation (i.e., metallization)

HAVING ORGANIC SEMICONDUCTIVE COMPONENT

MAKING POINT CONTACT DEVICE

Direct application of electrical current

HAVING SelenIUM OR TELLURIUM ELEMENTAL SEMICONDUCTOR COMPONENT

Direct application of electrical current

HAVING METAL OXIDE OR COPPER SULFIDE COMPOUND SEMICONDUCTOR COMPONENT

HAVING DIAMOND SEMICONDUCTOR COMPONENT

PACKAGING (E.G., WITH MOUNTING, ENCAPSULATING, ETC.) OR TREATMENT OF PACKAGED SEMICONDUCTOR

Assembly of plural semiconductive substrates each possessing electrical device

Flip-chip-type assembly

Stacked array (e.g., rectifier, etc.)

Using strip lead frame

And encapsulating

Substrate dicing

Utilizing a coating to perfect the dicing

Including contaminant removal or mitigation

Having light transmissive window

Incorporating resilient component (e.g., spring, etc.)

Including adhesive bonding step
..Electrically conductive adhesive
120 .With vibration step
121 .Metallic housing or support
122 ..Possessing thermal dissipation structure (i.e., heat sink)
123 ..Lead frame
124 ..And encapsulating
125 .Insulative housing or support
126 ..And encapsulating
127 .Encapsulating
128 MAKING DEVICE ARRAY AND SELECTIVELY INTERCONNECTING
129 .With electrical circuit layout
130 .Rendering selected devices operable or inoperable
131 .Using structure alterable to conductive state (i.e., antifuse)
132 .Using structure alterable to nonconductive state (i.e., fuse)
133 MAKING REGENERATIVE-TYPE SWITCHING DEVICE (E.G., SCR, IGBT, THYRISTOR, ETC.)
134 .Bidirectional rectifier with control electrode (e.g., triac, diac, etc.)
135 .Having field effect structure
136 ..Junction gate
137 ...Vertical channel
138 ..Vertical channel
139 .Altering electrical characteristic
140 .Having structure increasing breakdown voltage (e.g., guard ring, field plate, etc.)
141 MAKING CONDUCTIVITY MODULATION DEVICE (E.G., UNIJUNCTION TRANSISTOR, DOUBLE BASE DIODE, CONDUCTIVITY-MODULATED TRANSISTOR, ETC.)
142 MAKING FIELD EFFECT DEVICE HAVING PAIR OF ACTIVE REGIONS SEPARATED BY GATE STRUCTURE BY FORMATION OR ALTERATION OF SEMICONDUCTIVE ACTIVE REGIONS
143 .Gettering of semiconductor substrate
144 .Charge transfer device (e.g., CCD, etc.)
145 ..Having additional electrical device
146 .Majority signal carrier (e.g., buried or bulk channel, peristaltic, etc.)
147 ...Changing width or direction of channel (e.g., meandering channel, etc.)
148 ...Substantially incomplete signal charge transfer (e.g., bucket brigade, etc.)
149 .On insulating substrate or layer (e.g., TFT, etc.)
150 ...Specified crystallographic orientation
151 ...Having insulated gate
152 ...Combined with electrical device not on insulating substrate or layer
153 ...Complementary field effect transistors
154 ...Complementary field effect transistors
155 ...And additional electrical device on insulating substrate or layer
156 ...Vertical channel
157 ...Plural gate electrodes (e.g., dual gate, etc.)
158 ...Inverted transistor structure
159 ...Source-to-gate or drain-to-gate overlap
160 ...Utilizing backside irradiation
161 ...Including source or drain electrode formation prior to semiconductor layer formation (i.e., staggered electrodes)
162 ...Introduction of nondopant into semiconductor layer
163 ...Adjusting channel dimension (e.g., providing lightly doped source or drain region, etc.)
164 ...Semiconductor islands formed upon insulating substrate or layer (e.g., mesa formation, etc.)
165 ...Including differential oxidation
166 ...Including recrystallization step
167 .Having Schottky gate (e.g., MESFET, HEMT, etc.)
168 ...Specified crystallographic orientation
169 ...Complementary Schottky gate field effect transistors
..And bipolar device
..And passive electrical device (e.g., resistor, capacitor, etc.)
..Having heterojunction (e.g., HEMT, MODFET, etc.)
..Vertical channel
..Doping of semiconductive channel region beneath gate (e.g., threshold voltage adjustment, etc.)
..Buried channel
..Plural gate electrodes (e.g., dual gate, etc.)
..Closed or loop gate
..Elemental semiconductor
..Asymmetric
..Self-aligned
..Doping of semiconductive region
....T-gate
....Dummy gate
....Utilizing gate sidewall structure
.....Multiple doping steps
..Having junction gate (e.g., JFET, SIT, etc.)
..Specified crystallographic orientation
..Complementary junction gate field effect transistors
..And bipolar transistor
..And passive device (e.g., resistor, capacitor, etc.)
..Having heterojunction
..Vertical channel
..Multiple parallel current paths (e.g., grid gate, etc.)
..Doping of semiconductive channel region beneath gate (e.g., threshold voltage adjustment, etc.)
..Plural gate electrodes
..Including isolation structure
..Having insulated gate (e.g., IGFET, MISFET, MOSFET, etc.)
..Specified crystallographic orientation
..Complementary insulated gate field effect transistors (i.e., CMOS)
..And additional electrical device

....Including insulated gate field effect transistor having gate surrounded by dielectric (i.e., floating gate)
....Including bipolar transistor (i.e., BiCMOS)
.....Complementary bipolar transistors
.....Lateral bipolar transistor
.....Plural bipolar transistors of differing electrical characteristics
.....Vertical channel insulated gate field effect transistor
.....Including isolation structure
......Isolation by PN junction only
.....Including additional vertical channel insulated gate field effect transistor
.....Including passive device (e.g., resistor, capacitor, etc.)
...Having gate surrounded by dielectric (i.e., floating gate)
....Vertical channel
....Common active region
....Having underpass or crossunder
....Having fuse or integral short
....Gate insulator structure constructed of diverse dielectrics (e.g., MNOS, etc.) or of nonsilicon compound
....Doping of semiconductor channel region beneath gate insulator (e.g., threshold voltage adjustment, etc.)
....Including isolation structure
....Total dielectric isolation
....Isolation by PN junction only
....Dielectric isolation formed by grooving and refilling with dielectric material
.....With epitaxial semiconductor layer formation
.....Having well structure of opposite conductivity type
......Plural wells
....Recessed oxide formed by localized oxidation (i.e., LOCOS)
.....With epitaxial semiconductor layer formation


Having well structure of opposite conductivity type

Plural wells

Self-aligned

Utilizing gate sidewall structure

Plural doping steps

Plural doping steps

And contact formation

Including bipolar transistor (i.e., BiMOS)

Heterojunction bipolar transistor

Lateral bipolar transistor

Including diode

Including passive device (e.g., resistor, capacitor, etc.)

Capacitor

Having high dielectric constant insulator (e.g., Ta2O5, etc.)

And additional field effect transistor (e.g., sense or access transistor, etc.)

Including transistor formed on trench sidewalls

Trench capacitor

Utilizing stacked capacitor structure (e.g., stacked trench, buried stacked capacitor, etc.)

With epitaxial layer formed over the trench

Including doping of trench surfaces

Multiple doping steps

Including isolation means formed in trench

Doping by outdiffusion from a dopant source layer (e.g., doped oxide, etc.)

Planar capacitor

Including doping of semiconductive region

Multiple doping steps

Stacked capacitor

Including selectively removing material to undercut and expose storage node layer

Including texturizing storage node layer

Contacts formed by selective growth or deposition

Having additional gate electrode surrounded by dielectric (i.e., floating gate)

Including additional field effect transistor (e.g., sense or access transistor, etc.)

Including forming gate electrode in trench or recess in substrate

Textured surface of gate insulator or gate electrode

Multiple interelectrode dielectrics or nonsilicon compound gate insulator

Including elongated source or drain region disposed under thick oxide regions (e.g., buried or diffused bitline, etc.)

Tunneling insulator

Tunneling insulator

Oxidizing sidewall of gate electrode

Having additional, nonmemory control electrode or channel portion (e.g., for accessing field effect transistor structure, etc.)

Including forming gate electrode as conductive sidewall spacer to another electrode

Vertical channel

Utilizing epitaxial semiconductor layer grown through an opening in an insulating layer

Gate electrode in trench or recess in semiconductor substrate

V-gate

Totally embedded in semiconductive layers

Having integral short of source and base regions

Short formed in recess in substrate

Making plural insulated gate field effect transistors of differing electrical characteristics

Introducing a dopant into the channel region of selected transistors
...Including forming overlapping gate electrodes
...After formation of source or drain regions and gate electrode (e.g., late programming, encoding, etc.)
...Making plural insulated gate field effect transistors having common active region
...Having underpass or crossunder
...Having fuse or integral short
...Buried channel
...Plural gate electrodes (e.g., dual gate, etc.)
...Closed or loop gate
...Utilizing compound semiconductor
...Asymmetric
...Gate insulator structure constructed of diverse dielectrics (e.g., MNOS, etc.) or of nonsilicon compound
...Having step of storing electrical charge in gate dielectric
...Doping of semiconductive channel region beneath gate insulator (e.g., adjusting threshold voltage, etc.)
...After formation of source or drain regions and gate electrode
...Using channel conductivity dopant of opposite type as that of source and drain
...Direct application of electrical current
...Fusion or solidification of semiconductor region
...Including isolation structure
...Total dielectric isolation
...Dielectric isolation formed by grooving and refilling with dielectric material
...Recessed oxide formed by localized oxidation (i.e., LOCOS)
...Doping region beneath recessed oxide (e.g., to form chanstop, etc.)
...Self-aligned
...Having elevated source or drain (e.g., epitaxially formed source or drain, etc.)
...Source or drain doping

...Oblique implantation
...Utilizing gate sidewall structure
...Conductive sidewall component
...Plural doping steps
...Plural doping steps
...Using same conductivity-type dopant
...Radiation or energy treatment modifying properties of semiconductor regions of substrate (e.g., thermal, corpuscular, electromagnetic, etc.)

FORMING BIPOLAR TRANSISTOR BY FORMATION OR ALTERATION OF SEMICONDUCTIVE ACTIVE REGIONS

.Gettering of semiconductor substrate
...On insulating substrate or layer (i.e., SOI type)
...Having heterojunction
...Complementary bipolar transistors
...And additional bipolar device
...Forming inverted transistor structure
...Forming lateral transistor structure
...Wide bandgap emitter
...Including isolation structure
...Air isolation (e.g., mesa, etc.)
...Self-aligned
...Utilizing dummy emitter
...Complementary bipolar transistors
...Having common active region (i.e., integrated injection logic (I2L), etc.)
...Including additional electrical device
...Having lateral bipolar transistor
...Including additional electrical device
...Having lateral bipolar transistor
...Including diode
...Including passive device (e.g., resistor, capacitor, etc.)
...Resistor
Having same doping as emitter or collector

Lightly doped junction isolated resistor

Having fuse or integral short

Forming inverted transistor structure

Forming lateral transistor structure

Combined with vertical bipolar transistor

Active region formed along groove or exposed edge in semiconductor

Having multiple emitter or collector structure

Self-aligned

Making plural bipolar transistors of differing electrical characteristics

Using epitaxial lateral overgrowth

Having multiple emitter or collector structure

Mesa or stacked emitter

Washed emitter

Walled emitter

Emitter dip prevention or utilization

Permeable or metal base

Sidewall base contact

Pedestal base

Forming base region of specified dopant concentration profile (e.g., inactive base region more heavily doped than active base region, etc.)

Including isolation structure

Having semi-insulative region

Total dielectric isolation

Isolation by PN junction only

Including epitaxial semiconductor layer formation

Up diffusion of dopant from substrate into epitaxial layer

Dielectric isolation formed by grooving and refilling with dielectrical material

With epitaxial semiconductor formation in groove

Including deposition of polysilicon or noninsulative material into groove

Recessed oxide by localized oxidation (i.e., LOCOS)

With epitaxial semiconductor layer formation

Self-aligned

Forming active region from adjacent doped polycrystalline or amorphous semiconductor

Having sidewall

Including conductive component

Simultaneously outdiffusing plural dopants from polysilicon or amorphous semiconductor

Dopant implantation or diffusion

Forming buried region (e.g., implanting through insulating layer, etc.)

Simultaneous introduction of plural dopants

Plural doping steps

Multiple ion implantation steps

Using same conductivity-type dopant

Forming partially overlapping regions

Single dopant forming regions of different depth or concentrations

Through same mask opening

Radiation or energy treatment modifying properties of semiconductor regions of substrate (e.g., thermal, corpuscular, electromagnetic, etc.)

VOLTAGE VARIABLE CAPACITANCE DEVICE MANUFACTURE (E.G., VARACTOR, ETC.)

AVALANCHE DIODE MANUFACTURE (E.G., IMPATT, TRAPPAT, ETC.)

MAKING PASSIVE DEVICE (E.G., RESISTOR, CAPACITOR, ETC.)

Resistor

Lightly doped junction isolated resistor

Deposited thin film resistor

Altering resistivity of conductor
CLASS 438 SEMICONDUCTOR DEVICE MANUFACTURING: PROCESS

386 . Trench capacitor
387 ... Having stacked capacitor
388 ... structure (e.g., stacked
389 ... trench, buried stacked
390 ... capacitor, etc.)
391 ... With epitaxial layer formed
392 ... over the trench
393 ... Including doping of trench
394 ... surfaces
395 ... Multiple doping steps
396 ... Including isolation means
397 ... formed in trench
398 ... Doping by outdiffusion from a
dopant source layer (e.g.,
doped oxide)
399 ... Planar capacitor
400 ... Including doping of
401 ... semiconductive region
402 ... Multiple doping steps
403 ... Stacked capacitor
404 ... Including selectively removing
405 ... material to undercut and
406 ... expose storage node layer
407 ... Including texturizing storage
408 ... node layer
409 ... Having contacts formed by
410 ... selective growth or deposition
411 ... Formation of electrically
412 ... isolated lateral
413 ... semiconductive structure
414 ... Having substrate registration
415 ... feature (e.g., alignment mark)
416 ... And getting of substrate
417 ... Having semi-insulating component
418 ... Total dielectric isolation
419 ... And separate partially isolated
420 ... semiconductor regions
421 ... Bonding of plural
422 ... semiconductive substrates
423 ... Nondopant implantation
424 ... With electrolytic treatment
425 ... step
426 ... Porous semiconductor formation
427 ... Encroachment of separate
428 ... locally oxidized regions
429 ... Air isolation (e.g., beam lead
430 ... supported semiconductor
431 ... islands, etc.)
432 ... Semiconductor islands formed
433 ... upon insulating substrate or
434 ... layer (e.g., mesa isolation,
etc.)
435 ... With epitaxial semiconductor
436 ... formation
437 ... Isolation by PN junction only
438 ... Thermomigration
439 ... With epitaxial semiconductor
440 ... formation
441 ... And simultaneous
442 ... polycrystalline growth
443 ... Dopant addition
444 ... Plural doping steps
445 ... Having air-gap dielectric (e.g.,
groove, etc.)
446 ... Enclosed cavity
447 ... Implanted to form insulator
448 ... Grooved and refilled with
deposited dielectric material
449 ... Combined with formation of
recessed oxide by localized
oxidation
450 ... Recessed oxide laterally
extending from groove
451 ... Refilling multiple grooves of
different widths or depths
452 ... Reflow of insulator
453 ... And epitaxial semiconductor
454 ... formation in groove
455 ... And deposition of polysilicon
456 ... or noninsulative material into
groove
457 ... Oxidation of deposited
458 ... material
459 ... Nonoxidized portions
460 ... remaining in groove after
oxidation
461 ... Dopant addition
462 ... From doped insulator in groove
463 ... Multiple insulative layers in
groove
464 ... Reflow of insulator
465 ... Conformal insulator formation
466 ... Reflow of insulator
467 ... Recessed oxide by localized
468 ... oxidation (i.e., LOCOS)
469 ... Including nondopant
implantation
470 ... With electrolytic treatment
step
471 ... With epitaxial semiconductor
layer formation
472 ... Etchback of recessed oxide
473 ... Preliminary etching of groove
474 ... Masking of groove sidewall
475 ... Polysilicon containing
sidewall
476 ... Dopant addition
477 ... Utilizing oxidation mask having
polysilicon component

April 2011
Dopant addition
...Implanting through recessed oxide
...Plural doping steps
...Plural oxidation steps to form recessed oxide
...And electrical conductor formation (i.e., metallization)
.Field plate electrode

BONDING OF PLURAL SEMICONDUCTOR SUBSTRATES
.Having enclosed cavity
.Warping of semiconductor substrate
.Subsequent separation into plural bodies (e.g., delaminating, dicing, etc.)
.Thinning of semiconductor substrate

SEMICONDUCTOR SUBSTRATE DICING
.Beam lead formation
.Having specified scribe region structure (e.g., alignment mark, plural grooves, etc.)
.By electromagnetic irradiation (e.g., electron, laser, etc.)
.With attachment to temporary support or carrier
.Having a perfecting coating

DIRECT APPLICATION OF ELECTRICAL CURRENT
.To alter conductivity of fuse or antifuse element
.Emmigration
.Utilizing pulsed current
.Fusion of semiconductor region

GETTERING OF SUBSTRATE
.By vibrating or impacting
.By implanting or irradiating
.Ionized radiation (e.g., corpuscular or plasma treatment, etc.)
.Hydrogen plasma (i.e., hydrogenization)
.By layers which are coated, contacted, or diffused
.By vapor phase surface reaction

FORMATION OF SEMICONDUCTIVE ACTIVE REGION ON ANY SUBSTRATE (E.G., FLUID GROWTH, DEPOSITION)
.On insulating substrate or layer

Including implantation of ion which reacts with semiconductor substrate to form insulating layer
.Using epitaxial lateral overgrowth
.Amorphous semiconductor
.Compound semiconductor
.Running length (e.g., sheet, strip, etc.)
.Deposition utilizing plasma (e.g., glow discharge, etc.)
.And subsequent crystallization
.Using wave energy (e.g., laser, electron beam, etc.)
.Polycrystalline semiconductor
.Simultaneous single crystal formation
.Running length (e.g., sheet, strip, etc.)
.And subsequent doping of polycrystalline semiconductor
.Fluid growth step with preceding and subsequent diverse operation
.Plural fluid growth steps with intervening diverse operation
.Differential etching
.Doping of semiconductor
.Coating of semiconductive substrate with nonsemiconductive material
.Fluid growth from liquid combined with preceding diverse operation
.Differential etching
.Doping of semiconductor
.Heat treatment
.Fluid growth from gaseous state combined with preceding diverse operation
.Differential etching
.Doping of semiconductor
...Ion implantation
.Fluid growth from gaseous state combined with subsequent diverse operation
.Doping of semiconductor
.Heat treatment
510 INTRODUCTION OF CONDUCTIVITY MODIFYING DOPANT INTO SEMICONDUCTIVE MATERIAL

511 • Ordering or disordering
512 • Involving nuclear transmutation doping
513 • Plasma (e.g., glow discharge, etc.)
514 • Ion implantation of dopant into semiconductor region
515 • Ionized molecules
516 • Including charge neutralization
517 • Of semiconductor layer on insulating substrate or layer
518 • Of compound semiconductor
519 • Including multiple implantation steps
520 • Providing nondopant ion (e.g., proton, etc.)
521 • Using same conductivity-type dopant
522 • Including heat treatment
523 • And contact formation (i.e., metallization)
524 • Into grooved semiconductor substrate region
525 • Using oblique beam
526 • Forming buried region
527 • Including multiple implantation steps
528 • Providing nondopant ion (e.g., proton, etc.)
529 • Using same conductivity-type dopant
530 • Including heat treatment
531 • Using shadow mask
532 • Into polycrystalline region
533 • And contact formation (i.e., metallization)
534 • Rectifying contact (i.e., Schottky contact)
535 • By application of corpuscular or electromagnetic radiation (e.g., electron, laser, etc.)
536 • Recoil implantation
537 • Fusing dopant with substrate (i.e., alloy junction)
538 • Using additional material to improve wettability or flow characteristics (e.g., flux, etc.)
539 • Application of pressure to material during fusion

438 - 10 CLASS 438 SEMICONDUCTOR DEVICE MANUFACTURING: PROCESS

540 • Including plural controlled heating or cooling steps or nonuniform heating
541 • Including diffusion after fusing step
542 • Diffusing a dopant
543 • To control carrier lifetime (i.e., deep level dopant)
544 • To solid-state solubility concentration
545 • Forming partially overlapping regions
546 • Plural dopants in same region (e.g., through same mask opening, etc.)
547 • Simultaneously
548 • Plural dopants simultaneously in plural regions
549 • Single dopant forming plural diverse regions (e.g., forming regions of different concentrations or of different depths, etc.)
550 • Nonuniform heating
551 • Using multiple layered mask
552 • Having plural predetermined openings in master mask
553 • Using metal mask
554 • Outwardly
555 • Laterally under mask opening
556 • Edge diffusion by using edge portion of structure other than masking layer to mask
557 • From melt
558 • From solid dopant source in contact with semiconductor region
559 • Using capping layer over dopant source to prevent out-diffusion of dopant
560 • Plural diffusion stages
561 • Dopant source within trench or groove
562 • Organic source
563 • Glassy source or doped oxide
564 • Polycrystalline semiconductor source
565 • From vapor phase
566 • Plural diffusion stages
567 • Solid source in operative relation with semiconductor region
568 • In capsule-type enclosure
569 • Into compound semiconductor region
FORMING SCHOTTKY JUNCTION (I.E., SEMICONDUCTOR-CONDUCTOR RECTIFYING JUNCTION CONTACT)

Combined with formation of ohmic contact to semiconductor region

Compound semiconductor

Multilayer electrode

...T-shaped electrode

...Using platinum group metal (i.e., platinum (Pt), palladium (Pd), rhodium (Rh), ruthenium (Ru), iridium (Ir), osmium (Os), or alloy thereof)

...Into grooved or recessed semiconductor region

...Utilizing lift-off

...Forming electrode of specified shape (e.g., slanted, etc.)

....T-shaped electrode

...Using platinum group metal (i.e., platinum (Pt), palladium (Pd), rhodium (Rh), ruthenium (Ru), iridium (Ir), osmium (Os), or alloy thereof)

...Silicide

...Using refractory group metal (i.e., titanium (Ti), zirconium (Zr), hafnium (Hf), vanadium (V), niobium (Nb), tantalum (Ta), chromium (Cr), molybdenum (Mo), tungsten (W), or alloy thereof)

...Silicide

COATING WITH ELECTRICALLY OR THERMALLY CONDUCTIVE MATERIAL

.Insulated gate formation

Combined with formation of ohmic contact to semiconductor region

...Forming array of gate electrodes

...Plural gate levels

...Recessed into semiconductor substrate

...Compound semiconductor

...Gate insulator structure constructed of plural layers or nonsilicon containing compound

...Possessing plural conductive layers (e.g., polycide)

...Separated by insulator (i.e., floating gate)

....Tunnelling dielectric layer
Separating insulating layer
is laminate or composite of plural insulating materials

At least one metallization level formed of diverse conductive layers

Planarization

At least one layer forms a diffusion barrier

Having adhesion promoting layer

Diverse conductive layers limited to viahole/plug

Silicide formation

Having planarization step

Utilizing reflow

Simultaneously by chemical and mechanical means

Utilizing etch-stop layer

Insulator formed by reaction with conductor (e.g., oxidation, etc.)

Including use of antireflective layer

With formation of opening (i.e., viahole) in insulative layer

Having viaholes of diverse width

Having viahole with sidewall component

Having viahole of tapered shape

Selective deposition

Diverse conductors

At least one layer forms a diffusion barrier

Having adhesion promoting layer

Having planarization step

Utilizing reflow

Having electrically conductive polysilicon component

Altering composition of conductor

Implantation of ion into conductor

Including heat treatment of conductive layer

Subsequent fusing conductive layer

Utilizing laser

Rapid thermal anneal

Forming silicide

Utilizing textured surface

Specified configuration of electrode or contact

Conductive feedthrough or through-hole in substrate

Specified aspect ratio of conductor or viahole

And patterning of conductive layer

Utilizing lift-off

Utilizing multilayered mask

Plug formation (i.e., in viahole)

Tapered etching

Selective deposition of conductive layer

Plug formation (i.e., in viahole)

Utilizing electromagnetic or wave energy
...Pretreatment of surface to enhance or retard deposition

Electroless deposition of conductive layer

Evaporative coating of conductive layer

Utilizing chemical vapor deposition (i.e., CVD)

...Of organo-metallic precursor (i.e., MOCVD)

Silicide

...Of refractory group metal (i.e., titanium (Ti), zirconium (Zr), hafnium (Hf), vanadium (V), niobium (Nb), tantalum (Ta), chromium (Cr), molybdenum (Mo), tungsten (W), or alloy thereof)

Electrically conductive polysilicon

Refractory group metal (i.e., titanium (Ti), zirconium (Zr), hafnium (Hf), vanadium (V), niobium (Nb), tantalum (Ta), chromium (Cr), molybdenum (Mo), tungsten (W), or alloy thereof)

Noble group metal (i.e., silver (Ag), gold (Au), platinum (Pt), palladium (Pd), rhodium (Rh), ruthenium (Ru), iridium (Ir), osmium (Os), or alloy thereof)

Copper of copper alloy conductor

Aluminum or aluminum alloy conductor

CHEMICAL ETCHING

Combined with the removal of material by nonchemical means (e.g., ablating, abrading, etc.)

Combined mechanical and chemical material removal

...Simultaneous (e.g., chemical-mechanical polishing, etc.)

...Utilizing particulate abradant

...With coating step

Simultaneous etching and coating

Coating of sidewall

Planarization by etching and coating

...Utilizing reflow

...Plural coating steps

Formation of groove or trench

...Tapered configuration

...Plural coating steps

...Plural coating steps

...Plural coating steps

Having liquid and vapor etching steps

...Alter the etchability of substrate region by compositional or crystalline modification

Vapor phase etching (i.e., dry etching)

...Utilizing electromagnetic or wave energy

...Photo-induced etching

...Photo-induced plasma etching

...By creating electric field (e.g., plasma, glow discharge, etc.)

Utilizing multiple gas energizing means

...Reactive ion beam etching (i.e., RIBE)

...Forming tapered profile (e.g., tapered etching, etc.)

...Including change in etch influencing parameter (e.g., energizing power, etchant composition, temperature, etc.)

...With substrate heating or cooling

...With substrate handling (e.g., conveying, etc.)

...Utilizing multilayered mask

...Compound semiconductor

...Silicon

...Electrically conductive material (e.g., metal, conductive oxide, etc.)

...Silicide

...Metal oxide

...Silicon oxide or glass

...Silicon nitride

...Organic material (e.g., resist, etc.)

...Having microwave gas energizing

......Producing energized gas remotely located from substrate

......Using magnet (e.g., electron cyclotron resonance, etc.)

April 2011
Using specified electrode/susceptor configuration (e.g., of multiple substrates using barrel-type susceptor, planar reactor configuration, etc.) to generate plasma

Producing energized gas remotely located from substrate

Using intervening shield structure

Using magnet (e.g., electron cyclotron resonance, etc.)

Using or orientation dependent etchant (i.e., anisotropic etchant)

Sequential etching steps on a single layer

Differential etching of semiconductor substrate

Utilizing multilayered mask

Substrate possessing multiple layers

Selectively etching substrate possessing multiple layers of differing etch characteristics

Lateral etching of intermediate layer (i.e., undercutting)

Utilizing etch stop layer

PN junction functions as etch stop

Electrically conductive material (e.g., metal, conductive oxide, etc.)

Silicide

Silicon oxide

Silicon nitride

COATING OF SUBSTRATE CONTAINING SEMICONDUCTOR REGION OR OF SEMICONDUCTOR SUBSTRATE

Combined with the removal of material by nonchemical means

Utilizing reflow (e.g., planarization, etc.)

Multiple layers

At least one layer formed by reaction with substrate

Layers formed of diverse composition or by diverse coating processes

Formation of semi-insulative polycrystalline silicon

By reaction with substrate

Implantation of ion (e.g., to form ion amorphousized region prior to selective oxidation, reacting with substrate to form insulative region, etc.)

Compound semiconductor substrate

Reaction with conductive region

Reaction with silicon semiconductive region (e.g., oxynitride formation, etc.)

Oxidation

Using electromagnetic or wave energy

Microwave gas energizing

In atmosphere containing water vapor (i.e., wet oxidation)

In atmosphere containing halogen

Nitridation

Using electromagnetic or wave energy

Microwave gas energizing

Insulative material deposited upon semiconductive substrate

Compound semiconductor substrate

Depositing organic material (e.g., polymer, etc.)

Subsequent heating modifying organic coating composition
..With substrate handling during coating (e.g., immersion, spinning, etc.)

..Insulative material having impurity (e.g., for altering physical characteristics, etc.)

...Introduction simultaneous with deposition

..Insulative material is compound of refractory group metal (i.e., titanium (Ti), zirconium (Zr), hafnium (Hf), vanadium (V), niobium (Nb), tantalum (Ta), chromium (Cr), molybdenum (Mo), tungsten (W), or alloy thereof)

..Tertiary silicon containing compound formation (e.g., oxynitride formation, etc.)

..Silicon oxide formation

...Using electromagnetic or wave energy (e.g., photo-induced deposition, plasma, etc.)

....Organic reactant

....Organic reactant

...Silicon nitride formation

...Utilizing electromagnetic or wave energy (e.g., photo-induced deposition, plasma, etc.)

....Organic reactant

....Organic reactant

...Silicon nitride formation

...Utilizing electromagnetic or wave energy (e.g., photo-induced deposition, plasma, etc.)

....Organic reactant

....Organic reactant

RADIATION OR ENERGY TREATMENT MODIFYING PROPERTIES OF SEMICONDUCTOR REGION OF SUBSTRATE (E.G., THERMAL, CORPUSCULAR, ELECTROMAGNETIC, ETC.)

..Compound semiconductor

..Ordering or disordering

..Ionized irradiation (e.g., corpuscular or plasma treatment, etc.)

..By differential heating

MISCELLANEOUS

CROSS-REFERENCE ART COLLECTIONS

BULK EFFECT DEVICE MAKING

CAPACITIVE JUNCTION

CAPPING LAYER

CATALYST AIDED DEPOSITION
MASKING

. Movable
. Shadow
. Special (e.g., metal, etc.)
. Step and repeat
. Subphotolithographic processing
. Radiation resist
. Multilayer mask including nonradiation sensitive layer
. Lift-off
. Utilizing antireflective layer

MAKING RADIATION RESISTANT DEVICE

MAKING OXIDE-NITRIDE-OXIDE DEVICE

MAKING MULTIPLE WAVELENGTH EMISIVE DEVICE

MAKING METAL-INSULATOR-METAL DEVICE

PASSIVATION LAYER

MECHANICAL POLISHING OF WAFER

POROUS SEMICONDUCTOR

ION BEAM SOURCE AND GENERATION

QUANTUM DOTS AND LINES

REMOVING PROCESS RESIDUES FROM VERTICAL SUBSTRATE SURFACES

ROUGHENED SURFACE

SELECTED JUNCTION FORMATION

THEMORPHOIZED LAYER

SEMICONDUCTOR ON SPECIFIED INSULATOR

SEMICONDUCTOR-METAL-SEMICONDUCTOR

SIMULTANEOUS FORMATION OF MONOCRystalline AND POLYCRYSTalline REGIONS

SPECIFIED ETCH STOP MATERIAL

STOICHIOMETRIC CONTROL OF HOST SUBSTRATE COMPOSITION

STORED CHARGE ERASURE

SUBSTRATE OR MASK ALIGNING FEATURE

TEMPORARY PROTECTIVE LAYER

THINNING OR REMOVAL OF SUBSTRATE

FORMING TAPERED EDGES ON SUBSTRATE OR ADJACENT LAYERS

TUNNEL DIODES

UTILIZING PROCESS EQUIVALENTS OR OPTIONS

UTILIZING VARYING DIELECTRIC THICKNESS

VARYING ORIENTATION OF DEVICES IN ARRAY

ZENER DIODES

FOREIGN ART COLLECTIONS

FOR 000 CLASS-RELATED FOREIGN DOCUMENTS

Any foreign patents or non-patent literature from subclasses that have been reclassified have been transferred directly to FOR Collections listed below. These Collections contain only foreign patents or non-patent literature. The parenthetical references in the Collection titles refer to the abolished subclasses from which these Collections were derived.

METHODS (156/1)

FOR 100 . Etching of semiconductor precursor, substrates, and devices used in an electrical function (156/625.1)

FOR 101 . Measuring, testing, or inspecting (156/626.1)

FOR 102 . By electrical means or of electrical property (156/627.1)

FOR 103 . Altering the etchability of a substrate by alloying, diffusing, or chemical reacting (156/628.1)

FOR 104 . With uniting of preforms (e.g., laminating, etc.) (156/629.1)

FOR 105 . Prior to etching (156/630.1)

FOR 106 . Delamination subsequent to etching (156/631.1)

FOR 107 . With coating (156/632.1)

FOR 108 . Differential etching (156/633.1)

FOR 109 . Metal layer etched (156/634.1)

FOR 110 . With in situ activation or combining of etching components on surface (156/635.1)

FOR 111 . With thin film of etchant between relatively moving substrate and conforming surface (e.g., chemical lapping, etc.) (156/636.1)
FOR 112 ..With relative movement between the substrate and a confined pool of etchant (156/637.1)
FOR 113 ...With removal of adhered reaction product from substrate (156/638.1)
FOR 114 ...With substrate rotation, repeated dipping, or advanced movement (156/639.1)
FOR 115 ..Projection of etchant against a moving substrate or controlling the angle or pattern of projected etchant (156/640.1)
FOR 116 ..Recycling or regenerating etchant (156/642.1)
FOR 117 ..With treatment by high energy radiation or plasma (e.g., ion beam, etc.) (156/643.1)
FOR 118 ..Forming or increasing the size of an aperture (156/644.1)
FOR 119 ..With mechanical deformation, severing, or abrading of a substrate (156/645.1)
FOR 120 ..Etchant is a gas (156/646.1)
FOR 121 ..Etching according to crystalline planes (156/647.1)
FOR 122 ..Etching isolates or modifies a junction in a barrier layer (156/648.1)
FOR 123 ...Discrete junction isolated (e.g., mesa formation, etc.) (156/649.1)
FOR 124 ..Sequential application of etchant material (156/650.1)
FOR 125 ...Sequentially etching the same surface of a substrate (156/651.1)
FOR 126 ....Each etching exposes surface of an adjacent layer (156/652.1)
FOR 127 .....Etched layer contains silicon (e.g., oxide, nitride, etc.) (156/653.1)
FOR 128 ..Differential etching of a substrate (156/654.1)
FOR 129 ...Composite substrate (156/655.1)
FOR 130 ....Substrate contains metallic element or compound (156/656.1)
FOR 131 ....Substrate contains silicon or silicon compound (156/657.1)
FOR 132 ...Resist coating (156/659.11)
FOR 133 ....Plural resist coating (156/661.11)
FOR 134 ..Silicon, germanium, or gallium containing substrate (156/662.1)
FOR 135 MAKING DEVICE HAVING ORGANIC SEMICONDUCTOR COMPONENT (437/1)
FOR 136 MAKING DEVICE RESPONSIVE TO RADIATION (437/2)
FOR 137 .Radiation detectors, e.g., infrared, etc. (437/3)
FOR 138 .Composed of polycrystalline material (437/4)
FOR 139 .Having semiconductor compound (437/5)
FOR 140 MAKING THYRISTOR, E.G., DIAC, TRIAC, ETC. (437/6)
FOR 141 INCLUDING CONTROL RESPONSIVE TO SENSED CONDITION (437/7)
FOR 142 INCLUDING TESTING OR MEASURING (437/8)
FOR 143 INCLUDING APPLICATION OF VIBRATORY FORCE (437/9)
FOR 144 INCLUDING GETTERING (437/10)
FOR 145 .By ion implanting or irradiating (437/11)
FOR 146 .By layers which are coated, contacted, or diffused (437/12)
FOR 147 .By vapor phase surface reaction (437/13)
FOR 148 THERMOMIGRATION (437/14)
FOR 149 INCLUDING FORMING A SEMICONDUCTOR JUNCTION (437/15)
FOR 150 .Using energy beam to introduce dopant or modify dopant distribution (437/16)
FOR 151 ..Neutron, gamma ray or electron beam (437/17)
FOR 152 ..Ionized molecules (437/18)
FOR 153 ..Coherent light beam (437/19)
FOR 154 ..Ion beam implantation (437/20)
FOR 155 ..Of semiconductor on insulating substrate (437/21)
FOR 156 ...Of semiconductor compound (437/22)
FOR 157 ....Light emitting diode (LED) (437/23)
FOR 158 ...Providing nondopant ion including proton (437/24)
FOR 159 ...Providing auxiliary heating (437/25)
FOR 160 ...Forming buried region (437/26)
FOR 161 ....Including multiple implantations of same region (437/27)
FOR 162 ....Through insulating layer (437/28)
FOR 163 .....Forming field effect transistor (FET) type device (437/29)
FOR 164 ....Using same conductivity type dopant (437/30)
FOR 165 ....Forming bipolar transistor (NPN/PNP) (437/31)
FOR 166 .....Lateral bipolar transistor (437/32)
FOR 167 .....Having dielectric isolation (437/33)
FOR 168 ....Forming complementary MOS (metal oxide semiconductor) (437/34)
FOR 169 ...Using oblique beam (437/35)
FOR 170 ...Using shadow mask (437/36)
FOR 171 ...Having projected range less than thickness of dielectrics on substrate (437/37)
FOR 172 ...Into shaped or grooved semiconductor substrate (437/38)
FOR 173 ...Involving Schottky contact formation (437/39)
FOR 202 ....Gate structure constructed of diverse dielectrics (437/42)
FOR 203 .....Gate surrounded by dielectric layer, e.g., floating gate, etc. (437/43)
FOR 204 .....Adjusting channel dimension (437/44)
FOR 205 .....Active step for controlling threshold voltage (437/45)
FOR 185 .....Self-aligned (437/41 R)
FOR 186 .....With bipolar (437/41 RBP)
FOR 187 .....CMOS (437/41 RCM)
FOR 188 .....Lightly doped drain (437/41 RLD)
FOR 189 .....Memory devices (437/41 RMM)
FOR 190 .....Asymmetrical FET (437/41 AS)
FOR 191 .....Channel specifics (437/41 CS)
FOR 192 .....DMOS/vertical FET (437/41 DM)
FOR 193 .....Gate specifics (437/41 GS)
FOR 194 .....Junction FET/static induction transistor (437/41 JP)
FOR 195 .....Layered channel (437/41 LC)
FOR 196 .....Specifics of metallization/contact (437/41 SM)
FOR 197 .....Recessed gate (Schottky falls below in SH) (437/41 RG)
FOR 198 .....Schottky gate/MESFET (437/41 SH)
FOR 199 .....Sidewall (437/41 SW)
FOR 200 .....Thin film transistor, inverted (437/41 TFI)
FOR 201 .....Thin film transistor (437/41 TFT)
FOR 174 ....Forming pair of device regions separated by gate structure, i.e., FET (437/40 R)
FOR 175 .....Asymmetrical FET (any asymmetry in S/D profile, gate spacing, etc.) (437/40 AS)
FOR 176 .....DMOS/vertical FET (437/40 DM)
FOR 177 .....Gate specific (specifics of gate insulator/structure/material/contact) (437/40 GS)
FOR 178 .....Junction FET/static induction transistor (437/40 JP)
FOR 179 .....Layered channel (e.g., HEMT, MODFET, 2DEG, heterostructure FETS) (437/40 LC)
FOR 180 .....Recessed gate (437/40 RG)
FOR 181 .....Schottky gate/MESFET (controls over RG) (437/40 SH)
FOR 182 .....Sidewall (not LDDs) (437/40 SW)
FOR 183 .....Thin film transistor inverted/staggered (437/40 TFT)
FOR 184 .....Thin film transistor (437/40 TFT)
FOR 206 .....Into polycrystalline or polyamorphous regions (437/46)
FOR 207 .....Integrating active with passive devices (437/47)
FOR 208 .....Forming plural active devices in grid/array, e.g., RAMS/ROMS, etc. (437/48)
FOR 209 .....Having multiple-level electrodes (437/49)
FOR 210 .....Forming electrodes in laterally spaced relationships (437/50)
FOR 211 .....Making assemblies of plural individual devices having community feature, e.g., integrated circuit, electrical connection, etc. (437/51)
FOR 212 .....Memory devices (437/52)
FOR 213 ..Charge coupled devices (CCD) (437/53)
FOR 214 ..Diverse types (437/54)
FOR 215 ...Integrated injection logic (I2L) circuits (437/55)
FOR 216 ...Plural field effect transistors (CMOS) (437/56)
FOR 217 ....Complementary metal oxide having diverse conductivity source and drain regions (437/57)
FOR 218 ....Having like conductivity source and drain regions (437/58)
FOR 219 ...Including field effect transistor (437/59)
FOR 220 ...Including passive device (437/60)
FOR 221 .Including isolation step (437/61)
FOR 222 ..By forming total dielectric isolation (437/62)
FOR 223 ..By forming vertical isolation combining dielectric and PN junction (437/63)
FOR 224 ..Using vertical dielectric (air-gap/insulator) and horizontal PN junction (437/64)
FOR 225 ...Grooved air-gap only (437/65)
FOR 226 ....V-groove (437/66)
FOR 227 ...Grooved and refilled with insulator (437/67)
FOR 228 ....V-groove (437/68)
FOR 229 ...Recessed oxide by localized oxidation (437/69)
FOR 230 ....Preliminary formation of guard ring (437/70)
FOR 231 ....Preliminary anodizing (437/71)
FOR 232 ....Preliminary etching of groove (437/72)
FOR 233 ....Using overhanging oxidation mask and pretreatment of recessed walls (437/73)
FOR 234 ..Isolation by PN junction only (437/74)
FOR 235 ...By diffusion from upper surface only (437/75)
FOR 236 ...By up-diffusion from substrate region and down diffusion into upper surface layer (437/76)
FOR 237 ....Substrate and epitaxial regions of same conductivity type, i.e., P or N (437/77)
FOR 238 ...By etching and refilling with semiconductor material having diverse conductivity (437/78)
FOR 239 ...Using polycrystalline region (437/79)
FOR 240 .Shadow masking (437/80)
FOR 241 .Doping during fluid growth of semiconductor material on substrate (437/81)
FOR 242 ...Including heat to anneal (437/82)
FOR 243 ...Growing single crystal on amorphous substrate (437/83)
FOR 244 ...Growing single crystal on single crystal insulator (SOS) (437/84)
FOR 245 ...Including purifying stage during growth (437/85)
FOR 246 ...Using transitory substrate (437/86)
FOR 247 ...Using inert atmosphere (437/87)
FOR 248 ...Using catalyst to alter growth process (437/88)
FOR 249 ...Growth through opening (437/89)
FOR 250 ...Forming recess in substrate and refilling (437/90)
FOR 251 ....By liquid phase epitaxy (437/91)
FOR 252 ...By liquid phase epitaxy (437/92)
FOR 253 ...Specified crystal orientation other than (100) or (111) planes (437/93)
FOR 254 ...Introducing minority carrier life time reducing dopant during growth, i.e., deep level dopant Au (Gold), Cr (Cromium), Fe (Iron), Ni (Nickel), etc. (437/94)
FOR 255 ...Autodoping control (437/95)
FOR 256 ...Compound formed from Group III and Group V elements (437/96)
FOR 257 ...Forming buried regions with outdiffusion control (437/97)
FOR 258 ...Plural dopants simultaneously outdiffusioned (437/98)
FOR 259 ...Growing mono and polycrystalline regions simultaneously (437/99)
FOR 260 ...Growing silicon carbide (SiC) (437/100)
FOR 261 ...Growing amorphous semiconductor material (437/101)
FOR 262 ...Source and substrate in close-space relationship (437/102)
FOR 263  ...Group IV elements (437/103)
FOR 264  ...Compound formed from Group III and Group V elements (437/104)
FOR 265  ...Vacuum growing using molecular beam, i.e., vacuum deposition (437/105)
FOR 266  ...Group IV elements (437/106)
FOR 267  ...Compound formed from Group III and Group V elements (437/107)
FOR 268  ...Growing single layer in multi-steps (437/108)
FOR 269  ...Polycrystalline layers (437/109)
FOR 270  ...Using modulated dopants or materials, e.g., superlattice, etc. (437/110)
FOR 271  ...Using preliminary or intermediate metal layer (437/111)
FOR 272  ...Growing by varying rates (437/112)
FOR 273  ...Using electric current, e.g., Peltier effect, glow discharge, etc. (437/113)
FOR 274  ...Using seed in liquid phase (437/114)
FOR 275  ...Pulling from melt (437/115)
FOR 276  ...And diffusing (437/116)
FOR 277  ...Liquid and vapor phase epitaxy in sequence (437/117)
FOR 278  ...Involving capillary action (437/118)
FOR 279  ...Sliding liquid phase epitaxy (437/119)
FOR 280  ...Modifying melt composition (437/120)
FOR 281  ...Controlling volume or thickness of growth (437/121)
FOR 282  ...Preliminary dissolving substrate surface (437/122)
FOR 283  ...With nonlinear slide movement (437/123)
FOR 284  ...One melt simultaneously contacting plural substrates (437/124)
FOR 285  ...Tipping liquid phase epitaxy (437/125)
FOR 286  ...Heteroepitaxy (437/126)
FOR 287  ...Multi-color light emitting diode (LED) (437/127)
FOR 288  ...Graded composition (437/128)
FOR 289  ...Forming laser (437/129)
FOR 290  ...By liquid phase epitaxy (437/130)
FOR 291  ...Si (Silicon on Ge (Germanium) or Ge (Germanium) on Si (Silicon) (437/131)
FOR 292  ...Either Si (Silicon) or Ge (Germanium) layered with or on compound formed from Group III and Group V elements (437/132)
FOR 293  ...Compound formed from Group III and Group V elements on diverse Group III and Group V including substituted Group III and Group V compounds (437/133)
FOR 294  ...By fusing dopant with substrate, e.g., alloying, etc. (437/134)
FOR 295  ...Using flux (437/135)
FOR 296  ...Passing flux through material (437/136)
FOR 297  ...With application of pressure to material during fusing (437/137)
FOR 298  ...Including plural controlled heating or cooling steps (437/138)
FOR 299  ...Including diffusion after fusion step (437/139)
FOR 300  ...Including additional material to improve wettability or flow characteristics (437/140)
FOR 301  ...Diffusing a dopant (437/141)
FOR 302  ...To control carrier lifetime, i.e., deep level dopant Au (Gold), Cr (Chromium), Fe (Iron), Ni (Nickel), etc. (437/142)
FOR 303  ...Al (Aluminum) dopant (437/143)
FOR 304  ...Li (Lithium) dopant (437/144)
FOR 305  ...Including nonuniform heating (437/145)
FOR 306  ...To solid state solubility concentration (437/146)
FOR 307  ...Using multiple layered mask (437/147)
FOR 308  ...Having plural predetermined openings in master mask (437/148)
FOR 309  ...Forming partially overlapping regions (437/149)
FOR 310  ...Plural dopants in same region, e.g., through same mask opening, etc. (437/150)
FOR 311  ...Simultaneously (437/151)
FOR 312  ...Plural dopants simultaneously in plural region (437/152)
FOR 313 . Single dopant forming plural diverse regions (437/153)
FOR 314 . Forming regions of different concentrations or different depths (437/154)
FOR 315 . Using metal mask (437/155)
FOR 316 . Outwardly (437/156)
FOR 317 . Laterally under mask (437/157)
FOR 318 . Edge diffusion by using edge portion of structure other than masking layer to mask (437/158)
FOR 319 . From melt (437/159)
FOR 320 . From solid dopant source in contact with substrate (437/160)
FOR 321 . Using capping layer over dopant source to prevent outdiffusion of dopant (437/161)
FOR 322 . Polycrystalline semiconductor source (437/162)
FOR 323 . Organic source (437/163)
FOR 324 . Glassy source or doped oxide (437/164)
FOR 325 . From vapor phase (437/165)
FOR 326 . In plural stages (437/166)
FOR 327 . Zinc (Zn) dopant (437/167)
FOR 328 . Solid source is operative in relation with semiconductor material (437/168)
FOR 329 . In capsule type enclosure (437/169)
FOR 330 . Directly applying electrical current (437/170)
FOR 331 . And regulating temperature (437/171)
FOR 332 . Alternating or pulsed current (437/172)
FOR 333 . Applying corpuscular or electromagnetic energy (437/173)
FOR 334 . To anneal (437/174)
FOR 335 . Forming Schottky contact (437/175)
FOR 336 . On semiconductor compound (437/176)
FOR 337 . Multi-layer electrode (437/177)
FOR 338 . Using platinum group silicide, i.e., silicide of Pt (Platinum), Pd (Palladium), Rh (Rhodium), Ru (Ruthenium), Ir (Iridium), Os (Osmium) (437/178)
FOR 339 . Using metal, i.e., Pt (Platinum), Pd (Palladium), Rh (Rhodium), Ru (Ruthenium), Ir (Iridium), Os (Osmium), Au (Gold), Ag (Silver) (437/179)
FOR 340 . Making or attaching electrode on or to semiconductor, or securing completed semiconductor to mounting or housing (437/180)
FOR 341 . Forming transparent electrode (437/181)
FOR 342 . Forming beam electrode (437/182)
FOR 343 . Forming bump electrode (437/183)
FOR 344 . Electrode formed on substrate composed of elements of Group III and Group V semiconductor compound (437/184)
FOR 345 . Electrode formed on substrate composed of elements of Group II and Group VI semiconductor compound (437/185)
FOR 346 . Single polycrystalline electrode layer on substrate (437/186)
FOR 347 . Single metal layer electrode on substrate (437/187)
FOR 348 . Subsequently fusing, e.g., alloying, sintering, etc. (437/188)
FOR 349 . Forming plural layered electrode (437/189)
FOR 350 . Including central layer acting as barrier between outer layers (437/190)
FOR 351 . Of polysilicon only (437/191)
FOR 352 . Including refractory metal layer of Ti (Titanium), Zr (Zirconium), Hf (Hafnium), V (Vanadium), Nb (Niobium), Ta (Tantalum), Cr (Chromium), Mo (Molybdenum), W (Tungsten) (437/192)
FOR 353 . Including polycrystalline silicon layer (437/193)
FOR 354 . Including Al (Aluminum) layer (437/194)
FOR 355 . Including layer separated by insulator (437/195)
FOR 356 . Forming electrode of alloy or electrode of a compound of Si (Silicon) (437/196)
FOR 357 . Al (Aluminum) alloy (437/197)
FOR 358 . Including Cu (Copper) (437/198)
FOR 359 ...Including Si (Silicon) (437/199)
FOR 360 ...Silicide of Ti (Titanium), Zr (Zirconium), Hf (Hafnium), V (Vanadium), Nb (Niobium), Ta (Tantalum), Cr (Chromium), Mo (Molybdenum), W (Tungsten), (437/200)
FOR 361 ...Of platinum metal group Ru (Ruthenium), Rh (Rhodium), Pd (Palladium), Os (Osmium), Ir (Iridium), Pt (Platinum) (437/201)
FOR 362 ...By fusing metal with semiconductor (alloying) (437/202)
FOR 363 ...Depositing electrode in preformed recess in substrate (437/203)
FOR 364 ...Including positioning of point contact (437/204)
FOR 365 ...Making plural devices (437/205)
FOR 366 ...Using strip lead frame (437/206)
FOR 367 ...And encapsulating (437/207)
FOR 368 ...Stacked array, e.g., rectifier, etc. (437/208)
FOR 369 ...Securing completed semiconductor to mounting, housing or external lead (437/209)
FOR 370 ...Including contaminant removal (437/210)
FOR 371 ...Utilizing potting or encapsulating material only to surround leads and device to maintain position, i.e. without housing (437/211)
FOR 372 ...Including application of pressure (437/212)
FOR 373 ...Glass material (437/213)
FOR 374 ...Utilizing header (molding surface means) (437/214)
FOR 375 ...Insulating housing (437/215)
FOR 376 ...Including application of pressure (437/216)
FOR 377 ...And lead frame (437/217)
FOR 378 ...Ceramic housing (437/218)
FOR 379 ...Including encapsulating (437/219)
FOR 380 ...Lead frame (437/220)
FOR 381 ...Metallic housing (437/221)
FOR 382 ...Including application of pressure (437/222)
FOR 383 ...Including glass support base (437/223)
FOR 384 ...Including encapsulating (437/224)
FOR 385 ...Including coating or material removal, e.g., etching, grinding, etc. (437/225)
FOR 386 ...Substrate dicing (437/226)
FOR 387 ...With a perfecting coating (437/227)
FOR 388 ...Coating and etching (437/228)
FOR 389 ...Of radiation resist layer (437/229)
FOR 390 ...By immersion metal plating from solution, i.e., electroless plating (437/230)
FOR 391 ...By spinning (437/231)
FOR 392 ...Elemental Se (Selenium) substrate or coating (437/232)
FOR 393 ...Of polycrystalline semiconductor material on substrate (437/233)
FOR 394 ...Semiconductor compound or mixed semiconductor material (437/234)
FOR 395 ...Of a dielectric or insulative material (437/235)
FOR 396 ...Containing Group III atom (437/236)
FOR 397 ...By reacting with substrate (437/237)
FOR 398 ...Monoxide or dioxide or Ge (Germanium) or Si (Silicon) (437/238)
FOR 399 ...By reacting with substrate (437/239)
FOR 400 ...Doped with impurities (437/240)
FOR 401 ...Si (Silicon) and N (Nitrogen) (437/241)
FOR 402 ...By chemical reaction with substrate (437/242)
FOR 403 ...Directly on semiconductor substrate (437/243)
FOR 404 ...By chemical conversion of substrate (437/244)
FOR 405 ...Comprising metal layer (437/245)
FOR 406 ...On metal (437/246)
FOR 407 ...Temperature treatment modifying properties of semiconductor, e.g., annealing, sintering, etc. (437/247)
FOR 408 ...Heating and cooling (437/248)
FOR 409 ...Including shaping (437/249)
FOR 410 ...Miscellaneous (437/250)
FOR 411 ...Utilizing process equivalents or options (437/900)
FOR 412 MAKING PRESSURE SENSITIVE DEVICE (437/901)
FOR 413 MAKING DEVICE HAVING HEAT SINK (437/902)
FOR 414 MAKING THERMOPILE (437/903)
FOR 415 MAKING DIODE (437/904)
FOR 416 MAKING LIGHT EMITTING DIODE (437/905)
FOR 417 MAKING MOUNTING AND CONTACT (437/906)
FOR 418 LASER PROCESSING OF FIELD EFFECT TRANSISTOR (FET) (437/907)
FOR 419 LASER PROCESSING OF TRANSISTOR (437/908)
FOR 420 MAKING TRANSISTOR ONLY (437/909)
FOR 421 MAKING JOSEPHSON JUNCTION DEVICE (437/910)
FOR 422 MAKING JUNCTION-FIELD EFFECT TRANSISTOR (J-FET) OR STATIC INDUCTION THYRISTOR (SIT) DEVICE (437/911)
FOR 423 MAKING METAL SEMICONDUCTOR FIELD EFFECT TRANSISTOR (MESFET) DEVICE ONLY (437/912)
FOR 424 MAKING METAL OXIDE SEMICONDUCTOR FIELD EFFECT TRANSISTOR (MOSFET) DEVICE (437/913)
FOR 425 MAKING NON-EPI TAxIAL DEVICE (437/914)
FOR 426 MAKING VERTICALLY STACKED DEVICES (3-DIMENSIONAL STRUCTURE) (437/915)
FOR 427 MAKING PHOTOCATHODE OR VIDICON (437/916)
FOR 428 MAKING LATERAL TRANSISTOR (437/917)
FOR 429 MAKING RESISTOR (437/918)
FOR 430 MAKING CAPACITOR (437/919)
FOR 431 MAKING SILICON-OXIDE-NITRIDE-OXIDE ON SILICON (SONOS) DEVICE (437/920)
FOR 432 MAKING STRAIN GAGE (437/921)
FOR 433 MAKING FUSE OR FUSABLE DEVICE (437/922)
FOR 434 WITH REPAIR OR RECOVERY OF DEVICE (437/923)
FOR 435 HAVING SUBSTRATE OR MASK ALIGNING FEATURE (437/924)
FOR 436 SUBSTRATE SUPPORT OR CAPSULE CONSTRUCTION (437/925)
FOR 437 CONTINUOUS PROCESSING (437/926)
FOR 438 FORMING HOLLOW BODIES AND ENCLOSED CAVITIES (437/927)
FOR 439 ENERGY BEAM TREATING RADIATION RESIST ON SEMICONDUCTOR (437/928)
FOR 440 RADIATION ENHANCED DIFFUSION (R.E.D.) (437/929)
FOR 441 ION BEAM SOURCE AND GENERATION (437/930)
FOR 442 IMPLANTATION THROUGH MASK (437/931)
FOR 443 RECOIL IMPLANTATION (437/932)
FOR 444 DUAL SPECIES IMPLANTATION OF SEMICONDUCTOR (437/933)
FOR 445 DOPANT ACTIVATION PROCESS (437/934)
FOR 446 BEAM WRITING OF PATTERNS (437/935)
FOR 447 BEAM PROCESSING OF COMPOUND SEMICONDUCTOR DEVICE (437/936)
FOR 448 HYDROGEN PLASMA TREATMENT OF SEMICONDUCTOR DEVICE (437/937)
FOR 449 MAKING RADIATION RESISTANT DEVICE (437/938)
FOR 450 DEFECT CONTROL OF SEMICONDUCTOR WAFER (PRETREATMENT) (437/939)
FOR 451 SELECTIVE OXIDATION OF ION AMORPHOUSIZED LAYERS (437/940)
FOR 452 CONTROLLING CHARGING STATE AT SEMICONDUCTOR-INSULATOR INTERFACE (437/941)
FOR 453 INCOHERENT LIGHT PROCESSING (437/942)
FOR 454 THERMALLY ASSISTED BEAM PROCESSING (437/943)
FOR 455 UTILIZING LIFT OFF (437/944)
FOR 456 STOICHIOMETRIC CONTROL OF HOST SUBSTRATE COMPOSITION (437/945)
FOR 457 SUBSTRATE SURFACE PREPARATION (437/946)
FOR 458 FORMING TAPERED EDGES ON SUBSTRATE OR ADJACENT LAYERS (437/947)
FOR 459 MOVABLE MASK (437/948)
FOR 460 CONTROLLED ATMOSPHERE (437/949)
FOR 461 SHALLOW DIFFUSION (437/950)
FOR 462 AMPHOTERIC DOPING (437/951)
FOR 463 CONTROLLING DIFFUSION PROFILE BY OXIDATION (437/952)
FOR 464 DIFFUSION OF OVERLAPPING REGIONS (COMPENSATION) (437/953)
FOR 465 VERTICAL DIFFUSION THROUGH A LAYER (437/954)
FOR 466 NONSELECTIVE DIFFUSION (437/955)
FOR 467 DISPLACING P-N JUNCTION (437/956)
FOR 468 ELECTROMIGRATION (437/957)
FOR 469 ShAPED JUNCTION FORMATION (437/958)
CLASS 438 SEMICONDUCTOR DEVICE MANUFACTURING: PROCESS

FOR 470 USING NONSTANDARD DOPANT (437/959)
FOR 471 WASHED EMITTER PROCESS (437/960)
FOR 472 EMITTER DIP PREVENTION (OR UTILIZATION) (437/961)
FOR 473 UTILIZING SPECIAL MASKS (CARBON, ETC.) (437/962)
FOR 474 LOCALIZED HEATING CONTROL DURING FLUID GROWTH (437/963)
FOR 475 FLUID GROWTH INVOLVING VAPOR- LIQUID-SOLID STAGES (437/964)
FOR 476 FLUID GROWTH OF COMPOUNDS COMPOSED OF GROUPS II, IV, OR VI ELEMENTS (437/965)
FOR 477 FORMING THIN SHEETS (437/966)
FOR 478 PRODUCING POLYCRYSTALLINE SEMICONDUCTOR MATERIAL (437/967)
FOR 479 SELECTIVE OXIDATION OF POLYCRYSTALLINE LAYER (437/968)
FOR 480 FORMING GRADED ENERGY GAP LAYERS (437/969)
FOR 481 DIFFERENTIAL CRYSTAL GROWTH (437/970)
FOR 482 FLUID GROWTH DOPING CONTROL (437/971)
FOR 483 UTILIZING MELT-BACK (437/972)
FOR 484 SOLID PHASE EPITAXIAL GROWTH (437/973)
FOR 485 THINNING OR REMOVAL OF SUBSTRATE (437/974)
FOR 486 DIFFUSION ALONG GRAIN BOUNDARIES (437/975)
FOR 487 CONTROLLING LATTICE STRAIN (437/976)
FOR 488 UTILIZING ROUGHENED SURFACE (437/977)
FOR 489 UTILIZING MULTIPLE DIELECTRIC LAYERS (437/978)
FOR 490 UTILIZING THICK-THIN OXIDE FORMATION (437/979)
FOR 491 FORMING POLYCRYSTALLINE SEMICONDUCTOR PASSIVATION (437/980)
FOR 492 PRODUCING TAPERED ETCHING (437/981)
FOR 493 REFLOW OF INSULATOR (437/982)
FOR 494 OXIDATION OF GATE OR GATE CONTACT LAYER (437/983)
FOR 495 SELF-ALIGNING FEATURE (437/984)
FOR 496 DIFFERENTIAL OXIDATION AND ETCHING (437/985)
FOR 497 DIFFUSING LATERALLY AND ETCHING (437/986)

April 2011