H03K

PULSE TECHNIQUE (measuring pulse characteristics G01R; mechanical counters having an electrical input G06M; information storage devices in general G11; sample-and-hold arrangements in electric analogue stores G11C27/02; construction of switches involving contact making and breaking for generation of pulses, e.g. by using a moving magnet, H01H; static conversion of electric power H02M; generation of oscillations by circuits employing active elements which operate in a non-switching manner H03B; modulating sinusoidal oscillations with pulses H03C, H04L; discriminator circuits involving pulse counting H03D; automatic control of generators H03L; starting, synchronisation or stabilisation of generators where the type of generator is irrelevant or unspecified H03L; coding, decoding or code conversion in general H03M)

Definition statement

This subclass/group covers:

- Methods, circuits, devices or apparatus using active elements operating in a discontinuous or switching manner for generating, counting, amplifying. Shaping, modulating, demodulating or otherwise manipulating signals;
- Electronic switching not involving contact-making and braking.
- Logic circuits handling electric pulses.

In general, it should be noted that the word 'Pulse' in the title description is a clear limiting feature for this subclass.

References relevant to classification in this subclass

This subclass/group does not cover:

Measuring electrical signals (to get a value)	G01R 17/00- G01R 29/00
Testing electrical circuits	G01R 31/00
Measuring pulse characteristic	G01R
Mechanical counters having an electrical input	G06M;
Information storage devices in	G11

general	
Sample-and-hold arrangements in electric analogue stores	G11C 27/02
Construction of switches involving contact making and breaking for generation of pulses, e.g. by using a moving magnet	H01H
Static conversion of electric power	H02M;
Generation of oscillations by circuits employing active elements which operate in a non-switching manner	H03B;
Odulating sinusoidal oscillations with pulses	H03C, H04L;
Discriminator circuits involving pulse counting	H03D;
Automatic control of generators	H03L
Starting, synchronisation or stabilisation of generators where the type of generator is irrelevant or unspecified	H03L
Coding, decoding or code conversion in general	H03M

Glossary of terms

In this subclass/group, the following terms (or expressions) are used with the meaning indicated:

Differential	really means differential, not just complementary, i.e. two signals with an inverter in between are not differential

H03K 3/00

Circuits for generating electric pulses; Monostable, bistable or multistable circuits (H03K4/00 takes precedence; for digital computers G06F1/025, [N: G06F1/04])

Definition statement

This subclass/group covers:

- Latches and flip-flops;
- Non-linear (switching) oscillators;
- Latching level shifters.

References relevant to classification in this group

This subclass/group does not cover:

Duty cycle correction circuits	H03K 5/1565
Linear (non-switching) oscillators	H03B
Pulse width modulation	H03K 7/08
Random number generators	G06F 7/58

Examples of places where the subject matter of this subclass is covered when specially adapted, used for a particular purpose, or incorporated in a larger system:

Latches and flip-flops used as static stores in semiconductor memories	G11C 11/41
Latches used in scan test of integrated circuits	G01R 31/318541
Power pulse generators for driving lasers	H01S 5/42
Voltage- and current controlled oscillators	H03L 7/0995

Special rules of classification within this group

Latching level shifters should be classified in the corresponding bistable circuit

subgroups of this main group.

H03K 4/00

Generating pulses having essentially a finite slope or stepped portions (generation of supply voltages from deflection waveforms H04N3/18)

Definition statement

This subclass/group covers:

- Relaxation oscillators.
- Switched-capacitor oscillators
- Ramp and sawtooth generators.

Relationship between large subject matter areas

Multivibrators generating pulse signals other than finite-sloped or staircase signals should be classified in H03K 3/00.

References relevant to classification in this group

This subclass/group does not cover:

Direct-digital frequency synthesizers	G06F 1/025
Generation of supply voltages from deflection waveforms	H04N 3/18
Modifying slopes of pulses	H03K 6/04

Special rules of classification within this group

H03K 4/026: Digital generators followed by a digital-to-analog converter to produce analogue output stepped signals.

H03K 5/00

Manipulating pulses not covered by any of the other main groups in this subclass (circuits with regenerative action H03K3/00, H03K4/00; by the use of non-linear magnetic or dielectric devices H03K3/45)

H03K 6/00

Manipulating pulses having a finite slope and not covered by one of the other main groups of this subclass (circuits with regenerative action H03K4/00)

Definition statement

This subclass/group covers:

Slew rate correction in ramp or triangular waveform generators..

References relevant to classification in this group

This subclass/group does not cover:

Slew rate limiting	H03K 5/04, H03K 17/16, H03K 19/017581

H03K 7/00

Modulating pulses with a continuously-variable modulating signal

H03K 9/00

Demodulating pulses which have been modulated with a continuously-variable signal

H03K 11/00

Transforming types of modulations, e.g. position-modulated pulses into duration-modulated pulses

H03K 12/00

Producing pulses by distorting or combining sinusoidal waveforms (combining sinewaves using elements operating in a non-switching manner H03B; [N: limiting or clipping, e.g. H03G11/00])

H03K 17/00

Electronic switching or gating , i.e. not by contact-making or -braking (selection of the stylus or auxiliary electrode in electric printing B41J2/405; sample-and-hold arrangements G11C27/02; switching or interrupting devices in waveguides

H01P; gated amplifiers H03F3/72; switching arrangements for exchange systems using static devices H04Q3/52)

H03K 19/00

Logic circuits, i.e. having at least two inputs acting on one output; Inverting circuits [N: (inverting circuits used as delay elements H03K5/13)]

Definition statement

This subclass/group covers:

Circuits having at least two inputs acting on one output inverting circuits or buffers.

Relationship between large subject matter areas

When a circuit is used or adapted for switching a load, it is classified in H03K 17/00. When it is used/adapted for driving a logic circuit (e.g. output buffer), it goes to H03K 19/00.

References relevant to classification in this group

This subclass/group does not cover:

CAD, Layout and Routing	G06F 17/50
Clock generation/distribution	G06F 1/04
I/O data interface arrangement	G11C 7/10
Hot Plugging (device-to-bus)	G06F 13/4081
Emergency protective circuits	H02H
Baseband systems (for transmission): line drivers, impedance matching, termination	H04L 25/02
Program control	G06F 9/00
ESD protection	H01L 27/0248
Inverting circuits used as delay element	H03K 5/13

Informative references

Attention is drawn to the following places, which may be of interest for search:

Nano-technology logic	B82Y 10/00

Special rules of classification within this group

The groups H03K 19/00369 take precedence over H03K 19/0005

H03K 19/003: Circuits for increasing the reliability, not for notifying the user that a failure took place

H03K 19/00323: Skew compensation

H03K 19/00346: Slope control, slew rate adaptation

H03K 19/007: Circuits in this class go, when they fail, to a safe state. They do not notify the user of a failure

H03K 19/01 covers accelerating switching in logic circuits and should not be confused with H03K 17/04 which covers accelerating the switching of a switch

H03K 19/177: Field Programmable Gate Arrays (FPGA).

H03K 21/00

Details of pulse counters or frequency dividers [N: (number-of-one counters G06F7/607)]

Definition statement

This subclass/group covers:

Details of logic circuits having electric(digital) pulses as input signals and either counting incoming pulses or producing an output pulse stream based on the incoming pulse stream having a modified pulse repeating period.

Reference relevant to classification in this group

This subclass/group does not cover:

High Security Counting	G01C 22/02
Measuring Pulse Width Time	G01R 29/00
Coincidence Detection	G01T 1/72
Non-integer Counting and Performing	G06F 7/60

Operations by counting	
Member-of-one (population) Counter	G06F 7/607
Binary Multiplication andPulse rate divider	G06F 7/62 - G06F 7/68
PLLs including Dividers	H03B, H03L
Changing Frequency	H03K 5/00006

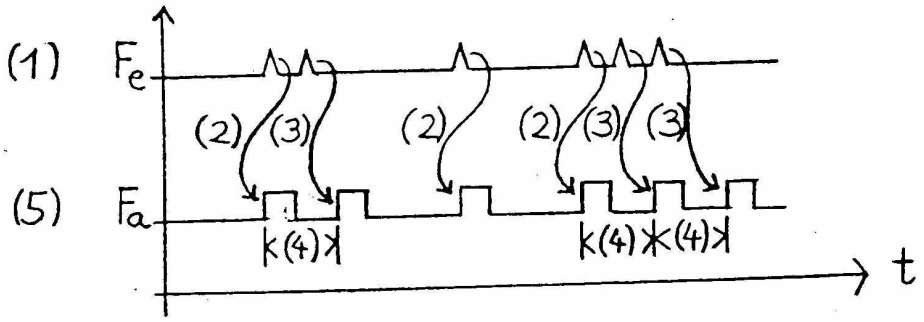
H03K 21/02

Input circuits

Definition statement

This subclass/group covers:

Special logic at input for pulse treatment e.g. pulse shaping



Figur 2

Figure taken from DE3842874

H03K 21/08

Output circuits

Definition statement

This subclass/group covers:
Special logic at register outputs e.g. for a counter value dependent reset.

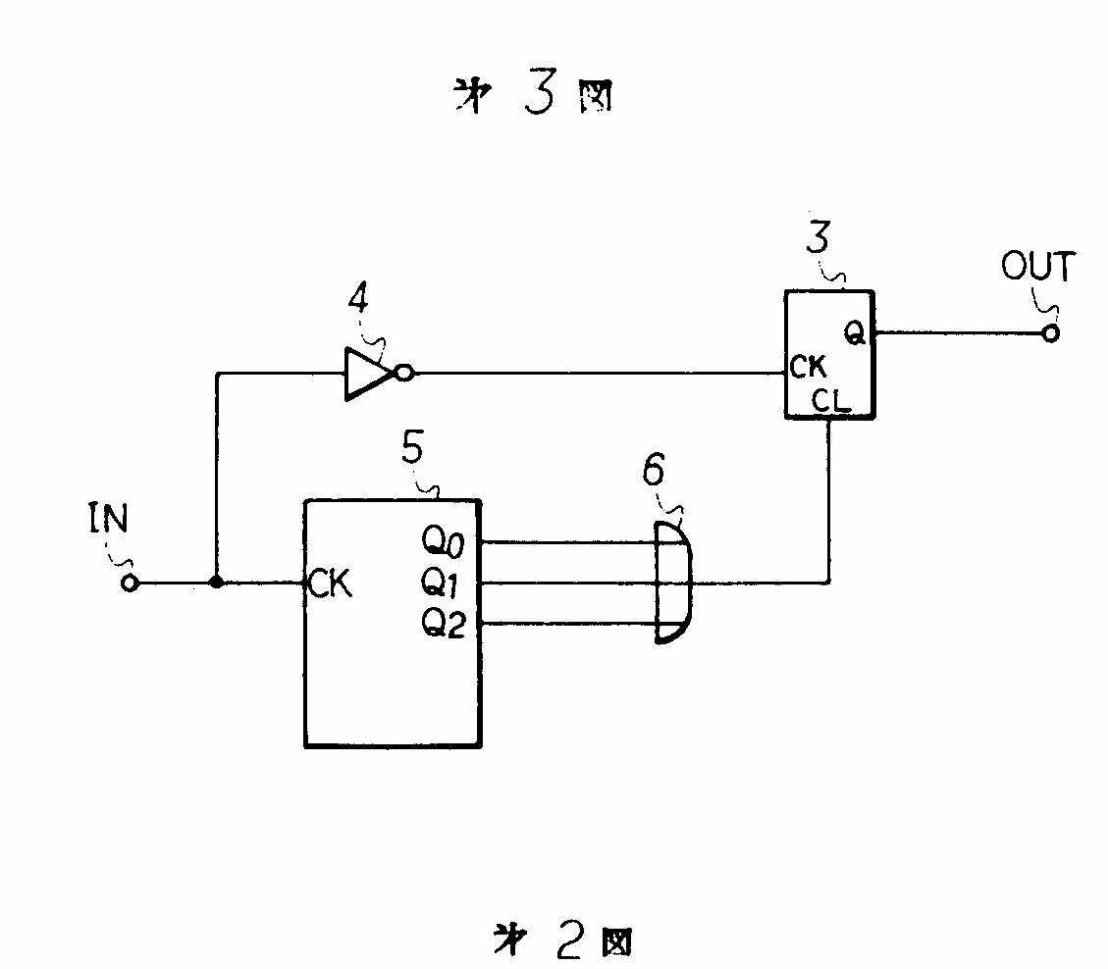


Figure taken from JP57199337

H03K 21/16

Circuits for carrying over pulses between successive decades

Definition statement

This subclass/group covers:

Logic counter having multiple counting stages including a carry over bit between stages.

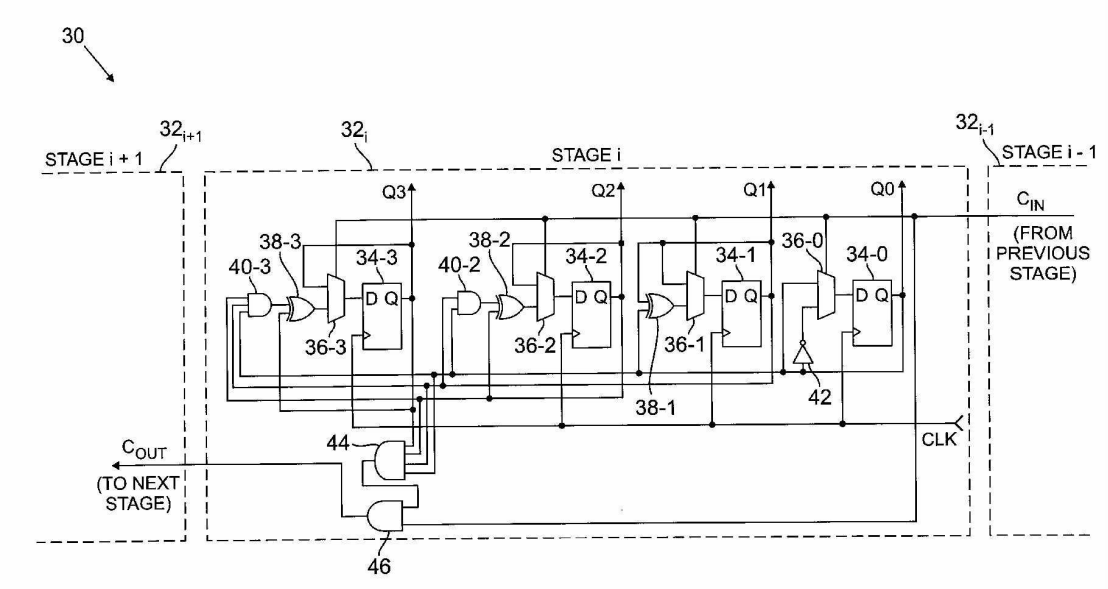


Figure taken from US5,946,369

H03K 21/18

Circuits for visual indication of the result

Definition statement

This subclass/group covers:
Logic for representing the result to a user.

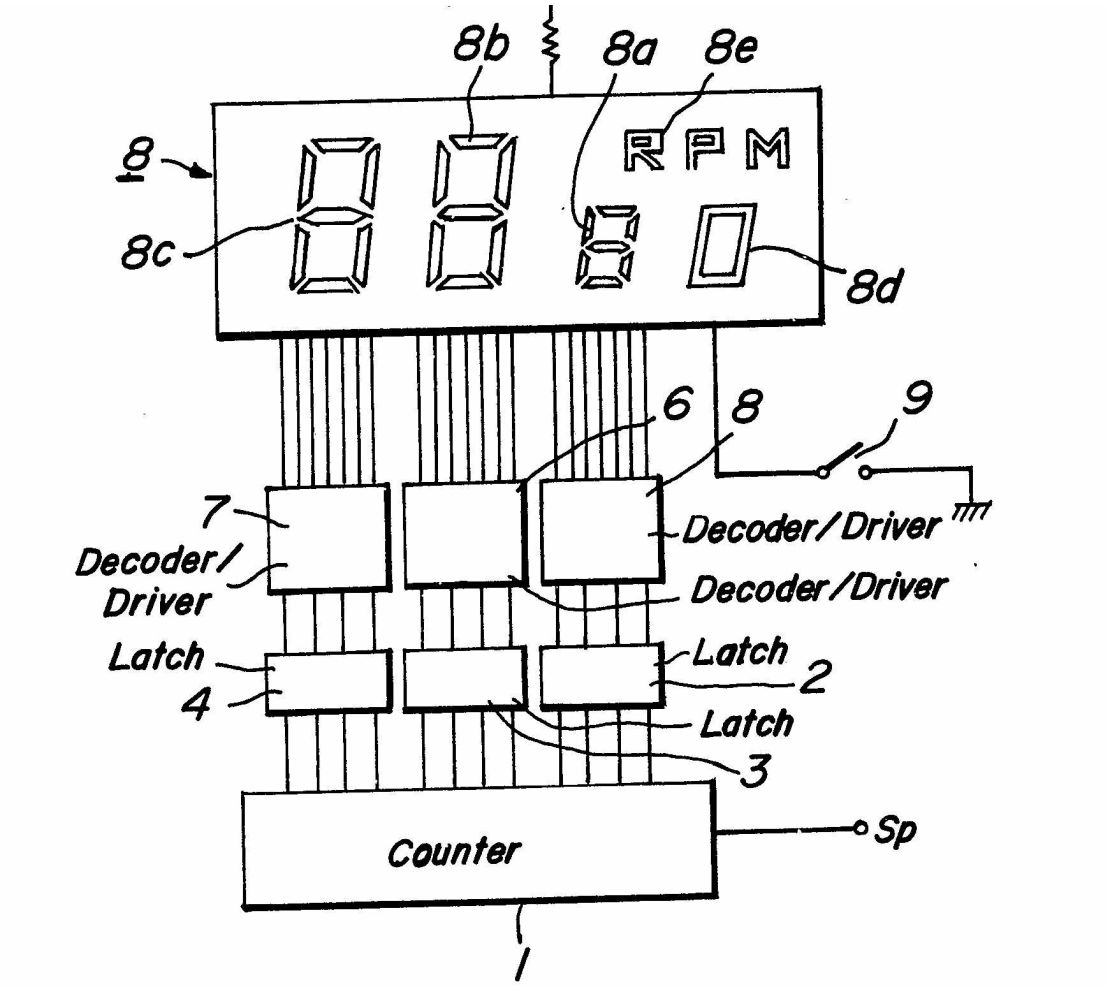


Figure taken from DE3031612

H03K 21/38

Starting, stopping or resetting the counter (counters with a base other than a power of two H03K23/48, H03K23/66)

Definition statement

This subclass/group covers:

Logic for influencing the counter status.

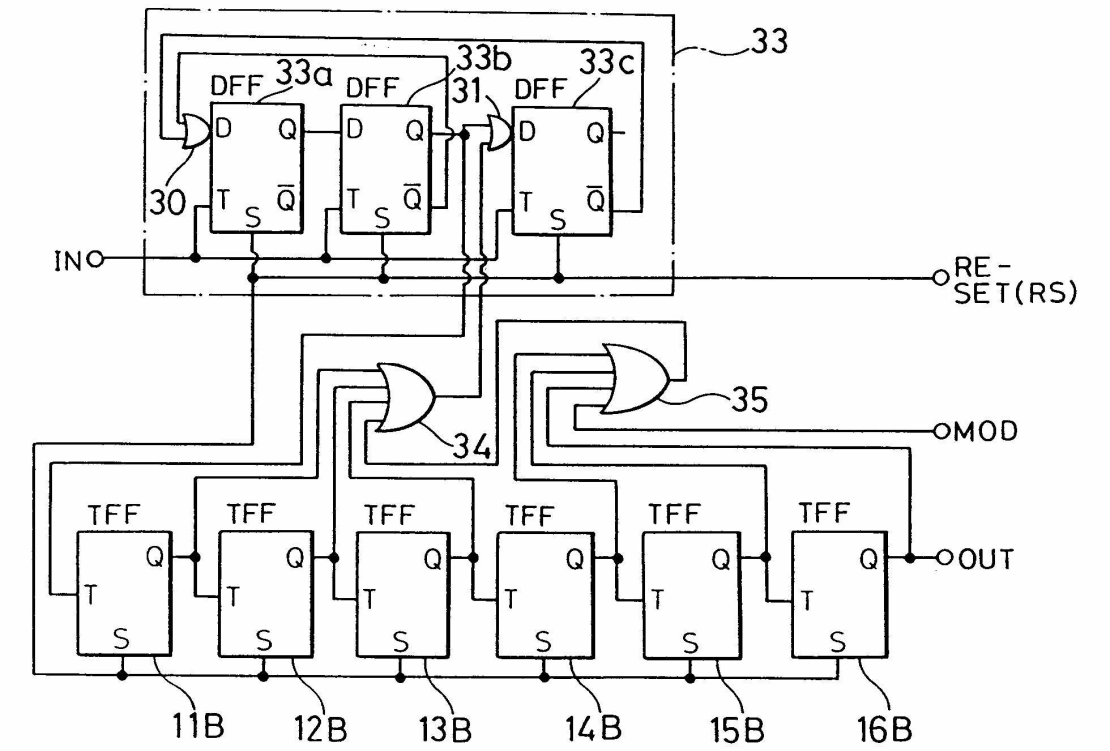


Figure taken from EP0471390.

H03K 21/40

Monitoring; Error detection; Preventing or correcting improper counter operation

Definition statement

This subclass/group covers:

Monitoring whether an error occured during the counting process (not the process producing the pulses)

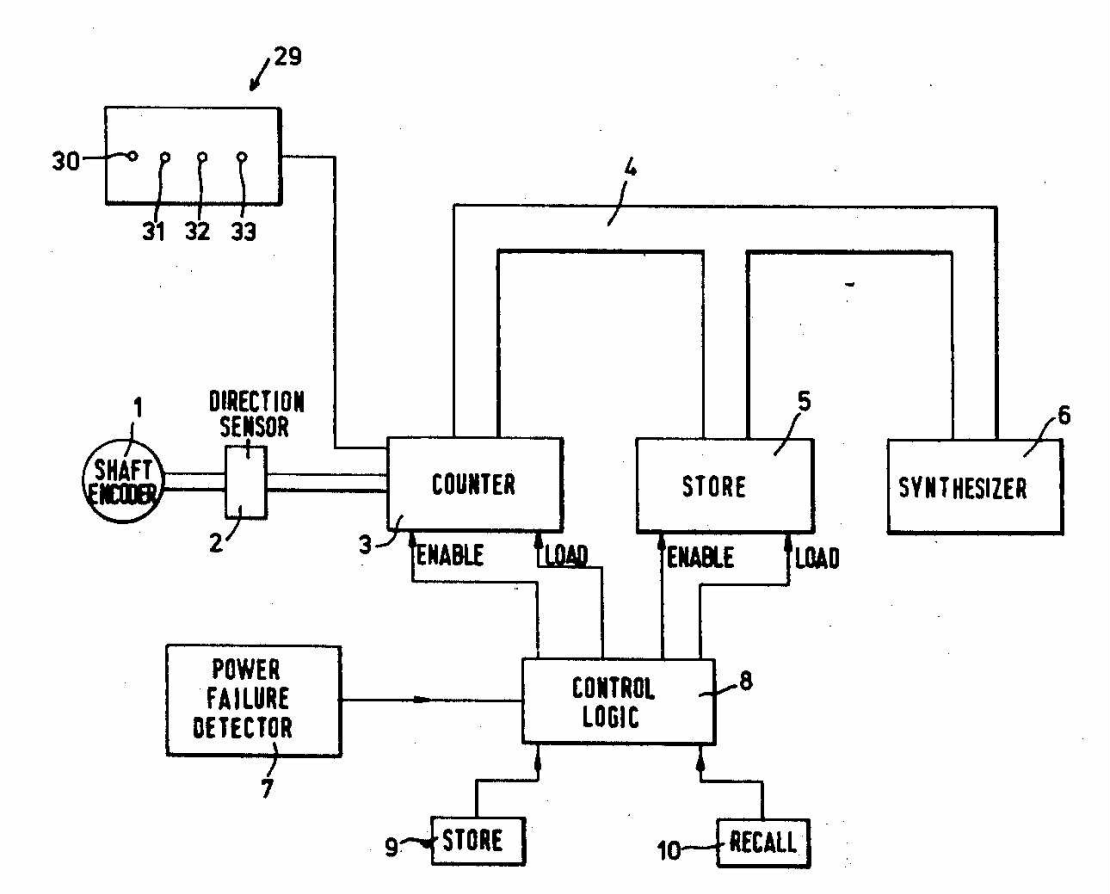


Figure taken from DE2550177

H03K 23/00

Pulse counters comprising counting chains; Frequency dividers comprising counting chains (H03K29/00 takes precedence)

Definition statement

This subclass/group covers:

Logic for digital counting chains used in pulse counters or frequency dividers

H03K 23/001

[N: using elements not covered by groups H03K23/002 and H03K23/74 to H03K23/84]

Definition statement

This subclass/group covers:

Other elements as complementary IGFET's, electrically-ignited compounds e.g. pyrotechnical static relays

H03K 23/004

[N: Counters counting in a non-natural counting order, e.g. random counters]

Definition statement

This subclass/group covers:

Detailed counting encoding scheme.

H03K 23/40

Gating or clocking signals applied to all stages, i.e. synchronous counters [N: (H03K23/74 to H03K23/84 take precedence)]

Definition statement

This subclass/group covers:

Details regarding the clock used for triggering the counting of incoming pulses

H03K 23/58

Gating or clocking signals not applied to all stages, i.e. asynchronous counters (H03K23/74 to H03K23/84 take precedence)

Definition statement

This subclass/group covers:

Counter with a "rippling" trigger pulse form stage to stage - asynchronous counters.

H03K 23/64

with a base or radix other than a power of two (H03K23/40 to H03K23/62 take precedence)

Definition statement

This subclass/group covers:

Variable counting base, non-integer or odd-number counters.

H03K 25/00

Pulse counters with step-by-step integration and static

storage; Analogous frequency dividers

Definition statement

This subclass/group covers:
Static storage type counters - e.g. capacitive type

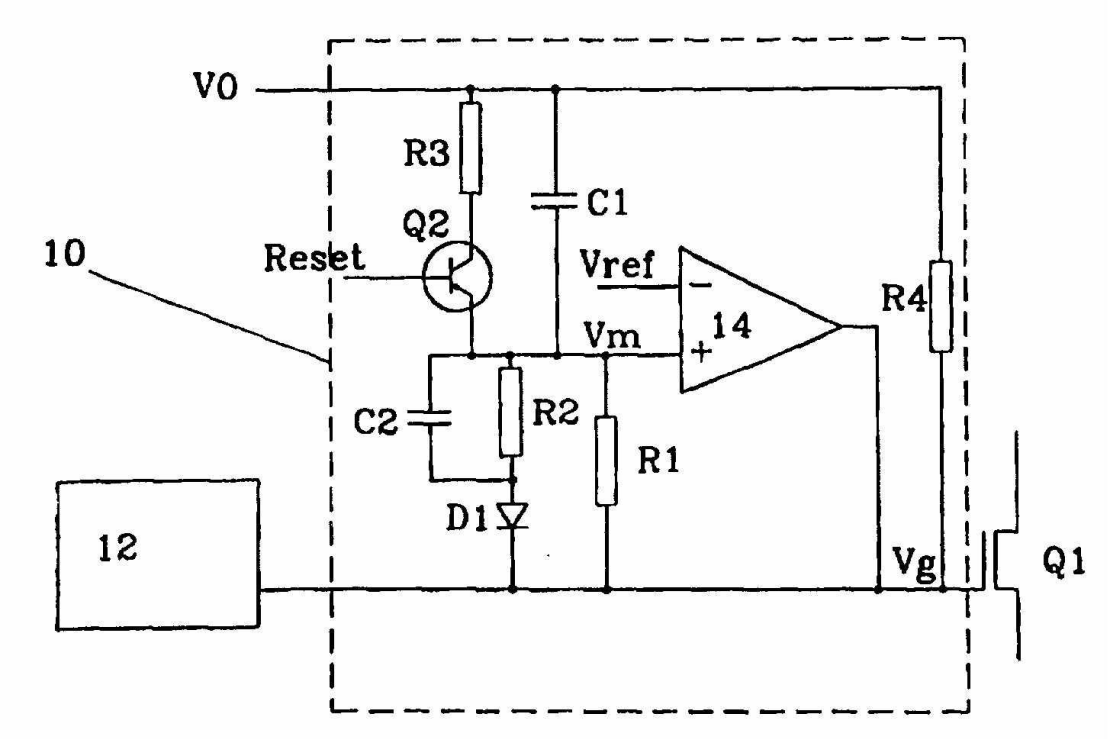


Figure taken from EP0916188

H03K 27/00

Pulse counters in which pulses are continuously circulated in a closed loop; Analogous frequency dividers (feedback shift register counters H03K23/54)

Definition statement

This subclass/group covers:

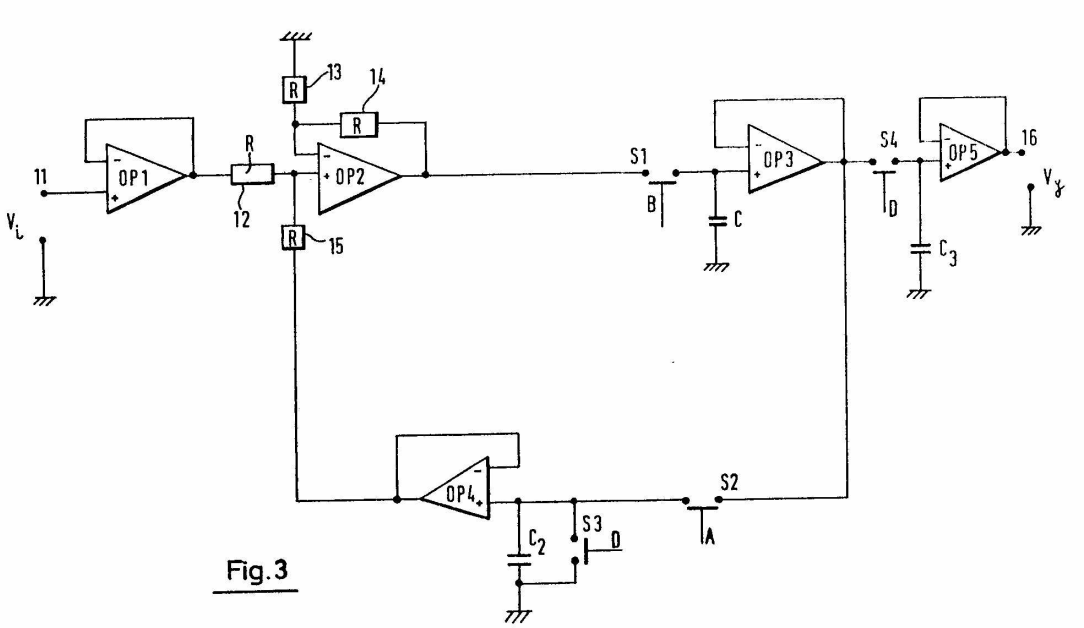


Figure taken from GB2008296.

H03K 29/00

Pulse counters comprising multi-stable elements, e.g. for ternary scale, for decimal scale; Analogous frequency dividers

Definition statement

This subclass/group covers:

A triggering pulse is generated in response to each input signal to be counted. The triggering pulse is applied to the device to change the voltage across the device. The voltage across the device is output as an indication of the number of received input signals. The device may be a resonant tunnelling diode with multiple peaks in its current versus voltage characteristic. The device may be a resonant tunnelling diode with multiple peaks in its current versus voltage characteristic.

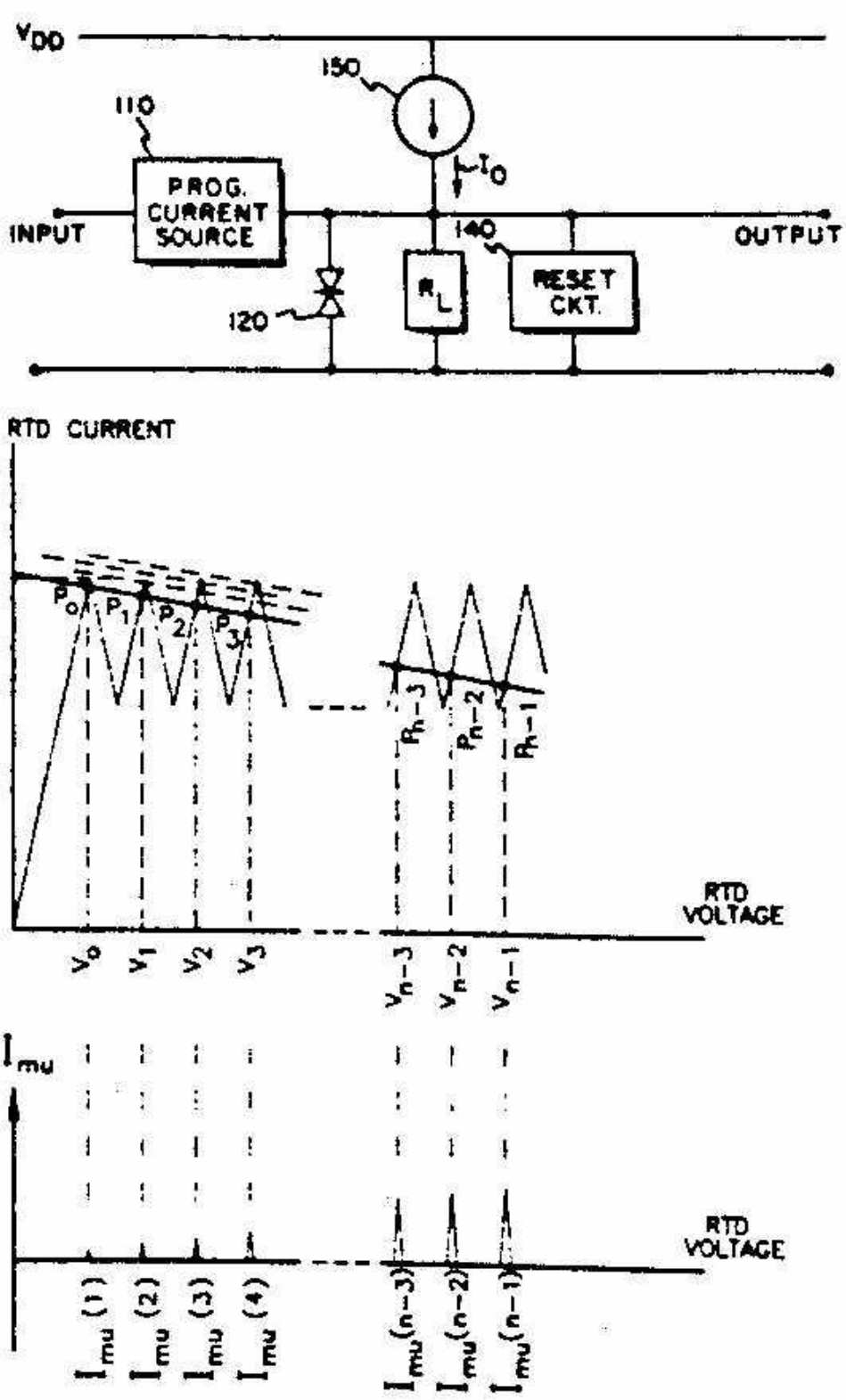


Figure taken from US 5,033,069