G11C

STATIC STORES (information storage based on relative movement between record carrier and transducer G11B; semiconductor devices for storage H01L, e.g. H01L27/108 to H01L27/115; pulse technique in general H03K, e.g. electronic switches H03K17/00; [N: using a static store as a picture recording medium H04N5/907])

Definition statement

This subclass/group covers:

Devices or arrangements for storage of digital or analogue information in which no relative movement takes place between an information storage element and a transducer; which incorporate a selecting-device for writing-in or reading-out the information into or from the store.

References relevant to classification in this subclass

This subclass/group does not cover:

Information storage based on relative movement between record carrier and transducer	G11B
Manufacturing processes	H01L 21/00, H01L 45/00
Semiconductor devices for storage; layout or structure of memory cells or devices at the fabrication level	H01L 23/00, H01L 27/00, H01L 27/108 - H01L 27/115, H01L 29/00
Pulse technique in general, e.g. electronic switches	H03K 17/00
Using a static store as a picture recording medium	H04N 5/907

Solid state disk drives	G06F 3/06E
Record carriers for machines	G06K 19/07

Informative references

Attention is drawn to the following places, which may be of interest for search:

Accessing or allocating memory in electronic computers	G06F 12/00

Special rules of classification within this subclass

In this sub-class there exist three general main groups, G11C 5/00, G11C 7/00 and G11C 8/00, which cover aspects such as power supply, reading and writing arrangements and addressing arrangements that are common to many if not all types of memories. There are further main groups which are dedicated to one or more specific types of memory cell technologies. Within these, there may be specific sub-groups for aspects such as power supply or addressing which parallel the general groups. The convention is that, where a document describes a specific aspect for a specific cell technology without indicating its use with other cell types, it should only be classified under the technology group. If it is described as applicable to two cell types then it should be classified under each cell type and in the general group. Thus, for example, a sense amplifier for a resistive RAM would be classified under G11C 13/004, while a document applying the same sense amplifier to both ReRAM and flash memory would be further classified in G11C 16/26 and G11C 7/06.

G11C 29/00 is a further general group covering the aspects of testing and repair of memory devices. There are no cell-type specific sub-groups for these aspects and thus they are only classified in this place. However other aspects also covered in testing documents will be classified according to the rules of the previous paragraph.

Glossary of terms

In this subclass/group, the following terms (or expressions) are used with the meaning indicated:

2D/3D	two/three dimensional
Storage element	an element which can hold at least one item of information and is provided with means for writing-in or reading-out this information
Memory	a device, including storage elements, which can hold information to be extracted when desired.

Synonyms and Keywords

In patent documents the following abbreviations are often used:

ATD	Address transition detection
RAM	Random Access Memory
DRAM	Dynamic RAM
FRAM, FeRAM	Ferro-electric RAM
MRAM	Magnetic RAM
NVRAM	Nonvolatile RAM
PCRAM, PRAM	Phase-change RAM
RRAM, ReRAM	Resistive RAM
SRAM	Static RAM
ROM	Read-only Memory
PROM	Programmable ROM
EPROM	Erasable PROM
EEPROM, E2PROM	Electrically-erasable PROM
EAROM	Electrically-alterable ROM

G11C 5/00

Details of stores covered by G11C11/00

Definition statement

This subclass/group covers:

Details of arrangements providing supporting functions for semiconductor memory devices, concerning protection against loss of information, memory layout and stacking, signal line and power line interconnection, memory modules and their electrical interconnections, and power supplies including backup supplies, as well as charge pumps, voltage and current reference generators as well as circuits for stabilization of voltages and currents, which are common to all semiconductor memories types covered by subclass G11C,

as detailed in main groups G11C 13/00, G11C 14/00, G11C 16/00, G11C 17/00, G11C 19/00, G11C 21/00, G11C 23/00, G11C 25/00, G11C 27/00 as well as G11C 11/00.

Relationship between large subject matter areas

This group covers the above mentioned aspects only when they are concerned with a semiconductor memory.

Furthermore, in the case where any of the above mentioned aspects are adapted to be used with a semiconductor memory of a specific type, such aspects should be classified in the relevant group covering that specific type of semiconductor device, as long as such a specific group is present.

References relevant to classification in this group

This subclass/group does not cover:

Power supplies, reference generators or voltage pumps in general not being concerned with semiconductor memories.	G05F, H02J, H02M
Circuit means for protection against loss of information in general having no connection to semiconductor memories.	H01L 21/26, G06F 11/00
Geometrical lay-out of the components in integrated circuits not concerned with semiconductor memories.	H01L 27/0207
Mechanical aspects of memory modules, supports and cards	H05K 5/02, H01L 25/00

Examples of places where the subject matter of this group is covered when specially adapted, used for a particular purpose, or incorporated in a larger system:

Protection means for ferromagnetic memories	G11C 11/1695
Power supply arrangements for ferromagnetic memories	G11C 11/1697
Protection means for ferroelectric memories	G11C 11/2295

Power supply arrangements for ferroelectric memories	G11C 11/2297
Means for protection concerning static memory cells (SRAM)	G11C 11/4125
Means for protection concerning static memory storage device (SRAM)	G11C 11/41355
Power supply arrangements for SRAMs	G11C 11/41357

Special rules of classification within this group

If documents are clearly restricted to one specific cell type or memory technology they should not be classified here but in the group of said cell technology, unless there is no group for that cell technology. If documents mention applications to different types of cells then they can be classified here.

G11C 5/025

[N: Geometric lay-out considerations of storage- and peripheral-blocks in a semiconductor storage device (geometrical lay-out of the components in integrated circuits, H01L27/0207)]

Definition statement

This subclass/group covers:

Geometrical layout considerations of the internal components of a memory device.

References relevant to classification in this group

This subclass/group does not cover:

Geometrical lay-out of the components in integrated circuits	H01L 27/0207

Special rules of classification within this group

Layout considerations on a printed circuit board are covered by H05K 1/18.

G11C 5/04

Supports for storage elements, Supports for storage elements, [N: e.g. memory modules]; Mounting or fixing of storage elements on such supports

Definition statement

This subclass/group covers:

Electrical aspects of memory modules such as e.g. SIMM, DIMM or flash memories.

G11C 5/143

[N: Detection of memory cassette insertion/removal; Continuity checks of supply and ground lines (in general G01R31/02); Detection of supply variations/ interruptions/ levels (G11C5/148 takes precedence); Switching between alternative supplies (back-up supplies per se H02J9/061), (G11C5/141 takes precedence)]

Definition statement

This subclass/group covers:

Covering the detection of change in supply voltage, on the voltage or the ground side, in general.

References relevant to classification in this group

This subclass/group does not cover:

Details of power up or power down circuits, standby circuits or recovery circuits	G11C 5/148
Battery and back-up supplies	G11C 5/141
Back-up supplies per se	H02J 9/061
Testing of electric apparatus, lines or components, for short-circuits, discontinuities, leakage	G01R 31/02

G11C 5/144

[N: Detection of predetermined disconnection or reduction of power supply, e.g. power down or power standby]

Definition statement

This subclass/group covers:

Voluntary power down or standby arrangements.

G11C 5/148

[N: Details of power up or power down circuits, standby circuits or recovery circuits

Definition statement

This subclass/group covers:

Covering the characteristics of the power up and power down circuits, the standby circuits and recovery circuits.

G11C 7/00

Arrangements for writing information into, or reading information out from, a digital store (G11C5/00 takes precedence; auxiliary circuits for stores using semiconductor devices G11C11/4063, G11C11/413, G11C11/4193)

Definition statement

This subclass/group covers:

All aspects of reading and writing of data to an address memory cell in general except the addressing of the cell. The addressing and row circuitry is covered in G11C 8/00. G11C 7/00IS more about column and input/output circuitry "In general" means that technology or cell specific documents are not covered here but in their respective groups.

References relevant to classification in this group

This subclass/group does not cover:

Encryption, data protection	G06F 1/00N, G06F 12/00
Higher level memory space management, free space management, garbage collection, cache memories	G06F 12/00
External memory control circuits, buses, bus protocols, DMA, memory	G06F 13/16

controllers	
Specific cell types of technologies	G11C 11/00 G11C 17/00
Details of stores	G11C 5/00
Auxiliary circuits for stores using semiconductor devices	G11C 11/4063, G11C 11/413

Examples of places where the subject matter of this group is covered when specially adapted, used for a particular purpose, or incorporated in a larger system:

Reading and writing arrangements for specific cell types	G11C 11/00 - G11C 17/00

Early solid state music players	G11C 7/16

Informative references

Attention is drawn to the following places, which may be of interest for search:

Security aspects, encryption	G06F 1/00N
External data synchronisation during read or write	G06F 13/16
Calibration	G06F 13/16, G11C 29/00
Auxiliary circuits, e.g. for addressing, decoding, driving, writing, sensing or timing	G11C 11/4063
Auxiliary circuits, e.g. for addressing, decoding, driving, writing, sensing, timing, power reduction	G11C 11/413
Amplifiers in general	H03F
Basic logic circuits, latches and flip-flops	H03K

Delays	H03K 5/00
PLL, DLL circuits per se	H03L
Synchronisation	H04L 7/00

Special rules of classification within this group

If documents are clearly restricted to one specific cell type or memory technology they should not be classified here but in the group of said cell technology, unless there is no group for that cell technology. If documents mention applications to different types of cells then they can be classified here.

G11C 7/02

with means for avoiding parasitic signals

Informative references

Attention is drawn to the following places, which may be of interest for search:

Bit lines or layout aspects	G11C 5/025, G11C 7/12, G11C 7/18
Power supply arrangements	G11C 5/14

G11C 7/04

with means for avoiding disturbances due to temperature effects

Special rules of classification within this group

If refresh is concerned G11C 11/406 takes precedence.

G11C 7/062

[N: Differential amplifiers of non-latching type, e.g. comparators, long-tailed pairs]

Definition statement

This subclass/group covers:

Most of the current sense amplifiers (current mirrors based) and most of the multi stage sense amplifiers.

G11C 7/08

Control thereof

Special rules of classification within this group

This is a recent group and most of the material about the control of sense amplifiers in general and about sense amplifier drivers is in G11C 7/06.

G11C 7/10

Input/output (I/0) data interface arrangements, e.g. I/O data control circuits, I/O data buffers (level conversion circuits in general H03K19/0175)

Definition statement

This subclass/group covers:

Input/output (I/0) data interface arrangements.

Covers all the synchronous memory data interfaces (Synclink, SDR, DDR, Rambus).

References relevant to classification in this group

This subclass/group does not cover:

Level conversion circuits in general	H03K 19/0175

Special rules of classification within this group

Serial interfaces (IC2, SPI, single wire) when applied to memories are mainly classified in G11C 5/066. Buses with Ring topologies (daisy chain or peer-to-peer buses) for memories are also covered in G11C 7/10, G11C 7/1051 and G11C 7/1078. Documents where the memory controller is the main aspect are in the G06F 13/16 groups. Data buses and bus protocols in general are in G06F 13/00.

G11C 7/1006

[N: Data managing, e.g. manipulating data before writing or reading out, data bus switches or control circuits therefor]

Definition statement

This subclass/group covers:

In particular:

- Data masking;
- Memories incorporating some form of processing capability from logic function and simple ALUs to memories embedded with a CPU (cache memories are in G06F 12/0802);
- "Sophisticated" data routing, reordering (X-bars).

It also contains sometimes memories with ECC circuits. However these should be searched and classified in G06F 11/10M2.

G11C 7/1039

[N: using pipelining techniques, i.e. using latches between functional memory parts, e.g. row/column decoders, I/O buffers, sense amplifiers]

Definition statement

This subclass/group covers:

The pipelining in clock synchronous and wave pipelining in clockless (asynchronous) memories.

Informative references

Attention is drawn to the following places, which may be of interest for search:

Power supply arrangements for memories with random access ports synchronised on clock signal pulse trains	G11C 7/1072

G11C 7/1042

[N: using interleaving techniques, i.e. read-write of one part of the memory while preparing another part]

Special rules of classification within this group

"Interleaving" when referring to a bit line layout is classified in G11C 7/18.

G11C 7/1045

[N: Read-write mode select circuits]

Definition statement

This subclass/group covers:

Mode setting registers and bonding pads.

Informative references

Attention is drawn to the following places, which may be of interest for search:

Redundancy; Test mode entry	G11C 29/00

G11C 7/1048

[N: Data bus control circuits, e.g. precharging, presetting, equalising]

Special rules of classification within this group

Also some on die termination (ODT) documents which are unfortunately spread over three groups G11C 7/1048, G11C 7/1051 and G11C 5/06, where they are now classified.

G11C 7/1051

[N: Data output circuits, e.g. read-out amplifiers, data output buffers, data output registers, data output level conversion circuits]

Definition statement

This subclass/group covers:

Together with G11C 7/1078, most of the synchronous interfaces documents.

G11C 7/1072

[N: for memories with random access ports synchronised on clock signal pulse trains, e.g. synchronous memories, self timed memories]

Definition statement

This subclass/group covers:

Many early SDRAMs but became rapidly obsolete as most dynamic memories are now synchronous.

G11C 7/1075

[N: for multiport memories each having random access ports and serial ports, e.g. video RAM]

Informative references

Attention is drawn to the following places, which may be of interest for search:

Multiport cells	G11C 8/16

G11C 7/1078

[N: Data input circuits, e.g. write amplifiers, data input buffers, data input registers, data input level conversion circuits]

Definition statement

This subclass/group covers:

Together with G11C 7/1051, most of the synchronous interfaces documents.

G11C 7/16

Storage of analogue signals in digital stores using an arrangement comprising analogue/digital (A/D) converters, digital memories and digital/analogue (D/A) converters

Definition statement

This subclass/group covers:

Also many early solid state music players and early solid state memory cards (e.g. Compact Flash, SDcard).These should not be classified here but in G11B, G06F and G06K.

G11C 7/22

Read-write (R-W) timing or clocking circuits; Read-write (R-W) control signal generators or management

Definition statement

This subclass/group covers:

- All the clock generating circuits (PLL, DLL, delay lines, oscillators),
- Overall control of memory operation (delay chains, state machines...) and memory operation mode/state, and
- Control aspects of specific parts of the memory which are not covered in other G11C 5/00, G11C 7/00 and G11C 8/00 groups.

Glossary of terms

In this subclass/group, the following terms (or expressions) are used with the meaning indicated:

Dummy cell	cell that is not used for storage but to provide a reference voltage or current during sensing
Embedded	memories which are designed to be incorporated on the same die as a microcontroller/processor usually in ASICs or System on a Chip circuits - not cache memories
Burst	Read or Write cycle during which a series of 2, 4, 8 or more external data are sequentially input to or output from the memory device
Precharge	to prepare the memory for a subsequent read operation (or a write operation) by charging bit lines and/or word lines to a certain voltage

Synonyms and keywords

In patent documents the following abbreviations are often used:

DPD	Deep Power Down
DLL	Delay locked loop
EDO	extended data output
I/O	Input/Output
LCD	Liquid Crystal Display

ODT	On Die Termination
PLL	Phase locked loop
SA	Sense Amplifier

In patent documents the following expressions/words are often used as synonyms.

"Bit line", "digit line" and "signal line"

"I/O line" and "data line"

"Reference cell" and "dummy cell".

G11C 8/00

Arrangements for selecting an address in a digital store (for stores using transistors G11C11/407, G11C11/413; [N: switching or gating circuits for general use H03K17/00])

Definition statement

This subclass/group covers:

Circuitry used for decoding a memory address selecting a row line, a bank , a block or a range of memory cells in a semiconductor memory device.

References relevant to classification in this group

This subclass/group does not cover:

Addressing schemes, architectures or methods, e.g. virtual addressing or multidimensional addressing	G06F 12/00
Address mapping	G06F 12/02
For memory cells of the field-effect type	G11C 11/407
Auxiliary circuits, e.g. for addressing, decoding, driving, writing, sensing, timing, power reduction	G11C 11/413
Shift registers in general, FIFO, LIFO	G11C 19/08, G06F 5/06

Switching or gating circuits for general use	H03K 17/00
Encoding or decoding method per se	H03M 7/00

Examples of places where the subject matter of this group is covered when specially adapted, used for a particular purpose, or incorporated in a larger system:

Particular aspects concerning addressing MRAM (ferromagnetic) devices	G11C 11/1653
Particular aspects concerning addressing FRAM (ferroelectric) devices	G11C 11/2253
Particular aspects concerning addressing DRAM (dynamic RAM) devices	G11C 11/408
Particular aspects concerning addressing SRAM (static RAM) devices	G11C 11/41313
Particular aspects concerning addressing memory devices having resistive memory elements	G11C 13/0023
Particular aspects concerning addressing circuits of EPROM, EAROM, EEPROM devices or other devices having charge storing memory elements	G11C 16/08
Contact or connection structure for RAS/CAS addressing pins/lines	G11C 5/066
Circuits selecting Bit lines or data latchs (I/O, input-ouput)	G11C 7/10
Multiport memory using "single port cells", i.e where the multiport ability it created e.g. in the I/O circuitry.	G11C 7/1075

Special rules of classification within this group

If documents are clearly restricted to one specific cell type or memory technology they should not be classified here but in the group of said cell technology, unless there is no group for that cell technology. If documents mention applications to different types of cells then they can be classified here.

G11C 8/08

Word line control circuits, e.g. drivers, boosters, pull-up circuits, pull-down circuits, precharging circuits, for word lines

Definition statement

This subclass/group covers:

Circuitries that have an electrical effect on the rows or word lines. e.g. applying a voltage or a potential to the word line or row.

G11C 8/10

Decoders

Definition statement

This subclass/group covers:

Decoders, circuitry which processes the address information to make a single or plural selection of word line or row line possible. However, these decoder circuits are usually not used for the electrical activation of the row or word line. This is the task of the word line control circuits.

References relevant to classification in this group

This subclass/group does not cover:

Address mapping per se	G06F 12/02

G11C 8/14

Word line organisation; Word line lay-out

Definition statement

This subclass/group covers:

In particular, global and local word line structure.

G11C 8/16

Multiple access memory array, e.g. addressing one storage element via at least independent addressing line groups [N: (multiport memories in general G11C7/1075)]

Definition statement

This subclass/group covers:

Only documents describing memories where each storage cell on its own has two or more ports.

References relevant to classification in this group

This subclass/group does not cover:

Multiport memories in general	G11C 7/1075

G11C 8/18

Address timing or clocking circuits; Address control signal generation or management, e.g. for row address strobe (RAS) or column address strobe (CAS) signals

Informative references

Attention is drawn to the following places, which may be of interest for search:

Physical realization of a corresponding interface	G11C 5/066

Synonyms and Keywords

In patent documents the following expressions/words "row" and "word line" are often used as synonyms.

G11C 11/00

Digital stores characterised by the use of particular electric or magnetic storage elements; Storage elements therefor (G11C14/00 to G11C21/00 take precedence)

Definition statement

This subclass/group covers:

- DRAM (Dynamic RAM), see G11C 11/401 to G11C 11/4099
- FRAM, FeRAM (Ferro-electric RAM) see G11C 11/22
- MRAM (Magnetic RAM) see G11C 11/14 to G11C 11/16
- SRAM (Static RAM) see G11C 11/41 to G11C 11/419
- Multi-level storage, using storage elements with more than two stable states represented by steps, e.g. of voltage, current, phase, frequency, see G11C 11/56.

References relevant to classification in this group

This subclass/group does not cover:

EPROM (Erasable PROM) EEPROM, E2PROM (Electrically-erasable PROM) EAROM (Electrically-alterable ROM) Flash memory	G11C 16/00 - G11C 16/349
RRAM, ReRAM (Resistive RAM)	G11C 13/0002 - G11C 13/00R53B
PCRAM, PRAM (Phase-change RAM)	G11C 13/0004
Digital stores characterised by arrangements of cells having volatile and non-volatile storage properties for back-up when the power is down	G11C 14/00
Digital stores in which information comprising one or more characteristic parts is written into the store and in which information is read-out by searching for one or more of these characteristic parts, i.e. associative or content-addressed stores	G11C 15/00
Erasable programmable read-only memories	G11C 16/00
Read-only memories programmable only once; Semi-permanent stores, e.g. manually-replaceable information cards	G11C 17/00
ROM (Read-only Memory)	G11C 17/02 - G11C 17/126

PROM (Programmable ROM)	G11C 17/14 - G11C 17/18
Digital stores in which the information is moved stepwise, e.g. shift register	G11C 19/00
Digital stores in which the information circulates	G11C 21/00
General aspects of testing.	G11C 29/00
General aspects of redundancy management.	G11C 29/00R
General aspects of power supplies, charge pumps, voltage references and battery backup.	G11C 5/00
NVRAM Nonvolatile battery backed up RAM	G11C 5/141
General aspects of input/output selection, read and write circuitry.	G11C 7/00
General aspects of address decoding and word line selection.	G11C 8/00

Informative references

Attention is drawn to the following places, which may be of interest for search:

Sensors	G01R 33/00

Special rules of classification within this group

G11C 11/56 takes precedence over sub-groups G11C 11/02 to G11C 11/54.

The sub-group classification G11C 11/34 is not to be assigned as there exist more specific places for different cell types.

Glossary of terms

In this subclass/group, the following terms (or expressions) are used with the meaning indicated:

In this group, the following expression is used with the meaning indicated:

2D	two dimensional

Synonyms and Keywords

In patent documents the following abbreviations are often used:

AFM	Antiferromagnetic
CPP	Current Perpendicular to Plane
FeFET	Ferro-electric Field Effect Transistor
FM	Ferromagnetic
GMR	Giant Magnetic Resistive
MTJ	Magnetic Tunnel Junction
SAF	Synthetic Antiferromagnetic

G11C 11/005

[N: comprising combined but independently operative RAM-ROM, RAM-PROM, RAM-EPROM cells]

Definition statement

This subclass/group covers:

Memories having two distinct arrays of memory elements, one with volatile memory elements and another one with non-volatile memory elements, the latter functioning as a backup memory for the volatile part of the memory.

Informative references

Attention is drawn to the following places, which may be of interest for search:

Memories having two types of memory cells or memory elements merged to each other or otherwise combined in the same memory array	G11C 14/00

G11C 11/02

using magnetic elements [N: (using multibit magnetic storage elements G11C11/5607; counters with magnetic elements H03K23/76; pulse generators, static switches, logic circuits with such elements H03K3/45, H03K17/80, H03K19/16; measurement of magnetic variables G01R33/00)]

Informative references

Attention is drawn to the following places, which may be of interest for search:

Measurement of magnetic variables	G01R 33/00
Multibit magnetic storage elements	G11C 11/5607
Counters with magnetic elements	H03K 23/76
Pulse generators, static switches, logic circuits with such elements	H03K 3/45, H03K 17/80 ,H03K 19/16

G11C 11/04

using rod-type storage elements [N: contains no documents; see G11C11/06085, G11C11/14, G11C11/155]

Special rules of classification within this group

Contains no documents; see G11C 11/06085, G11C 11/14, G11C 11/155 instead.

G11C 11/06

using single-aperture storage elements, e.g. ring core; using multi-aperture plates in which each individual aperture forms a storage element

Definition statement

This subclass/group covers:

Also the (now obsolete) magnetic-core memories.

G11C 11/14

using thin-film elements

Definition statement

This subclass/group covers:

Memories using a single magnetic layer.

Memories using domain wall displacement in a shift register like manner, see also G11C 19/0833.

Informative references

Attention is drawn to the following places, which may be of interest for search:

Magnetic thin film layers per se	H01F 10/00
Manufacturing of a magnetic memory	H01L 21/8246M

G11C 11/15

using multiple magnetic layers (G11C11/155 takes precedence)

Definition statement

This subclass/group covers:

Memories using multiple magnetic layers not using any spin effect.

References relevant to classification in this group

This subclass/group does not cover:

With cylindrical configuration	G11C 11/155

G11C 11/16

using elements in which the storage effect is based on magnetic spin effect [N: (sensors using magnetoresistive multilayer structures G01R33/093; thin layer magnetic read heads for magnetic discs G11B5/31; non-reciprocal magnetic elements in waveguides H01P; composition of ferromagnetic material H01F1/00; gyrators H03H7/002)]

Definition statement

This subclass/group covers:

Memories using magnetic spin effect, i.e. where the memory elements have magnetic tunnel junctions.

References relevant to classification in this group

This subclass/group does not cover:

Sensors using magnetoresistive multilayer structures	G01R 33/093
Thin layer magnetic read heads for magnetic discs	G11B 5/31
Non-reciprocal magnetic elements in waveguides	H01P
Composition of ferromagnetic material	H01F 1/00
Gyrators	H03H 7/002

Informative references

Attention is drawn to the following places, which may be of interest for search:

Spin-exchange coupled multilayers per se	H01F 10/32
Memory structures	H01L 27/22
Manufacturing of magnetic memory	H01L 21/8246M

G11C 11/165

[N: Auxiliary circuits]

Definition statement

This subclass/group covers:

Auxiliary circuitry for MRAM elements.

Informative references

Attention is drawn to the following places, which may be of interest for search:

Details of stores	G11C 5/00
Arrangements for writing information into, or reading information out from, a digital store	G11C 7/00
Arrangements for selecting an address in a digital store	G11C 8/00

G11C 11/1653

[N: Address circuits or decoders]

Informative references

Attention is drawn to the following places, which may be of interest for search:

Arrangements for selecting an address in a digital store	G11C 8/00

G11C 11/1655

[N: Bit-line or column circuits]

Informative references

Attention is drawn to the following places, which may be of interest for search:

Bit line control circuits, e.g. drivers, boosters, pull-up circuits, pull-down circuits, precharging circuits, equalising circuits, for bit lines	G11C 7/12
Bit line organisation; Bit line lay-out	G11C 7/18

G11C 11/1657

[N: Word-line or row circuits]

Informative references

Attention is drawn to the following places, which may be of interest for search:

Word line control circuits	G11C 8/08
Word line organisation; Word line lay-out	G11C 8/14

G11C 11/1659

[N: Cell access]

Definition statement

This subclass/group covers:

MRAM specific details of selecting a memory element, e.g. select transistors, diodes or mere word line or bit line selection voltages.

G11C 11/1673

[N: Reading or sensing circuits or methods]

Informative references

Attention is drawn to the following places, which may be of interest for search:

Sense amplifiers; Associated circuits	G11C 7/06
Data output circuits, e.g. read-out amplifiers, data output buffers, data output registers, data output level conversion circuits	G11C 7/1051

G11C 11/1675

[N: Writing or programming circuits or methods]

Informative references

Attention is drawn to the following places, which may be of interest for search:

Data input circuits, e.g. write amplifiers, data input buffers, data input registers, data input level conversion circuits	G11C 7/1078

G11C 11/1677

[N: Verifying circuits or methods]

Definition statement

This subclass/group covers:
Details of checking written data in MRAM elements.

G11C 11/1693

[N: Timing circuits or methods]

Informative references

Attention is drawn to the following places, which may be of interest for search:

Read-write (R-W) timing or clocking circuits; Read-write (R-W) control signal generators or management	G11C 7/22
Address timing or clocking circuits; Address control signal generation or management, e.g. for row address strobe (RAS) or column address strobe (CAS) signals	G11C 8/18

G11C 11/1695

[N: Protection circuits or methods]

Informative references

Attention is drawn to the following places, which may be of interest for search:

Memory cell safety or protection circuits, e.g. arrangements for preventing inadvertent reading or writing; Status cells; Test cells	G11C 7/24
Address safety or protection circuits, i.e. arrangements for preventing unauthorised or accidental access	G11C 8/20

G11C 11/1697

[N: Power supply circuits]

Informative references

Attention is drawn to the following places, which may be of interest for search:

Power supply arrangements	G11C 5/14

G11C 11/22

using ferroelectric elements [N: (using multibit ferroelectric storage elements G11C11/5657; pulse generators using ferroelectric elements H03K3/45; counters using such elements H03K23/76)]

Definition statement

This subclass/group covers:

Memories using ferroelectric elements. This covers memories with capacitive elements where the insulating dielectric material between the capacitor plates is a ferroelectric material.

References relevant to classification in this group

This subclass/group does not cover:

Using multibit ferroelectric storage	G11C 11/5657
Pulse generators using ferroelectric elements	H03K 3/45
Counters using such elements	H03K 23/76

Informative references

Attention is drawn to the following places, which may be of interest for search:

Ferroelectric capacitors per se	H01G 1/00
Ferroelectric materials	H01G 4/12
Memory structures	H01L 27/11502, H01L 27/11585

Manufacturing of ferroelectric memories	H01L 29/516

G11C 11/221

[N: using ferroelectric capacitors]

Definition statement

This subclass/group covers:

Details of FRAM memory elements comprising a ferroelectric capacitor.

G11C 11/223

[N: using MOS with ferroelectric gate insulating film]

Definition statement

This subclass/group covers:

Details of FRAM memory elements comprising a transistor with ferroelectric material, e.g. a FEFET.

G11C 11/225

[N: Auxiliary circuits]

Definition statement

This subclass/group covers:

Auxiliary circuitry for FRAM elements.

Informative references

Attention is drawn to the following places, which may be of interest for search:

Details of stores	G11C 5/00
Arrangements for writing information into, or reading information out from, a digital store	G11C 7/00
Arrangements for selecting an address in a digital store	G11C 8/00

G11C 11/2253

[N: Address circuits or decoders]

Informative references

Attention is drawn to the following places, which may be of interest for search:

Arrangements for selecting an address in a digital store	G11C 8/00

G11C 11/2255

[N: Bit-line or column circuits]

Informative references

Attention is drawn to the following places, which may be of interest for search:

Bit line control circuits, e.g. drivers, boosters, pull-up circuits, pull-down circuits, precharging circuits, equalising circuits, for bit lines	G11C 7/12
Bit line organisation; Bit line lay-out	G11C 7/18

G11C 11/2257

[N: Word-line or row circuits]

Informative references

Attention is drawn to the following places, which may be of interest for search:

Word line control circuits, e.g. drivers, boosters, pull-up circuits, pull-down circuits, precharging circuits, for word lines	G11C 8/08
Word line organisation; Word line lay-out	G11C 8/14

G11C 11/2259

[N: Cell access]

Definition statement

This subclass/group covers:

FRAM specific details of selecting a memory element, e.g. select transistors, diodes or mere word line or bit line selection voltages.

G11C 11/2273

[N: Reading or sensing circuits or methods]

Informative references

Attention is drawn to the following places, which may be of interest for search:

Sense amplifiers; Associated circuits	G11C 7/06
Data output circuits, e.g. read-out amplifiers, data output buffers, data output registers, data output level conversion circuits.	G11C 7/1051

G11C 11/2275

[N: Writing or programming circuits or methods]

Informative references

Attention is drawn to the following places, which may be of interest for search:

Data input circuits, e.g. write amplifiers, data input buffers, data input registers, data input level conversion circuits	G11C 7/1078

G11C 11/2277

[N: Verifying circuits or methods]

Definition statement

This subclass/group covers:

Details of checking written data in MRAM elements.

G11C 11/2293

[N: Timing circuits or methods]

Informative references

Attention is drawn to the following places, which may be of interest for search:

Read-write (R-W) timing or clocking circuits; Read-write (R-W) control signal generators or managemen	G11C 7/22
Address timing or clocking circuits; Address control signal generation or management, e.g. for row address strobe (RAS) or column address strobe (CAS) signals	G11C 8/18

G11C 11/2295

[N: Protection circuits or methods]

Informative references

Attention is drawn to the following places, which may be of interest for search:

Memory cell safety or protection circuits, e.g. arrangements for preventing inadvertent reading or writing; Status cells; Test cells.	G11C 7/24
Address safety or protection circuits, i.e. arrangements for preventing unauthorised or accidental access.	G11C 8/20

G11C 11/2297

[N: Power supply circuits]

Informative references

Attention is drawn to the following places, which may be of interest for search:

Power supply arrangements	G11C 5/14

G11C 11/34

using semiconductor devices [N: (processes or apparatus for the manufacture or treatment of semiconductor or solid state devices H01L21/00; integrated circuit devices H01L27/00; generating electric pulses, e.g. bistable devices using semiconductor devices H03K3/00)]

Informative references

Attention is drawn to the following places, which may be of interest for search:

Processes or apparatus for the manufacture or treatment of semiconductor or solid state devices	H01L 21/00
Integrated circuit devices	H01L 27/00
Generating electric pulses, e.g. bistable devices using semiconductor devices	H03K 3/00

Special rules of classification within this group

Documents should not be classified in this group unless there is no more specific place available below or in G11C 14/00 to G11C 21/00 (see precedence rule at beginning of this main group). e.g., for:

DRAM (Dynamic RAM), see G11C 11/401 to G11C 11/4099

FRAM, FeRAM (Ferro-electric RAM) see G11C 11/22

MRAM (Magnetic RAM) see G11C 11/14 to G11C 11/16

NVRAM (Nonvolatile RAM) see G11C 5/141 (battery backed RAM) or G11C 16/00 (EAROM/EEPROM/Flash memory)

PCRAM, PRAM (Phase-change RAM) see G11C 13/0004

RRAM, ReRAM (Resistive RAM) see G11C 13/0002 to G11C 13/00R53B

SRAM (Static RAM) see G11C 11/41 to G11C 11/419

ROM (Read-only Memory) see G11C 17/02 to G11C 17/126

PROM (Programmable ROM) see G11C 17/14 to G11C 17/18

EPROM (Erasable PROM) see G11C 16/00 to G11C 16/349

EEPROM, E2PROM (Electrically-erasable PROM) see G11C 16/00 to G11C 16/349

EAROM (Electrically-alterable ROM) see G11C 16/00 to G11C 16/349

G11C 11/401

forming cells needing refreshing or charge regeneration, [N: i.e. dynamic cells]

Definition statement

This subclass/group covers:

Basically this group covers DRAMs - and some further types of cells needing to be periodically and frequently refreshed such gain cells.

This group and its sub groups concerns mainly DRAM cells of any type from classic one transistor-one capacitor cell types to more exotic types such single transistor cells or gain cells. All cells have in common that they require to be updated or rewritten or refreshed frequently in order to retain their data.

References relevant to classification in this group

This subclass/group does not cover:

The much less frequent refreshing or updating of data in non-volatile memories	G11C 16/3418, G11C 13/0021
Ferro-electric RAMs or FeRAMs	G11C 11/22
Fabrication, integration, layout of DRAM cells	H01L 27/108

Examples of places where the subject matter of this group is covered when specially adapted, used for a particular purpose, or incorporated in a larger system:

Control of displays, e.g. graphic cards	G09G

Special rules of classification within this group

This is a technology or cell type specific group and only DRAMs and memories needing frequent refreshes should be classified here. FeRAM with a dynamic mode should be classified in G11C 11/22.

G11C 11/404

with one charge-transfer gate, e.g. MOS transistor, per cell

Definition statement

This subclass/group covers:

Mostly 1T1C cells but single transistor cells are also found here (see also G11C 2211/4016 for SOI and isolated well single transistor cells).

G11C 11/405

with three charge-transfer gates, e.g. MOS transistors, per cell

Definition statement

This subclass/group covers:

Cells with three charge-transfer gates, but it also contains gain cells and other cells with access transistors combined with another charge storage transistor. Finally, it covers also partially capacitor based cells with two access transistors and those with more than 3 access transistors (multiport DRAM cells see also G11C 8/16).

G11C 11/4072

Circuits or initialisation, powering up or down, clearing memory or presetting

Informative references

Attention is drawn to the following places, which may be of interest for search:

Initialisation circuits in general	G11C 7/20

G11C 11/4074

Power supply or voltage generation circuits, e.g. bias voltage generators, substrate voltage generators, back-up power, power control circuits

Definition statement

This subclass/group covers:

All the power supply or voltage generation circuits, e.g. bias voltage generators, substrate voltage generators, back-up power, power control circuits specific to DRAM - see also G11C 5/14-G11C 5/147 for memory

power circuits in general; see also G11C 11/4076 and G11C 7/22 for some power management aspects (changing memory state or mode and DPD e.g. deep power down wake-ups) and G11C 11/406 for the refresh aspects in low power mode (self-refresh).

The group contains also most of the documents concerning cells with a controlled back plate and back plate voltage circuits.

G11C 11/4076

Timing circuits (for regeneration management G11C11/406)

References relevant to classification in this group

This subclass/group does not cover:

Regeneration management	G11C 11/406

Informative references

Attention is drawn to the following places, which may be of interest for search:

Read-write (R-W) timing or clocking circuits; Read-write (R-W) control signal generators or management	G11C 7/22
For memories with random access ports synchronised on clock signal pulse trains, e.g. synchronous memories, self timed memories	G11C 7/1072
Details of clock generating circuits	G11C 7/222
Clock buffers	G11C 7/225

G11C 11/4078

Safety or protection circuits, e.g. for preventing inadvertent or unauthorised reading or writing; Status cells; Test cells (protection of memory contents during checking or testing G11C29/52)

References relevant to classification in this group

This subclass/group does not cover:

Protection of memory contents during checking or testing	G11C 29/52

Informative references

Attention is drawn to the following places, which may be of interest for search:

Safety or protection circuits in general	G11C 7/24

G11C 11/408

Address circuits

Informative references

Attention is drawn to the following places, which may be of interest for search:

Address circuits in general	G11C 8/00

G11C 11/4082

[N: Address Buffers; level conversion circuits]

Informative references

Attention is drawn to the following places, which may be of interest for search:

Address Buffers	G11C 8/06

G11C 11/4085

[N: Word line control circuits, e.g. word line drivers, - boosters, - pull-up, - pull-down, - precharge]

Informative references

Attention is drawn to the following places, which may be of interest for search:

Word line control circuits in general	G11C 8/08

G11C 11/4087

[N: Address decoders, e.g. bit - or word line decoders; Multiple line decoders]

Informative references

Attention is drawn to the following places, which may be of interest for search:

Address decoders in general	G11C 8/10
Banks	G11C 8/12

G11C 11/4091

Sense or sense/refresh amplifiers, or associated sense circuitry, e.g. for coupled bit-line precharging, equalising or isolating

Definition statement

This subclass/group covers:

Precharging, equalising or isolating circuits for DRAMs are in G11C 11/4094 and in general also in G11C 7/12.

Informative references

Attention is drawn to the following places, which may be of interest for search:

Sense or sense/refresh amplifiers in general	G11C 7/06
Latching type sense amplifiers	G11C 7/065
Control thereof (sense amplifier drivers)	G11C 7/08
Precharging, equalising or isolating circuits for DRAMs	G11C 11/4094
Precharging, equalising or isolating circuits for DRAMs in general	G11C 7/12

G11C 11/4093

Input/output (I/O) data interface arrangements, e.g. data buffers (level conversion circuits in general H03K19/0175)

References relevant to classification in this group

This subclass/group does not cover:

Level conversion circuits in general	H03K 19/0175

Informative references

Attention is drawn to the following places, which may be of interest for search:

Input/output (I/O) data interface arrangements in general	G11C 7/10
All the d ata interface circuits (e.g. Synclink, DDR, Rambus)	G11C 7/10, G11C 7/1051, G11C 7/1078 ,G11C 7/1072.

G11C 11/4094

Bit-line management or control circuits

Informative references

Attention is drawn to the following places, which may be of interest for search:

Bit-line management or control circuits in general	G11C 7/12

G11C 11/4096

Input/output (I/O) data management or control circuits, e.g. reading or writing circuits, I/O drivers, bit-line switches

Informative references

Attention is drawn to the following places, which may be of interest for search:

Input/output (I/O) data management or control circuits in general	G11C 7/1048, G11C 7/1051, G11C 7/1078.

G11C 11/4097

Bit-line organisation, e.g. bit-line layout, folded bit lines

Informative references

Attention is drawn to the following places, which may be of interest for search:

Bit-line organisation in general	G11C 7/18

G11C 11/4099

Dummy cell treatment; Reference voltage generators

Informative references

Attention is drawn to the following places, which may be of interest for search:

Dummy cell treatment and reference voltage generators in general	G11C 7/14

Glossary of terms

In this subclass/group, the following terms (or expressions) are used with the meaning indicated:

1T-1C	One transistor one capacitor cells
Self-refresh	A power saving memory operation mode in which the refreshes its cells autonomously
Auto-refresh	An external signal (from a memory controller usually) triggers the refresh, but the rest of the refresh operation is done by circuitry internal to the memory (refresh address counters etc ...)
Twin cell	Arrangement in which a single datum is stored in two (or more) cells
Gain cell	Cells (usually made of three transistors) in which the charge is stored in a gate electrode of a gain

	transistor (thereby controlling the conductivity of that transistor),
SOI	Silicon on Insulator - often used to make single transistor DRAM cells (or ZRAM)

G11C 11/41

forming [N: static] cells with positive feedback, i.e. cells not needing refreshing or charge regeneration, e.g. bistable multivibrator or Schmitt trigger

Definition statement

This subclass/group covers:

Memories having memory cells with positive feedback or a latch, i.e. a Static RAM or SRAM. This group only covers the aspects of the memory device itself. Manufacturing is covered by H01L 21/8442 and array structures by H01L 27/11.

G11C 11/412

using field-effect transistors only [N: (latent image memory G11C7/20; multi-port cells G11C8/160)]

Definition statement

This subclass/group covers:

This group contains SRAM memory cells per se.

Informative references

Attention is drawn to the following places, which may be of interest for search:

Latent image memory	G11C 7/20
Multi-port cells	G11C 8/16

G11C 11/413

Auxiliary circuits, e.g. for addressing, decoding, driving, writing, sensing, timing, power reduction (in general G11C5/00

to G11C8/00)

Definition statement

This subclass/group covers:

Circuitry providing for power, address decoding, signal control etc. required for the functioning of the SRAM. This group and its dependents cover SRAMs having bipolar as well as FET transistor memory cells.

Informative references

Attention is drawn to the following places, which may be of interest for search:

Auxiliary circuits in general	G11C 5/00, G11C 7/00, G11C 8/00.

G11C 11/44

using super-conductive elements, e.g. cryotron [N: (pulse generators using such elements H03K3/38; counters H03K23/001)]

Definition statement

This subclass/group covers:

Memories using super-conductive elements like squids.

Informative references

Attention is drawn to the following places, which may be of interest for search:

Pulse generators using such elements	H03K 3/38
For counters	H03K 23/001

G11C 11/48

using displaceable coupling elements, e.g. ferromagnetic cores, to produce change between different states of mutual or self-inductance [N: contains no documents; see G11C17/00 and subgroups]

Special rules of classification within this group

This sub-group contains no documents; see G11C 17/00 and subgroups.

G11C 11/54

using elements simulating biological cells, e.g. neuron

Definition statement

This subclass/group covers:

As used in neural networks.

Informative references

Attention is drawn to the following places, which may be of interest for search:

Computer systems based on biological models, e.g. neural networks per se	G06N 3/00
Cells storing analogue weights	G11C 27/00

G11C 11/56

using storage elements with more than two stable states represented by steps, e.g. of voltage, current, phase, frequency (counting arrangements comprising multi-stable elements of this type H03K25/00, H03K29/00)

Definition statement

This subclass/group covers:

Additional aspects relating to the cell type rather than multi-state storage per se should be classified under the relevant cell technology. For counting arrangements comprising multi-stable elements of this type see H03K 25/00, H03K 29/00.

G11C 11/5607

[N: using magnetic storage elements]

Informative references

Attention is drawn to the following places, which may be of interest for search:

Magnetic storage per se	G11C 11/02 - G11C 11/18

G11C 11/5614

[N: using conductive bridging RAM [CBRAM] or programming metallization cells [PMC]

Informative referenes

Attention is drawn to the following places, which may be of interest for search:

Comprising conductive bridging RAM [CBRAM] or programming metallization cells [PMCs]	G11C 13/0011

G11C 11/5621

[N: using charge storage in a floating gate]

Informative references

Attention is drawn to the following places, which may be of interest for search:

Comprising cells containing floating gate transistors	G11C 16/0408

G11C 11/5628

[N: Programming or writing circuits; Data input circuits]

Informative references

Attention is drawn to the following places, which may be of interest for search:

Programming or data input circuits	G11C 16/10

G11C 11/5635

[N: Erasing circuits]

Informative references

Attention is drawn to the following places, which may be of interest for search:

Circuits for erasing electrically, e.g. erase voltage switching circuits	G11C 16/14

G11C 11/5642

[N: Sensing or reading circuits; Data output circuits]

Informative references

Attention is drawn to the following places, which may be of interest for search:

Sensing or reading circuits; Data output circuits	G11C 16/26

G11C 11/565

[N: using capacitive charge storage elements]

Informative references

Attention is drawn to the following places, which may be of interest for search:

Forming cells needing refreshing or charge regeneration	G11C 11/401

G11C 11/5657

N: using ferroelectric storage elements]

Informative references

Attention is drawn to the following places, which may be of interest for search:

Using ferroelectric elements	G11C 11/22

G11C 11/5664

[N: using organic memory material storage elements]

Informative references

Attention is drawn to the following places, which may be of interest for search:

Using organic memory material storage elements	G11C 13/0014

G11C 11/5671

[N: using charge trapping in an insulator]

Informative references

Attention is drawn to the following places, which may be of interest for search:

Comprising cells with charge storage in an insulating layer, e.g. MNOS, SNOS	G11C 16/0466

G11C 11/5678

[N: using amorphous/crystalline phase transition storage elements]

Informative references

Attention is drawn to the following places, which may be of interest for search:

Comprising amorphous/crystalline phase transition cells	G11C 13/0004

G11C 11/5685

using storage elements comprising metal oxide memory material, e.g. perovskites

Informative references

Attention is drawn to the following places, which may be of interest for search:

Comprising metal oxide memory material, e.g. perovskites	G11C 13/0007

G11C 11/5692

[N: read-only digital stores using storage elements with more than two stable states]

Informative references

Attention is drawn to the following places, which may be of interest for search:

Read-only memories programmable only once; Semi-permanent stores, e.g. manually-replaceable information cards	G11C 17/00

G11C 13/00

Digital stores characterised by the use of storage elements not covered by groups G11C11/00, G11C23/00 to G11C25/00

Definition statement

This subclass/group covers:

Digital stores or memories:

- Using elements in which the information is stored in the form of steps of electrical resistance [Ohm], Resistance RAM (RRAM) and auxiliary circuitry therefore; under G11C 13/0002;

- Using elements whose operation depends on chemical change, G11C 13/02 (G11C 13/0009 takes precedence);

- Using nanotube elements, under G11C 13/025;

- Using optical elements, under G11C 13/04;

- Using magneto-optical elements, under G11C 13/06.

Relationship between large subject matter areas

H01L: Semiconductor fabrication means and methods.

G03H: Holographic processes and apparatus.

References relevant to classification in this group

This subclass/group does not cover:

Digital stores in which the storage effect is based exclusively on magnetism e.g. Magnetic RAM (MRAM)	G11C 11/15, G11C 11/16

Informative references

Attention is drawn to the following places, which may be of interest for search:

Bistable switching devices, e.g. Ovshinsky-effect devices	H01L 45/00B
The switching materials being oxides or nitrides	H01L 45/00B2

G11C 13/0002

[N: using resistance random access memory [RRAM] elements]

Definition statement

This subclass/group covers:

RRAM storage elements; for MRAM storage elements see G11C 11/15 and G11C 11/16.

G11C 13/0004

[N: comprising amorphous/crystalline phase transition cells]

Definition statement

This subclass/group covers:

RRAM elements in which the electrical resistance change is based on an amorphous to crystalline or crystalline to amorphous transition in a phase change material.

Informative references

Attention is drawn to the following places, which may be of interest for search:

Multi-state phase transition memory cells	G11C 11/5678

G11C 13/0007

[N: comprising metal oxide memory material, e.g. perovskites]

Definition statement

This subclass/group covers:

RRAM elements in which the electrical resistance change is based on a switching mechanism in metal oxides e.g. TiO, NiO, HfO2, CuO.

Informative references

Attention is drawn to the following places, which may be of interest for search:

Multibit storage elements using metal oxide memory material	G11C 11/5685

G11C 13/0009

[N: RRAM elements whose operation depends upon chemical change]

Definition statement

This subclass/group covers:

RRAM elements in which the electrical resistance change is based on the formation and breaking of chemical bonds.

G11C 13/0011

[N: comprising conductive bridging RAM [CBRAM] or programming metallization cells [PMCs]]

Definition statement

This subclass/group covers:

RRAM elements in which the electrical resistance change is based on ion movement in a solid electrolyte between metal electrodes.

G11C 13/0014

[N: comprising cells based on organic memory material]

Informative references

Attention is drawn to the following places, which may be of interest for search:

Multibit storage elements using organic memory material	G11C 11/5664

G11C 13/0021

[N: Auxiliary circuits]

Definition statement

This subclass/group covers:
Auxiliary circuitry for RRAM elements.

Informative references

Attention is drawn to the following places, which may be of interest for search:

Details of stores	G11C 5/00
Arrangements for writing information into, or reading information out from, a digital store	G11C 7/00
Arrangements for selecting an address in a digital store	G11C 8/00

G11C 13/0023

[N: Address circuits or decoders]

Informative references

Attention is drawn to the following places, which may be of interest for search:

Arrangements for selecting an address in a digital store	G11C 8/00

G11C 13/0026

[N: Bit-line or column circuits]

Informative references

Attention is drawn to the following places, which may be of interest for search:

Bit line control circuits, e.g. drivers, boosters, pull-up circuits, pull-down circuits, precharging circuits, equalising circuits, for bit lines	G11C 7/12

Bit line organisation; Bit line lay-out	G11C 7/18

G11C 13/0028

[N: Word-line or row circuits]

Informative references

Attention is drawn to the following places, which may be of interest for search:

Word line control circuits, e.g. drivers, boosters, pull-up circuits, pull-down circuits, precharging circuits, for word lines	G11C 8/08
Word line organisation; Word line lay-out	G11C 8/14

G11C 13/0038

[N: Power supply circuits]

Informative references

Attention is drawn to the following places, which may be of interest for search:

Power supply arrangements	G11C 5/14

G11C 13/004

[N: Reading or sensing circuits or methods]

Informative references

Attention is drawn to the following places, which may be of interest for search:

Sense amplifiers; Associated circuits	G11C 7/06
Data output circuits, e.g. read-out amplifiers, data output buffers, data output registers, data output level conversion circuits	G11C 7/1051

G11C 13/0059

[N: Security or protection circuits or methods]

Informative references

Attention is drawn to the following places, which may be of interest for search:

Memory cell safety or protection circuits, e.g. arrangements for preventing inadvertent reading or writing; Status cells; Test cells	G11C 7/24
Address safety or protection circuits, i.e. arrangements for preventing unauthorised or accidental access	G11C 8/20

G11C 13/0061

[N: Timing circuits or methods]

Informative references

Attention is drawn to the following places, which may be of interest for search:

Read-write (R-W) timing or clocking circuits; Read-write (R-W) control signal generators or management	G11C 7/22
Address timing or clocking circuits; Address control signal generation or management, e.g. for row address strobe (RAS) or column address strobe (CAS) signals	G11C 8/18

G11C 13/0069

[N: Writing or programming circuits or methods]

Informative references

Attention is drawn to the following places, which may be of interest for search:

Data input circuits, e.g. write amplifiers, data input buffers, data input registers, data input level	G11C 7/1078

conversion circuits	

G11C 13/02

using elements whose operation depends upon chemical change [N: (G11C13/00R5T takes precedence)]; using electrochemical charge G11C11/00)

Definition statement

This subclass/group covers:

Storage elements in which the electrical resistance change is based on the formation and breaking of chemical bonds (for RRAM G11C 13/0009 takes precedence).

References relevant to classification in this group

Attention is drawn to the following places, which may be of interest for search:

Using electrochemical charge	G11C 11/00

G11C 13/06

using magneto-optical elements (magneto-optics in general G02F) [N: G11C13/042 takes precedence]

References relevant to classification in this group

This subclass/group does not cover:

Using information stored in the form of an interference pattern	G11C 13/042
Using magnetic-optical storage elements	G11C 13/043

Informative references

Attention is drawn to the following places, which may be of interest for search:

Magneto-optics in general	G02F

Synonyms and Keywords

In patent documents the following abbreviations are often used:

CBRAM	Conductive Bridging RAM
OUM	Ovonic Unified Memory
PCM	Phase Change Memory
PRAM	Phase change RAM
PCRAM	Phase Change RAM
PMC	Programming Metallization Cell
ReRAM	Resistance RAM
RRAM	Resistance RAM

In patent documents the expressions "PMC" and "CBRAM" are often used as synonyms.

In patent documents the expressions "PRAM", "PCRAM", "PCM", "OUM", "Chalcogenide RAM" and "Ovshinsky-effect memory" are often used as synonyms.

G11C 14/00

Digital stores characterised by arrangements of cells having volatile and non-volatile storage properties for back-up when the power is down [N: bistable elements storing the actual state when the supply voltage fails H03K3/02335, H03K3/0375, H03K3/2865, H03K3/356008]

Definition statement

This subclass/group covers:

Memories with arrangements to save information from a volatile to a nonvolatile memory when power supply is lost and to restore the information from the nonvolatile to the volatile memory when power is restored.

Sub-groups cover details of cells adapted for this purpose, classified first by volatile and then by nonvolatile storage type.

Relationship between large subject matter areas

For memories where volatile and non-volatile elements co-exist but are operated independently, see G11C 11/005. For volatile memories which are designed to power up in a known state (latent image memory), see G11C 7/20.

References relevant to classification in this group

This subclass/group does not cover:

Bistable elements storing the actual state when the supply voltage fails	H03K 3/02335, H03K 3/0375, H03K 3/2865, H03K 3/356008

Special rules of classification within this group

Where a document only describes the presence of a nonvolatile memory to backup a volatile memory, without cell details, it should be placed in the main group. In principle, a search for such a document would need to encompass all the sub-groups as well as the main group. More detail about the type of storage elements can be added by using Indexing Codes relating to specific cell types.

G11C 14/0009

[N: in which the volatile element is a DRAM cell]

Informative references

Attention is drawn to the following places, which may be of interest for search:

DRAM cells	G11C 11/401

Special rules of classification within this group

In case the nonvolatile element is not covered below, classify here with an Indexing Code to specify its type.

G11C 14/0018

[N: and the nonvolatile element is an EEPROM element, e.g. a floating gate or MNOS transistor]

Special rules of classification within this group

Can further distinguish between FG (Indexing Code G11C 16/0408) and MNOS (Indexing Code: G11C 16/0466).

G11C 14/0027

[N: and the nonvolatile element is a ferroelectric element]

Informative references

Attention is drawn to the following places, which may be of interest for search:

FeRAM cells in general	G11C 11/22

G11C 14/0036

[N: and the nonvolatile element is a magnetic RAM [MRAM] element or ferromagnetic cell]

Special rules of classification within this group

Can be further characterised using codes from Indexing Code G11C 11/14 to Indexing Code G11C 11/16.

G11C 14/0045

[N: and the nonvolatile element is a resistive RAM element, i.e. programmable resistors, e.g. formed of phase change or chalcogenide material.]

Special rules of classification within this group

Can be further characterised using codes from Indexing Code G11C 13/0002 to Indexing Code G11C 13/0019.

G11C 14/0054

[N: in which the volatile element is a SRAM cell]

Special rules of classification within this group

In case the nonvolatile element is not covered below, classify here with an Indexing Code to specify its type. For SRAM cells in general see G11C 11/41.

G11C 14/0063

[N: and the nonvolatile element is an EEPROM element, e.g. a

floating gate or MNOS transistor]

Special rules of classification within this group

Can further distinguish between FG (Indexing Code G11C 16/0408) and MNOS (Indexing Code G11C 16/0466).

G11C 14/0072

[N: and the nonvolatile element is a ferroelectric element]

Informative references

Attention is drawn to the following places, which may be of interest for search:

FeRAM cells	G11C 11/22

G11C 14/0081

[N: and the nonvolatile element is a magnetic RAM [MRAM] element or ferromagnetic cell]

Special rules of classification within this group

Can be further characterised using codes from Indexing Code G11C 11/14 to Indexing Code G11C 11/16.

G11C 14/009

[N: and the nonvolatile element is a resistive RAM element, i.e. programmable resistors, e.g. formed of phase change or chalcogenide material.]

Special rules of classification within this group

Can be further characterised using codes from Indexing Code G11C 13/0002 to Indexing Code G11C 13/0019.

G11C 15/00

Digital stores in which information comprising one or more characteristic parts is written into the store and in which information is read-out by searching for one or more of these characteristic parts, i.e. associative or content-addressed stores (in which information is addressed to a specific location G11C11/00; [N: selection information using

addressing means, e.g. hashing, tree addressing, chaining, G06F11/22; information retrieval systems using a computer G06F17/30])

Definition statement

This subclass/group covers:

Memories wherein a sought data word for a given field (characteristic part) is supplied as input to the memory, which is able to search its stored data contents to determine if the supplied data word is present among said data contents. If a match or 'hit' is established, the address(es) in the memory where the supplied data word was found is/are returned. Optionally the contents of all fields of the matching word are returned.

References relevant to classification in this group

This subclass/group does not cover:

Selection information using addressing means, e.g. hashing, tree addressing, chaining	G06F 11/22
Information retrieval systems using a computer	G06F 17/30
Digital stores in which information is addressed to a specific location	G11C 11/00

Synonyms and Keywords

In patent documents the following abbreviation is often used:

CAM	Content Addressable Memory

G11C 16/00

Erasable programmable read-only memories (G11C14/00 takes precedence)

Definition statement

This subclass/group covers:

Memories of the type in which charge is stored in a non-volatile manner, either in a "floating gate" capacitor (see G11C 16/0408) or trapped in the gate insulator of a transistor (see G11C 16/0466).

In both cases, the effect of charge storage is to modify the threshold voltage of the transistor, e.g. from depletion to enhancement mode (stored state discriminated by conduction or not at zero gate voltage) or from 'normal' to 'deep' enhancement (stored state discriminated by conduction or not at small positive gate voltage).

References relevant to classification in this group

This subclass/group does not cover:

NVRAM Nonvolatile battery backed up RAM	G11C 5/141
Digital stores in which the storage effect is based exclusively on magnetism e.g. Magnetic RAM (MRAM)	G11C 11/15, G11C 11/16
FeRAMs	G11C 11/22
RRAM, ReRAM (Resistive RAM)	G11C 13/0002 - G11C 13/00R53B
PCRAM, PRAM (Phase-change RAM)	G11C 13/0004
Digital stores characterised by arrangements of cells having volatile and non-volatile storage properties for back-up when the power is down	G11C 14/00
Fabrication of EPROM	H01L 21/8247
EPROM memory structures	H01L 27/115

Examples of places where the subject matter of this group is covered when specially adapted, used for a particular purpose, or incorporated in a larger system:

Use of a cell to back-up the contents of a corresponding volatile memory cell	G11C 14/00

Informative references

Attention is drawn to the following places, which may be of interest for search:

Structures of non-volatile memory arrays; individual transistor structures	H01L 27/115, H01L 29/788, H01L 29/792

G11C 16/02

electrically programmable [N: (programmable multibit digital storage elements G11C11/5621)

Informative references

Attention is drawn to the following places, which may be of interest for search:

Programmable multi-state digital storage elements	G11C 11/5621

G11C 16/0408

[N: comprising cells containing floating gate transistors (G11C16/0483, G11C16/0491 take precedence)]

Definition statement

This subclass/group covers:

Also cells in which the floating gate is composed of 'nanocrystals'.

References relevant to classification in this group

This subclass/group does not cover:

Comprising cells having several storage transistors connected in series	G11C 16/0483
Virtual ground arrays	G11C 16/0491

G11C 16/0416

[N: comprising cells containing a single floating gate transistor and no select transistor, e.g. UV EPROM]

Definition statement

This subclass/group covers:

May also comprise cells with additional control gates, e.g. an erase gate.

G11C 16/0425

[N. comprising cells containing a merged floating gate and select transistor]

Definition statement

This subclass/group covers:

The also known as "split-gate" or "1½ transistor" cells.

G11C 16/0433

[N: comprising cells containing a single floating gate transistor and one or more separate select transistors]

Definition statement

This subclass/group covers:

The classical EEPROM cells.

G11C 16/0441

[N: comprising cells containing multiple floating gate devices, e.g. separate read-and-write FAMOS transistors with connected floating gates]

Definition statement

This subclass/group covers:

Aso complementary-pair type cells, in which two floating gate transistors store opposite states. This type is often used to store redundancy information, see also G11C 29/789.

G11C 16/0483

[N: comprising cells having several storage transistors connected in series]

Definition statement

This subclass/group covers:

i.e. NAND type cells.

G11C 16/0491

[N: Virtual ground arrays]

Definition statement

This subclass/group covers:

i.e. arrays in which the individual cell transistors are formed between parallel bitlines, one of which is selected by decoder circuitry to be ground and the other as a normal bitline.

G11C 16/06

Auxiliary circuits, e.g. for writing into memory (in general G11C7/00)

Informative references

Attention is drawn to the following places, which may be of interest for search:

Details of stores	G11C 5/00
Arrangements for writing information into, or reading information out from, a digital store	G11C 7/00
Arrangements for selecting an address in a digital store	G11C 8/00

Special rules of classification within this group

This group is only used if no lower sub-group is suitable - assign multiple sub-groups rather than placing here.

G11C 16/08

Address circuits; Decoders; Word-line control circuits

Informative references

Attention is drawn to the following places, which may be of interest for search:

Arrangements for selecting an address in a digital store	G11C 8/00
Word line control circuits, e.g. drivers, boosters, pull-up circuits, pull-down circuits, precharging circuits, for word lines	G11C 8/08

Word line organisation; Word line lay-out	G11C 8/14

G11C 16/10

Programming or data input circuits

Informative references

Attention is drawn to the following places, which may be of interest for search:

Data input circuits, e.g. write amplifiers, data input buffers, data input registers, data input level conversion circuits	G11C 7/1078

G11C 16/107

[N: Programming all cells in an array, sector or block to the same state prior to flash erasing]

Definition statement

This subclass/group covers:

Erase preprogramming, also called preconditioning.

G11C 16/12

Programming voltage switching circuits

Definition statement

This subclass/group covers:

Especially high-voltage switches (see e.g. EP862183, figures 1-3), ramp generators (see e.g. EP903750, figure 4).

Fig.1

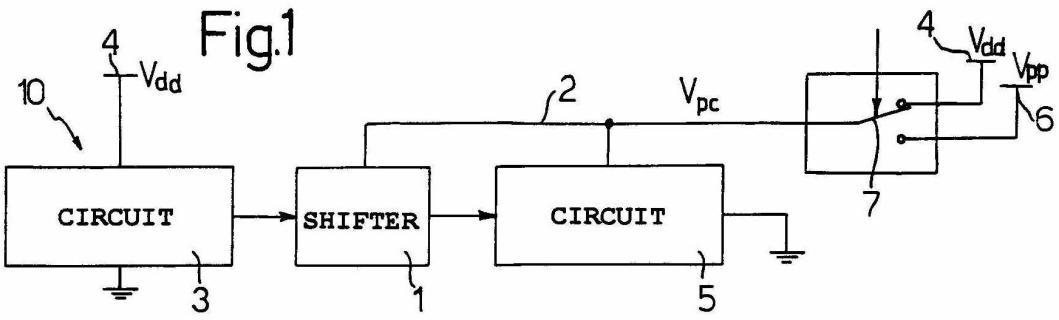
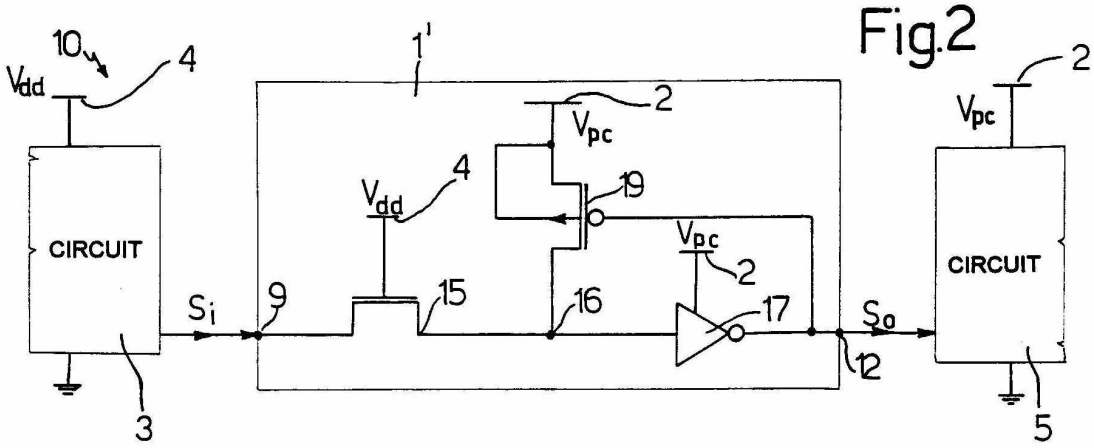


Fig.2



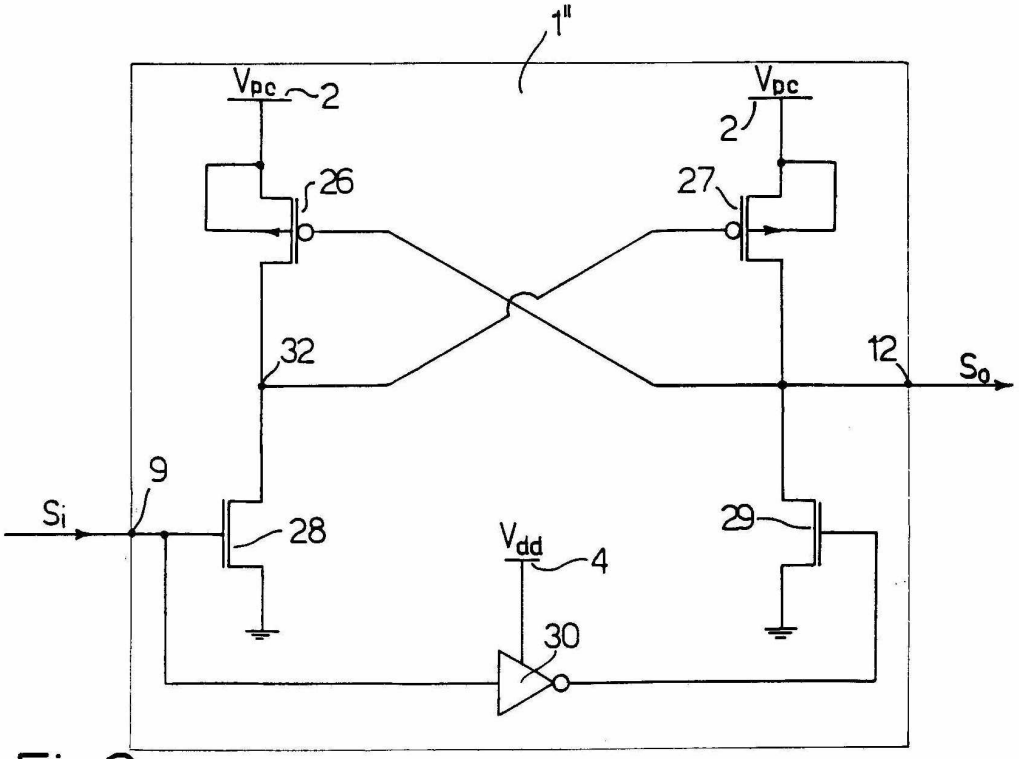
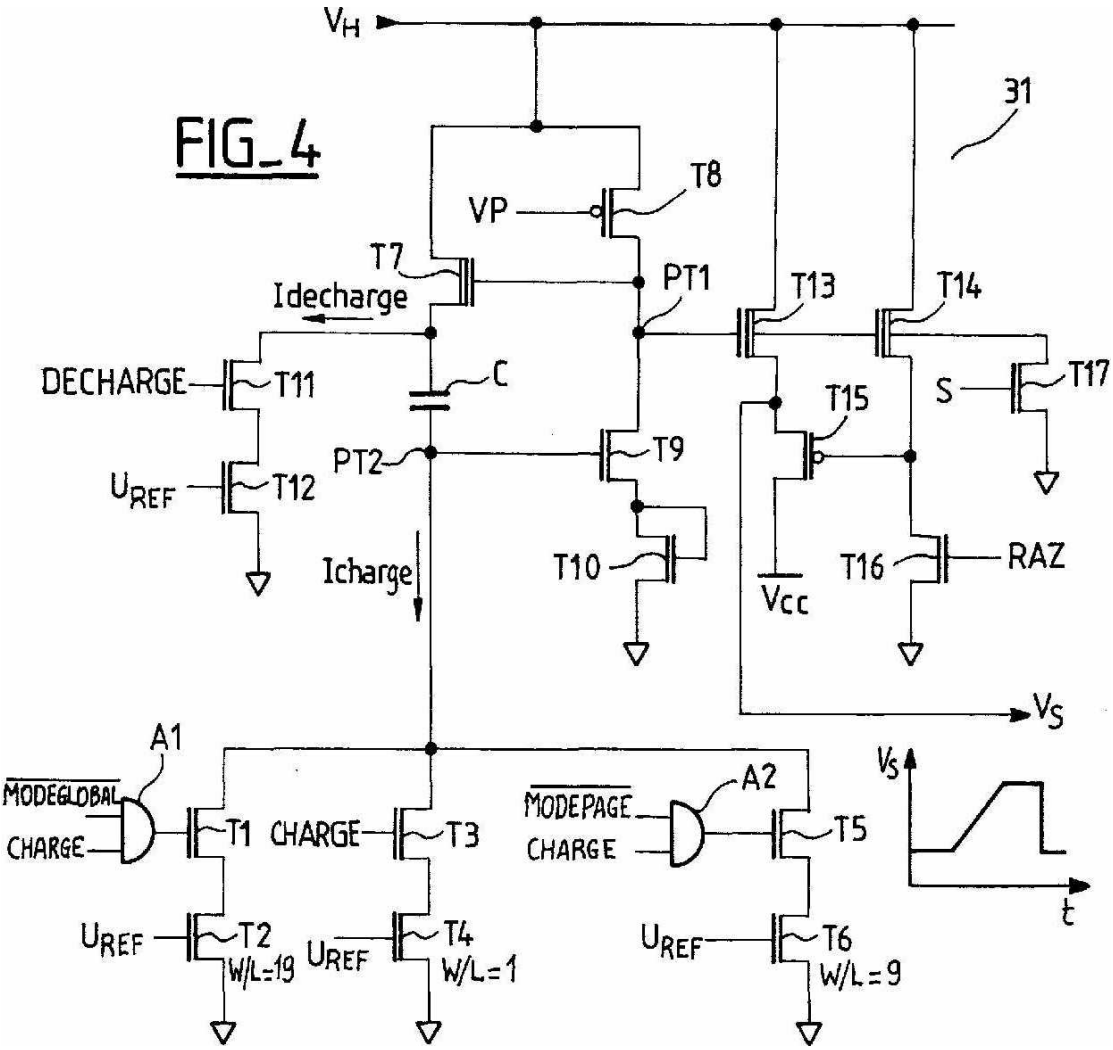


Fig.3



Informative references

Attention is drawn to the following places, which may be of interest for search:

Switches	H03K 5/003
Ramp generators	H03K 4/00

G11C 16/18

Circuits for erasing optically

Definition statement

This subclass/group covers:
e.g. ultra-violet erase.

G11C 16/20

Initialising; Data preset; Chip identification

Informative references

Attention is drawn to the following places, which may be of interest for search:

Memory initialisation circuits	G11C 7/20

G11C 16/22

Safety or protection circuits preventing unauthorised or accidental access to memory cells

Informative references

Attention is drawn to the following places, which may be of interest for search:

Memory cell safety or protection circuits	G11C 7/24
Address safety or protection circuits	G11C 8/20

G11C 16/225

[N: Preventing erasure, programming or reading when power supply voltages are outside the required ranges]

Informative references

Attention is drawn to the following places, which may be of interest for search:

Voltage level detection	G11C 5/143

G11C 16/24

Bit-line control circuits

Informative references

Attention is drawn to the following places, which may be of interest for search:

Bit line control circuits	G11C 7/12

Bit line organisation; Bit line lay-out	G11C 7/18

G11C 16/26

Sensing or reading circuits; Data output circuits

Informative references

Attention is drawn to the following places, which may be of interest for search:

Sense amplifiers; Associated circuits	G11C 7/06
Data output circuits	G11C 7/1051

G11C 16/30

Power supply circuits

Informative references

Attention is drawn to the following places, which may be of interest for search:

Power supply arrangements	G11C 5/14

G11C 16/32

Timing circuits

Informative references

Attention is drawn to the following places, which may be of interest for search:

Read-write (R-W) timing or clocking circuits; Read-write (R-W) control signal generators or management	G11C 7/22
Address timing or clocking circuits; Address control signal generation or management, e.g. for row address strobe (RAS) or column address strobe (CAS) signals	G11C 8/18

G11C 16/3404

[N: Convergence or correction of memory cell threshold voltages; Repair or recovery of overerased or overprogrammed cells]

Definition statement

This subclass/group covers:

What is also known as "overerase/overprogram correction" or "threshold convergence".

G11C 16/3445

[N: Circuits or methods to verify correct erasure of nonvolatile memory cells]

Definition statement

This subclass/group covers:

May lead to repeated erase, verify steps until correctly erased or retry limit reached (= failure).

G11C 16/345

[N: Circuits or methods to detect overerased nonvolatile memory cells, usually during erasure verification]

Definition statement

This subclass/group covers:

Circuits that make no attempt at recovery; the device is therefore regarded as faulty.

G11C 16/3459

[N: Circuits or methods to verify correct programming of nonvolatile memory cells]

Definition statement

This subclass/group covers:

Circuits that may lead to repeated program, verify steps until correctly programmed or retry limit reached (= failure).

G11C 16/3463

[N: Circuits or methods to detect overprogrammed nonvolatile memory cells, usually during program verification]

Definition statement

This subclass/group covers:

Circuits that make no attempt at recovery; the device is therefore regarded as faulty.

G11C 16/349

[N: Arrangements for evaluating degradation, retention or wearout, e.g. by counting erase cycles]

Synonyms and Keywords

In patent documents the following abbreviations are often used:

EAROM	Electrically-Alterable ROM
EEPROM, E2PROM	Electrically-Erasable PROM
EPROM	Erasable PROM
FAMOS	Floating-gate Avalanche Injection MOS
M(O)NOS	Metal (Oxide-)Nitride-Oxide Silicon
S(O)NOS	Silicon (Oxide-)Nitride-Oxide Silicon

In patent documents the following expressions/words "soft programming" (or "soft erasure/erasing"), "overerase (or overprogramming) correction" and "threshold convergence" are often used as synonyms.

G11C 17/00

Read-only memories programmable only once; Semi-permanent stores, e.g. manually-replaceable information cards ([N: multibit read-only memories G11C11/5692;] erasable programmable read-only memories G11C16/00; coding, decoding or code conversion, in general H03M; [N: combination of ROM and RAM G11C11/005, G11C14/00; for electrical control of combustion engines F02D41/2406])

Definition statement

This subclass/group covers:

Memories in which the stored data are permanently defined at the time of manufacturing (mask ROM) or which are adapted to be programmed with data one time only after manufacture (PROM).

References relevant to classification in this group

This subclass/group does not cover:

Multibit read only memories	G11C 11/5692
Rewritable resistive memories (RRAM)	G11C 13/0002
Erasable programmable read-only memories	G11C 16/00
Fabrication of read only memories	H01L 21/8246
Read only memory structures	H01L 27/112

Examples of places where the subject matter of this group is covered when specially adapted, used for a particular purpose, or incorporated in a larger system:

For electrical control of combustion engines	F02D 41/2406
Combination of ROM and RAM	G11C 11/005, G11C 14/00

G11C 17/123

[N: comprising cells having several storage transistors connected in series]

Definition statement

This subclass/group covers:

i.e. NAND-type cells.

G11C 17/126

[N: Virtual ground arrays]

Definition statement

This subclass/group covers:

i.e. arrays in which the individual cell transistors are formed between parallel bitlines, one of which is selected by decoder circuitry to be ground and the other as a normal bitline.

G11C 17/14

in which contents are determined by selectively establishing, breaking or modifying connecting links by permanently altering the state of coupling elements, e.g. PROM

Special rules of classification within this group

So-called OTPROM (one-time programmable read only memories), i.e. EPROMs or flash memory arrays which are wholly or partly adapted to not be erasable (e.g. UV EPROM with no erasing window in the package, flash arrays not selectable to receive erasing voltages) are classified in G11C 16/00, with code G11C 2216/26.

G11C 17/16

using electrically-fusible links

Definition statement

This subclass/group covers:

e.g. fuses, antifuses.

G11C 17/18

Auxiliary circuits, e.g. for writing into memory (in general G11C7/00)

Informative references

Attention is drawn to the following places, which may be of interest for search:

Details of stores	G11C 5/00
Arrangements for writing information into, or reading information out from, a digital store	G11C 7/00
Arrangements for selecting an	G11C 8/00

address in a digital store	

Synonyms and Keywords

In patent documents the following abbreviations are often used:

PROM	Programmable ROM
ROM	Read-only Memory

G11C 19/00

Digital stores in which the information is moved stepwise, e.g. shift register (counting chains H03K23/00) [N: stack stores, push-down stores (linear pulse counters H03K23/02, pulse distributors H03K5/15, methods and arrangements for shifting data G06F5/01)]

Definition statement

This subclass/group covers:

Digital stores or memories in which information is cascaded between neighbouring data storage locations in a chain under the control of at least one common clock signal.

References relevant to classification in this group

This subclass/group does not cover:

Methods and arrangements for shifting data	G06F 5/01
Counting chains	H03K 23/00
Linear pulse counters	H03K 23/02
Pulse distributors	H03K 5/15

G11C 21/00

Digital stores in which the information circulates [N:

continuously] (stepwise G11C19/00)

Definition statement

This subclass/group covers:

Digital stores or memories in which information bits circulate stepwise in a closed loop or ring arrangement.

References relevant to classification in this group

This subclass/group does not cover:

In which information circulates stepwise	G11C 19/00

G11C 23/00

Digital stores characterised by movement of mechanical parts to effect storage, e.g. using balls; Storage elements therefor (storing by actuating contacts G11C11/50)

Definition statement

This subclass/group covers:

Micromechanical and nanomechanical systems for data storage.

References relevant to classification in this group

This subclass/group does not cover:

Storing by actuating contacts	G11C 11/50

Informative references

Attention is drawn to the following places, which may be of interest for search:

Switches making use of microelectromechanical systems (MEMS)	H01H 1/0036
Switches making use of nanoelectromechanical systems (NEMS)	H01H 1/0094

Glossary of terms

In this subclass/group, the following terms (or expressions) are used with the meaning indicated:

In this group, the following terms are used with the meaning indicated:

MEMS	Microelectromechanical systems
NEMS	Nanoelectromechanical systems

G11C 25/00

Digital stores characterised by the use of flowing media; Storage elements therefor [N: (multiple fluid-circuit element arrangements for performing digital operations F15C1/12)]

Definition statement

This subclass/group covers:

Digital stores or memories whose operation is based on fluid or liquid media.

References relevant to classification in this group

This subclass/group does not cover:

Multiple fluid-circuit element arrangements for performing digital operations	F15C 1/12

G11C 27/00

Electric analogue stores, e.g. for storing instantaneous values [N: (integrating circuits acting as stores G06G7/18; pulse counters with step by step integration and static storage H03K25/00)]

Definition statement

This subclass/group covers:

Static stores or memories comprising:

- Analogue non-volatile charge storage, under G11C 27/005;

- Sample and hold arrangements, under G11C 27/02, G11C 27/024, G11C 27/026;
- Switched current memories under G11C 27/028;
- Shift registers with analogue charge storage, under G11C 27/04.

Relationship between large subject matter areas

H03K 17/00: Electronic switching or gating i.e. not by contact-making or -braking.

H03K 5/13: Arrangements having a single output and transforming input signals into pulses delivered at desired time intervals.

References relevant to classification in this group

This subclass/group does not cover:

Integrating circuits acting as stores	G06G 7/18
Pulse counters with step by step integration and static storage	H03K 25/00

Informative references

Attention is drawn to the following places, which may be of interest for search:

Digital stores using storage elements with more than two stable states	G11C 11/56

Synonyms and Keywords

In patent documents the following abbreviations are often used:

S/H	Sample and Hold

In patent documents the expressions "track and hold" and "sample and hold" are often used as synonyms.

G11C 29/00

Checking stores for correct operation; [N: Subsequent repair];

Testing stores during standby or offline operation [N: (testing of electronic circuits in general G01R31/28; error detection or error correction in computer memories during normal operation G06F11/1008, G06F11/1666; testing of computers during standby G06F11/22)]

Definition statement

This subclass/group covers:

The two main fields Test and Repair of semiconductor memories.

Concerning Test: This group covers test in particular

- after manufacturing including i. e. wafer test and test of packaged memories at manufacturer;
- after shipping to client and being in use when device is in test mode or performs test during power-on, idle or stand-by state, during refresh cycle.

Repair of memories is found below at G11C 29/70

Relationship between large subject matter areas

H01L: Semiconductor fabrication means and methods.

G06F 11/00: Error detection and correction, monitoring of normal operation.

G06F 12/00: Accessing, addressing or allocation within memory systems.

G01R 31/28: Test of electronic circuits.

References relevant to classification in this group

This subclass/group does not cover:

Test of electronic circuits in general	G01R 31/28
Test of digital circuits, e.g. separate computer components	G01R 31/317
Tester hardware in general	G01R 31/319
Error detection and correction in static stores integrated on a chip of data during normal operation with adding special bits of coded information in memories.	G06F 11/1008

Error detection or correction of the data by redundancy in hardware where the redundant component is memory or memory area	G06F 11/1666
Detection of defective computer hardware by testing during stand-by operation or during idle time, e.g. start-up testing.	G06F 11/22
Interconnection of, or transfer of information or other signals between, memories, input/output devices or central processing units for access to memory bus.	G06F 13/16
Memory bus transfer protocols	G06F 13/4234
Test and repair of storage types other than static stores (e.g. rotating disk drives).	G11B
Determination of programming status in electrically erasable and programmable read only memories (e.g. for floating gate transistors correction of threshold voltages , recovery of overerased or overprogrammed floating gate transistor cells G11C 16/3404; verifying correct erasure or programming of floating gate transistor cells G11C 16/3436; evaluation of degradation, retention or wearout of floating gate transistor cells G11C 16/349).	G11C 16/34
Test and configuration during manufacture	H01L 21/66
Test of single circuit components not integrated in memory device (e.g. transistors, capacitors) and not individual auxiliary circuits not integrated in memory device (e.g. power supplies, input/output circuitry).	Various classes

Informative references

Attention is drawn to the following places, which may be of interest for search:

Tester hardware in general	G01R 31/319
Error detection and correction in static stores integrated on a chip	G06F 11/10M2A
Error detection and correction in CAM	G06F 11/10M2A1
Error detection and correction in sector programmable memories, flash disks	G06F 11/10M2A3
Error detection and correction in multilevel memories	G06F 11/10M2A5
Details of memory controllers	G06F 13/1668

Special rules of classification within this group

Invention related features(concerning testing):

- G11C 29/02 Detection of defective auxiliary circuits

e.g. short circuit and cross talking on signal lines, intercell defects, stuck at fault (line permanently to GND or Vcc), refresh counter, fuses, charge pumps

G11C 29/021: in voltage or current generators

G11C 29/022: in I/O circuitry

G11C 29/023 : in clock generator or timing circuitry

G11C 29/024: in decoders

G11C 29/025: in signal lines

G11C 29/026: in sense amplifiers

G11C 29/027: in fuses

G11C 29/028: with adaption or trimming of parameters

- G11C 29/04 Detection of defective memory elements

- e.g. test of individual cells

- G11C 29/06 Acceleration test

e.g. only when stress (high temperature/voltage/clock frequency) is essential feature - EC documents only classified therein from 2007 onwards (IPC class for mostly Korean and Japanese documents relating to accelerated test)

- G11C 29/08 Functional test

e.g. when test is performed by writing/reading/comparing data, includes stress test (high temperature/voltage/clock frequency) when stress is not essential feature; test when something else is measured, i.e. not by write/read/compare in G11C 29/50

- G11C 29/10 Test algorithms and patterns

e.g. checkerboard pattern

- G11C 29/12 Built-in arrangements used for test

e.g. all for which no particular sub-class exists like error catch memory, word/bit line control, identification means, self refresh logic, interconnection details

G11C 29/12005: comprising voltage or current generators

G11C 29/1201: comprising IO circuitry

G11C 29/12015: comprising clock generation or timing circuitry

- G11C 29/14 Control logic

e.g. test configuration, internal clock generation, provisions for high speed test with low speed tester

- G11C 29/16 Micro programmed control logic

e.g. state machines, sequencers

- G11C 29/18 Address generation, memory access

e.g. address circuits, scrambling

- G11C 29/20 Using counters, linear feedback shift registers

e.g. linear address generation

- G11C 29/24 Accessing extra cells, dummy, redundant

e.g. test of redundant cells (replacement of defective cells in G11C 29/00R)

- G11C 29/26 Accessing multiple arrays

e.g. memories with multiple arrays serially accessed

- G11C 29/28 Dependent multiple arrays, multi bit

e.g. bit line/word line spans over multiple arrays and is in normal mode accessed at once

- G11C 29/30 Accessing single arrays

e.g. test on single array / block

- G11C 29/32 Serial access, Scan testing

e.g. cells connected in series only for test (overlap with G01R 31/318536 scan chain for logic test)

- G11C 29/34 Multiple bits

e.g. bit line/word line testing, more than one bit a time tested in single array, word line and bit line driver, controller, decoder therefor

- G11C 29/36 Data generation devices

e.g. data storage in DUT, inverters, row copy circuits

- G11C 29/38 Response verification devices

e.g. built-in comparators, means to read out test data from memory

- G11C 29/40 Using compression techniques

e.g. by use of LFSR (Linear Feedback Shift Register), EXOR logic circuit

- G11C 29/42 Using parity or error correction devices

e.g. test performed with use of ECC (overlap with G06F 11/10)

- G11C 29/44 Identification or indication of errors

e.g. for repair, keep track on found errors, failure capture (overlap with G06F 11/20)

- G11C 29/4401: for self repair
- G11C 29/46 Test trigger logic

e.g. initiation of test mode, how to avoid entering test mode

- G11C 29/48 Arrangements to allow test with external means

e.g. inside or outside memory, overlap with 12 and 56, test interfaces, test connectors, probes, I/O lines, reducing number of used pads/terminals to tester, external monitoring of test results, access paths, interface to scan chains, JTAG, DMA, external provided clock for test

- G11C 29/50 Other testing methods

e.g. marginal test including current, race, refresh, temperature, timing/delay, signal margin, imprint and fatigue, floating gate transistor test by dielectric layer test, e.g. gate oxide stress test; EEPROM erase/program verify when focus on threshold voltage or current measurement, i.e. at multilevel EEPROM; charge gain/leakage, DRAM data retention time test, trimming circuits

G11C 29/50004: of threshold voltage

G11C 29/50008: of impedance

G11C 29/50012: of timing

G11C 29/50016: of retention

e.g. data retention in DRAM or EEPROM cells

- G11C 29/52 Detection of memory contents errors

e.g. soft errors (i.e. radiation) or when memory content can not be read from outside (content protected), transparent test (modifies contents and restores back to original) EEPROM erase/program verify when 0/1 read (during normal operation G11C 16/34) when EEPROM cell is not defective but overerased / overprogrammed

- G11C 29/54 Design for test tools

e.g. design of test techniques, simulation, test coverage, error latency (probability)

- G11C 29/56 Tester hardware

e.g. external test machines, external pattern and address generation/scrambling, here only when specific for memories, overlap with G01R 31/319

G11C 29/56004: pattern generation

G11C 29/56008: error analysis

G11C 29/56012: timing aspects, clock generation, synchronisation

G11C 29/56: tester apparatus features

- G11C 29/66 Test of serial memories

e.g. FIFO, stacks, serial buffers

- G11C 29/68 Testing at wafer scale level

e.g. features particular related to wafer test, probing, test circuit location on wafer, e.g. in cut slot, chip identification, IDDQ-test. For test and configuration during manufacturing, see H01L 21/66.

Additional (not directly invention) related features:

- S11C 29/0402 Test of embedded memories
- S11C 29/0404 Test during or with feedback to manufacture

e.g. when test result is feedback into manufacturing process

- S11C 29/0406 Test circuit comprising complete loop

e.g. document discloses all essential elements off test loop from data generation via DUT to data comparison

- S11C 29/0408 Power on test
- S11C 29/0410 Online test

e.g. test is performed when memory operates in user application, either in idle state or by monitoring, leading to repair in case of failure

- S11C 29/0412 Online error detection and correction

Document relates to error correction (only) in normal operation:

- G11C 2029/1208 BIST with word line control
- S11C 29/1210 BIST with bit line control
- S11C 29/1212 Location of test circuitry on chip / wafer
- S11C 29/1214 BIST with error catch memory
- G11C 2029/1802 Test of address decoder
- G11C 2029/1804 Test with manipulation of data or word size
- G11C 2029/1806 Test with address conversion/mapping

e.g. translation of logical address to physical address

- G11C 2029/2602 Concurrent test

e.g. parallel / simultaneous test of multiple word lines / blocks / arrays / devices / modules

- G11C 2029/3202 BIST comprising scan chain
- G11C 2029/3602 BIST comprising pattern generator
- G11C 2029/4002 Comparison of products

e.g. comparison of test results of identical chips or with golden chip; or looping test result through a plurality of chips / modules

- G11C 2029/4402 Internal storage of test result related data

e.g. repair information, chip identification, quality data

- G11C 2029/5002 Test of characteristic

e.g. physical values not covered elsewhere

- G11C 2029/5004 Test of voltage
- G11C 2029/5006 Test of current
- G11C 2029/5602 Tester interface to DUT

e.g. for timing, voltage, multiplexing of test channels

- G11C 2029/5604 Tester with display of error information

e.g. as failure bit map

- G11C 2029/5606 Tester comprising error catch memory

e.g. raw data collection and management

Glossary of terms

In this subclass/group, the following terms (or expressions) are used with the meaning indicated:

In patent documents the following terms are used with the meaning indicated:

Scrubbing	Background test
Automatic test machine	External tester

Monitoring	Observation of normal operation
Scrambling, mapping	Translation of a logic address in a physical address or vice versa

Synonyms and Keywords

In patent documents the following abbreviations are often used:

ATM	Automatic Test Machine
BISR	Built-In Self-Repair
BIST	Built-In Self-Test
DUT, CUT	Device / Cell Under Test
IDDQ-test	direct current test
ECC	Error Correction Code
LFSR	Linear Feedback Shift Register

G11C 29/70

[N: Masking faults in memories by using spares or by reconfiguring]

Definition statement

This subclass/group covers:

Repairing defective memory devices by using redundant (spare) elements; repairing defective memory devices by reconfiguring the address space (this implies a reduced memory capacity compared with a non-defective device); algorithms for effecting such repairs.

Informative references

Attention is drawn to the following places, which may be of interest for search:

Error correction in digital computer systems using redundancy	G06F 11/16

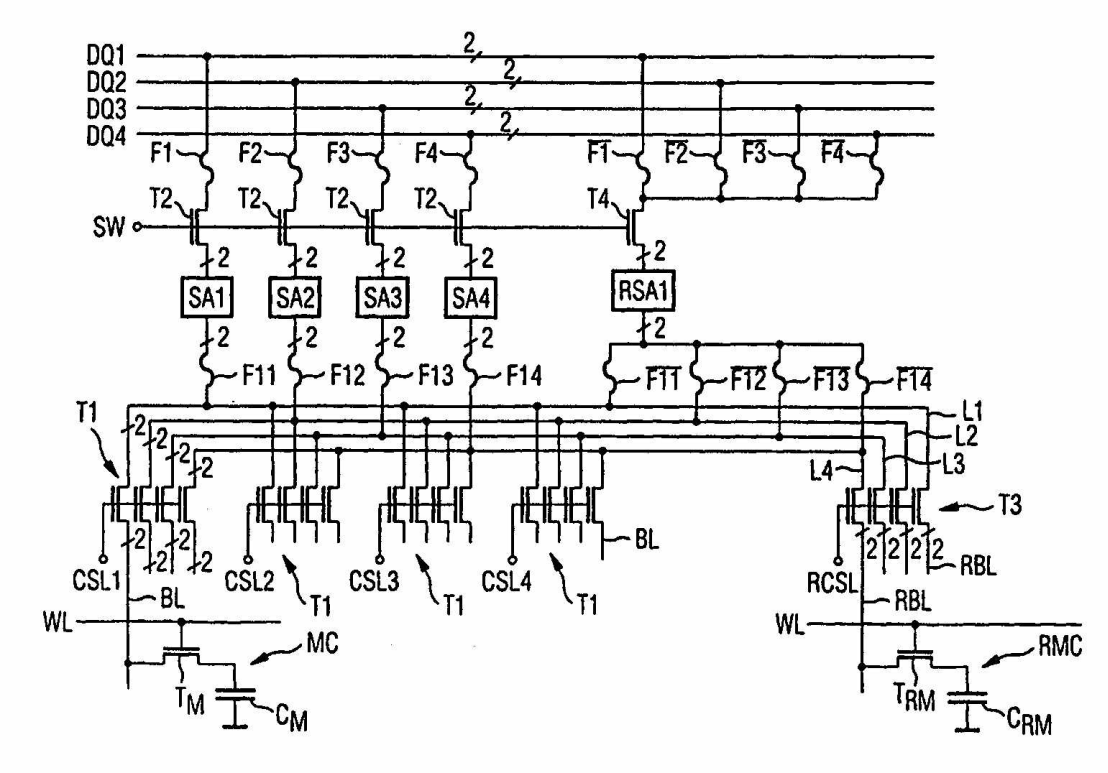
G11C 29/702

[N: by replacing auxiliary circuits, e.g. spare voltage generators, decoders or sense amplifiers, to be used instead of defective ones]

Definition statement

This subclass/group covers:

Illustrative example of subject matter classified in this group: EP1141834, figure 1.



G11C 29/72

[N: with optimized replacement algorithms]

Definition statement

This subclass/group covers:

Replacement algorithms (failure map to redundancy implementation).

G11C 29/74

[N: using duplex memories, i.e. using dual copies]

Informative references

Attention is drawn to the following places, which may be of interest for search:

Attention is drown to the following places, which may be of interest for search:

On disk or system level	G06F 11/20L

G11C 29/76

[N: using address translation or modifications]

Definition statement

This subclass/group covers:

Both with and without dedicated spares - typically address translations via pointers.

Techniques used for redundancy in this kind of applications are always very similar and almost all of them involve sector mapping, counting of read/erase operations, wear-out detection, etc. Many of these documents include lower level features related to flash memories (flash).

Special rules of classification within this group

See also G11C 16/349 for wear-out detection; G11C 29/88 for 'hard wired' reconfiguration.

G11C 29/78

[N: using programmable devices]

Definition statement

This subclass/group covers:

Could include disconnecting faulty elements.

G11C 29/783

[N: with refresh of replacement cells, e.g. in DRAMs]

Definition statement

This subclass/group covers:

In DRAMS, how to refresh the redundant lines which are substituting faulty

lines.

G11C 29/785

[N: with redundancy programming schemes]

Definition statement

This subclass/group covers:

Fuse related issues; most of these documents have descriptions at transistor level, explaining how the fuse circuits are built or how they are included in the redundancy decoding elements.

G11C 29/787

[N: using a fuse hierarchy (for memories using fuses in general G11C17/16)]

Definition statement

This subclass/group covers:

In this case, a master fuse can be used to decide whether a redundant line or decoder is in use. This allows to save time when programming the fuses. See EP646866, fig.3 (reference 50).

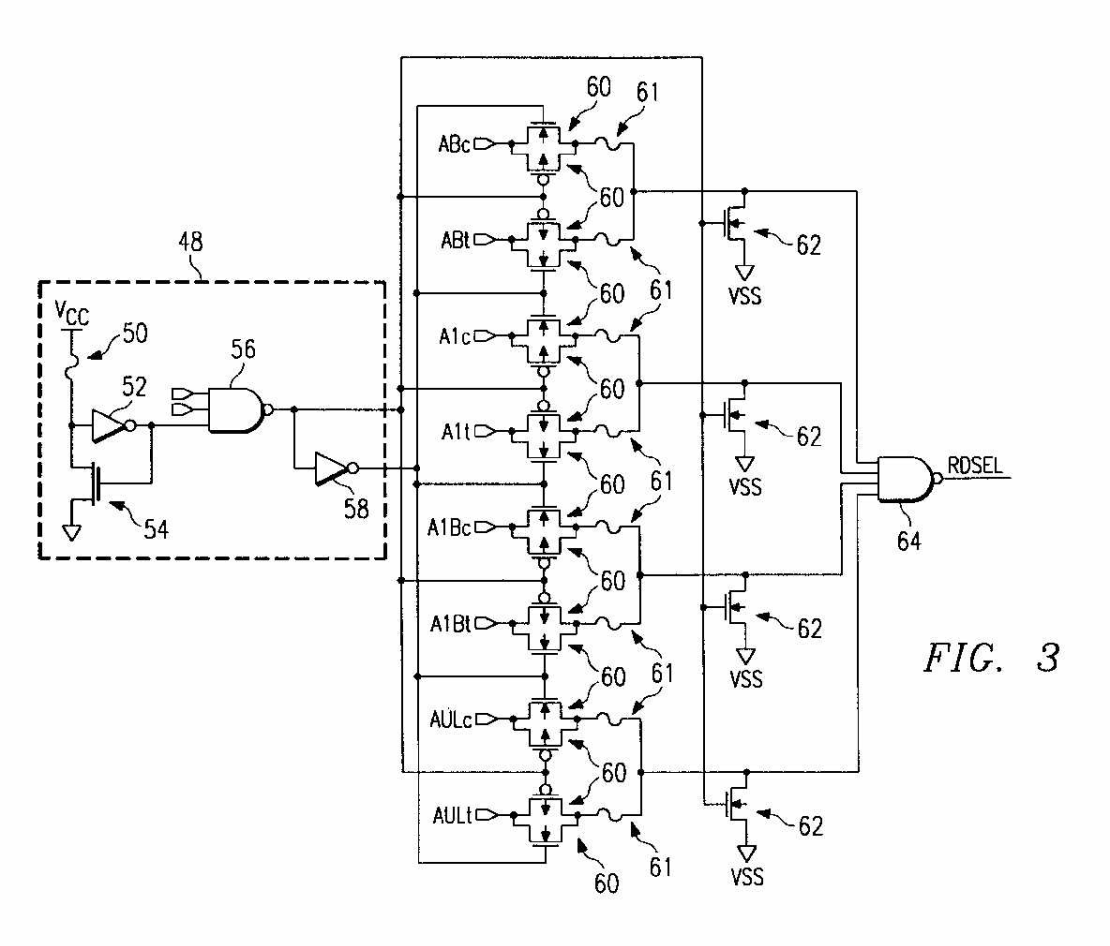


FIG. 3

Informative references

Attention is drawn to the following places, which may be of interest for search:

Attention is drown to the following places, which may be of interest for search:

Memories using fuses in general	G11C 17/16

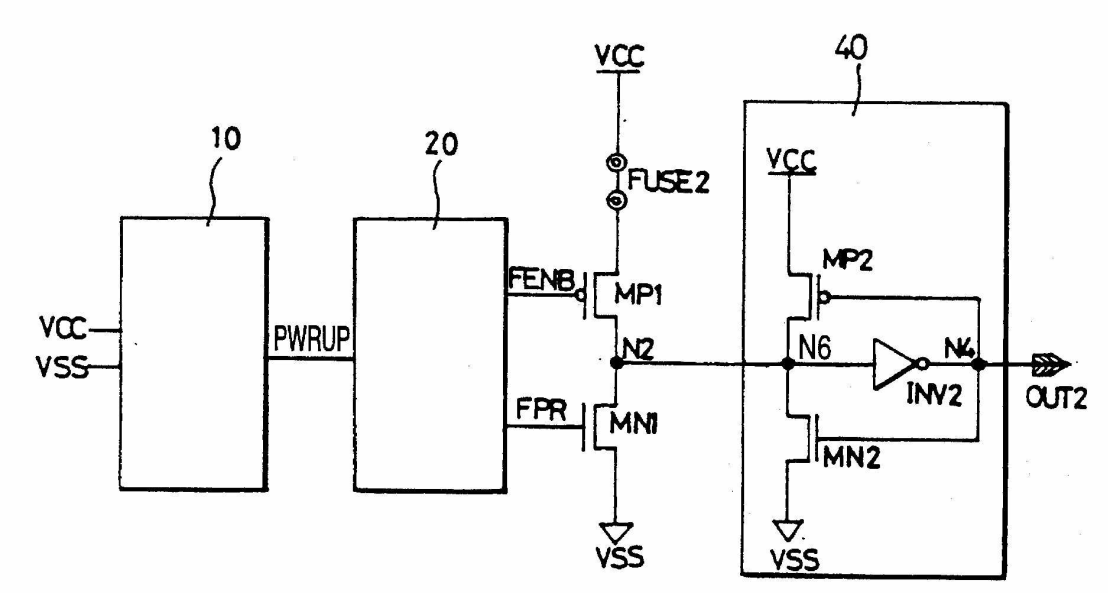
G11C 29/789

[N: using non-volatile cells or latches (erasable programmable memory cells in general G11C16/00)]

Definition statement

This subclass/group covers:

In these documents, the "fuse" is not a fuse as such, but rather a non-volatile memory cell or a combination of a fuse with a latch to retain its status (i.e. the fuse is only read at power up to reduce stress thereon). See US5619469, fig2.



Informative references

Attention is drawn to the following places, which may be of interest for search:

Attention is drown to the following places, which may be of interest for search:

Erasable programmable memory cells in general	G11C 16/00

G11C 29/80

[N: with improved layout]

Definition statement

This subclass/group covers:

Under this group, techniques which tend to reduce real estate by several means. When the document is a pure layout description - i.e. without a clear functionality other than a "new layout" - it is included in this 'head group'. It should be clear that there is a clear "layout" approach in the description and figures.

G11C 29/802

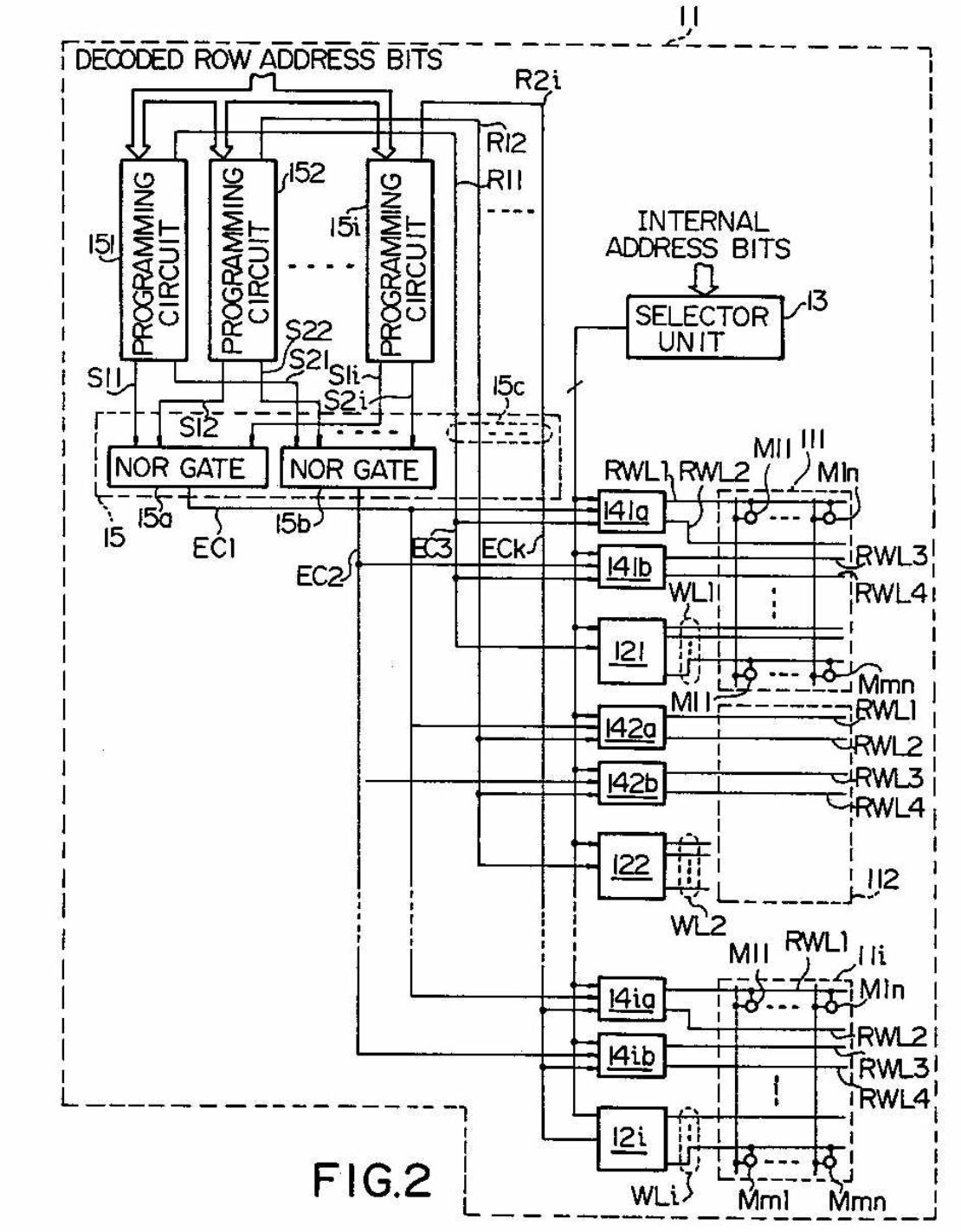
[N: by encoding redundancy signals]

Definition statement

This subclass/group covers:

Transmission of faulty/redundant addresses between the fuse boxes and the

final decoders is done by encoding: For 2n redundant lines only n lines have to be routed. See EP496282, fig.2.



G11C 29/804

[N: to prevent clustered faults]

Definition statement

This subclass/group covers:

Faults which involve several (adjacent) lines can be solved in a simplified way, 'simplified' implying using a reduced amount of coding or storage for the defect. These kind of faults are very frequent due to impurities of a big size. See US5281868, fig. 3,4.

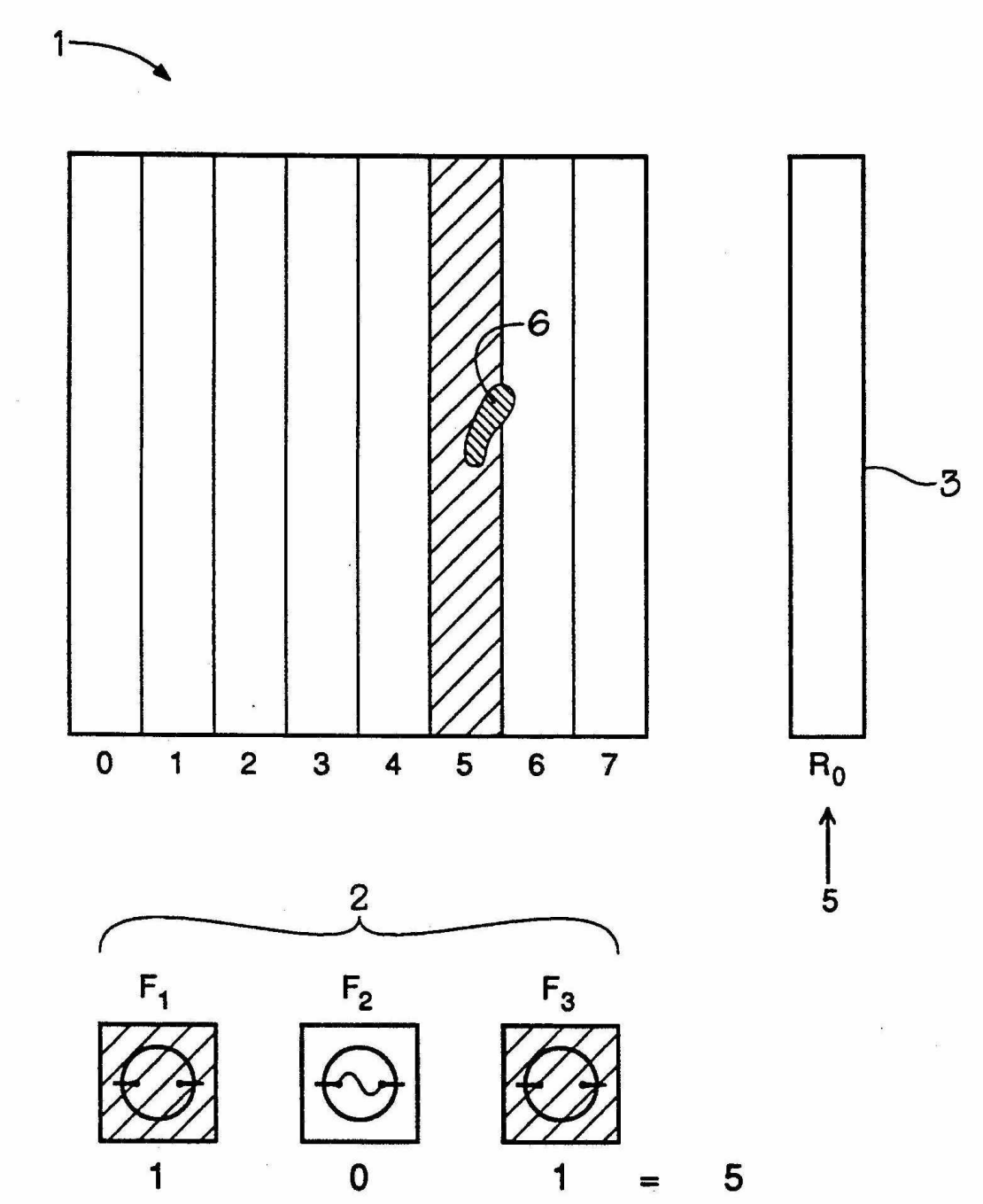


FIG. 3

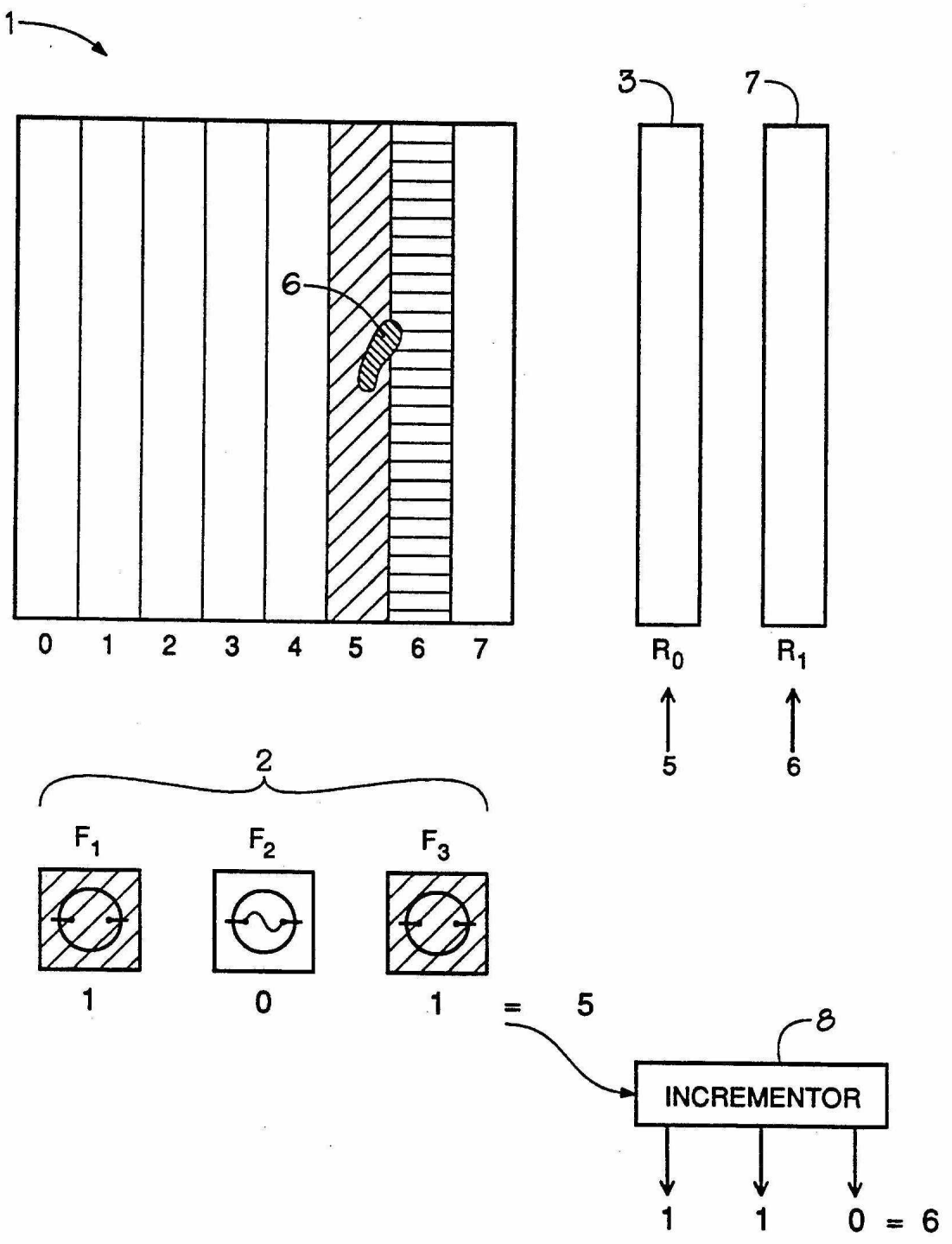


FIG. 4

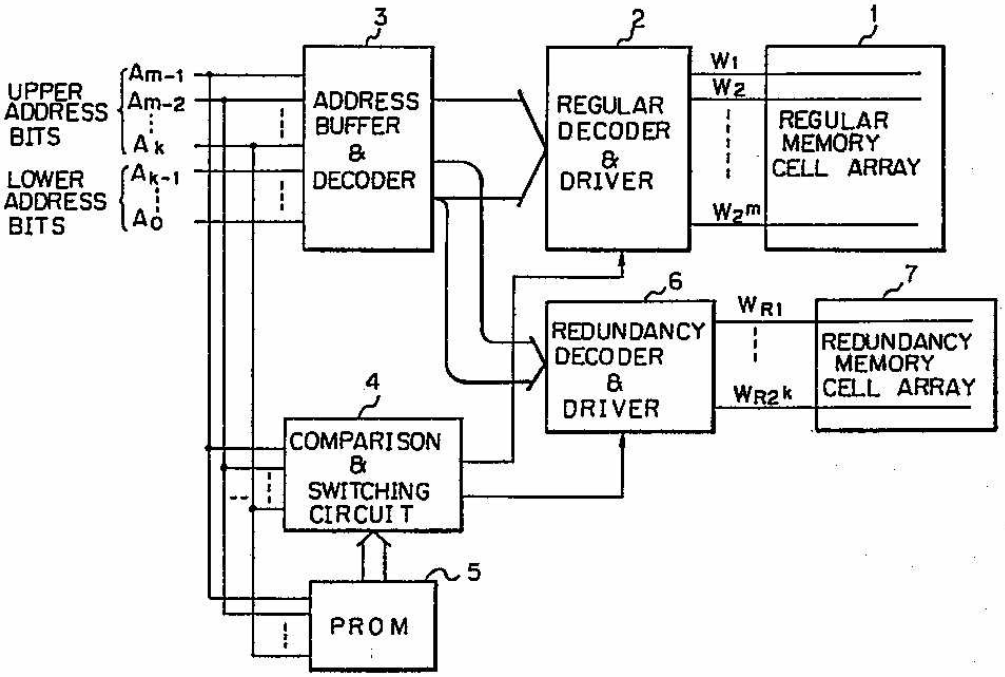
G11C 29/806

[N: by reducing size of decoders]

Definition statement

This subclass/group covers:

Solutions that might have a lower redundancy efficiency (e.g. lines can only be replaced in sets of four, regardless of the fault) but allows to have fewer and/or smaller comparators. See EP239196, fig 3.



G11C 29/808

[N: using a flexible replacement scheme]

Definition statement

This subclass/group covers:

All kinds of solutions in which different combinations of faulty/redundant replacement are possible to allow for a higher level of repair with a lower number of spares. For instance, when redundant lines in a block can be used to substitute faulty lines in any other block, or when the same redundant line can be used for row or column repair, etc. See US5469388 fig 4A.

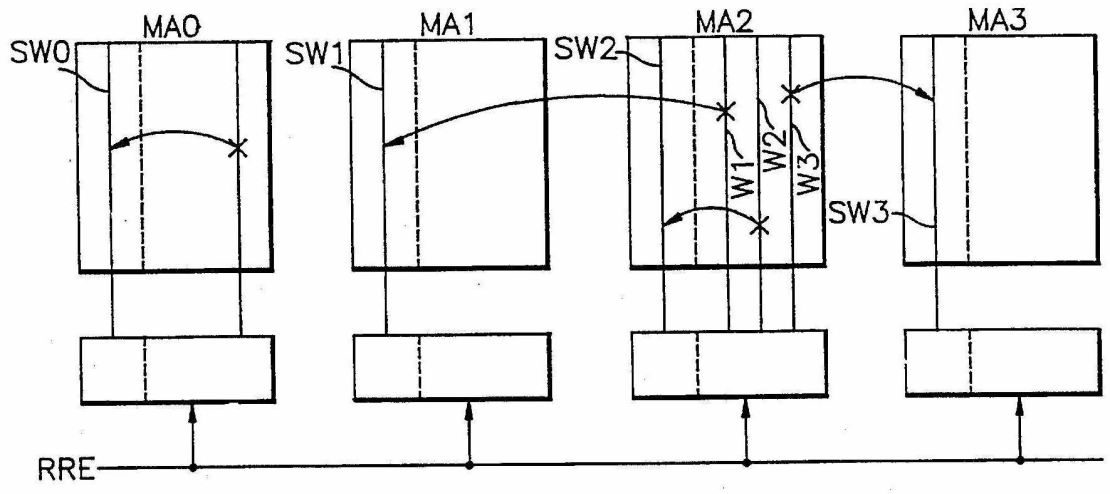


FIG. 4A

G11C 29/81

[N: using a hierarchical redundancy scheme]

Definition statement

This subclass/group covers:

Faults are solved in a hierarchical way. For instance: lines are replaced with redundant lines in a given block or, if not possible, then the complete block is repaired with a redundant block as a whole unit, etc. See US5295101, fig. 7.

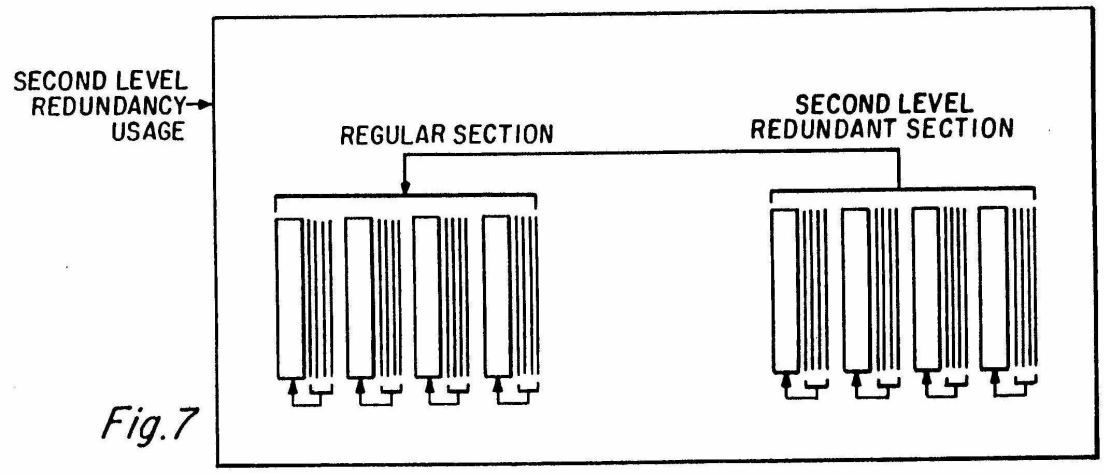


Fig.7

G11C 29/812

[N: using a reduced amount of fuses]

Definition statement

This subclass/group covers:

The amount of real estate occupied by fuses is lower.

G11C 29/814

[N: for optimized yield]

Definition statement

This subclass/group covers:

The layout is done in such a way that a certain cost function associated with the yield is optimized. A lot of NPL and thesis-like stuff. See XP237814.

G11C 29/816

[N: for an application-specific layout]

Definition statement

This subclass/group covers:

Certain applications (ROMs, synchronous memories, cache memories) demand redundancy solutions which are very related to the nature of the application itself and therefore more likely to be relevant in an application-oriented context.

G11C 29/818

[N: for dual-port memories]

Definition statement

This subclass/group covers:

For the case of Dual port RAMs, video memories and the like.

G11C 29/82

[N: for EEPROMs]

Definition statement

This subclass/group covers:

These redundancy solutions are usually taking into account the block erase operations as well as the aging of EEPROM cells due to program/erase. Many of these documents are also classified with the solid state disks solutions (G11C 29/765). Normally documents put in this group work at a lower level (i.e. row/columns in a block, rather than sector mapping level.

G11C 29/822

[N: for read only memories]

Definition statement

This subclass/group covers:

Redundancy solutions for Mask ROMs which have specific layouts.

G11C 29/824

[N: for synchronous memories]

Definition statement

This subclass/group covers:

Same as above for the case of synchronous memories. Timing (synchronicity) requirements as well as the specific (i.e. sequential) nature of read/write operations are linked to some redundancy requirements.

G11C 29/83

[N: with reduced power consumption]

Definition statement

This subclass/group covers:

Most of the solutions for this problem are related to the avoidance of DC faults.

G11C 29/832

[N: with disconnection of faulty elements]

Definition statement

This subclass/group covers:

A common way to reduce power consumption in these cases.

G11C 29/835

[N: with roll call arrangements for redundant substitutions]

Definition statement

This subclass/group covers:

Roll call circuits to identify redundancy substitutions.

G11C 29/838

[N: with substitution of defective spares]

Definition statement

This subclass/group covers:

Solving the problem of a faulty spare element which must be disabled for redundant substitution.

G11C 29/84

[N: with improved access time or stability]

Definition statement

This subclass/group covers:

In this group, solutions which propose to eliminate or reduce the difference in speed between a non-faulty and a faulty line selection. Many of these documents are actually addressing stability problems (e.g. obtain a reliable voltage level before sampling fuse values) employing similar solutions such as ATDs.

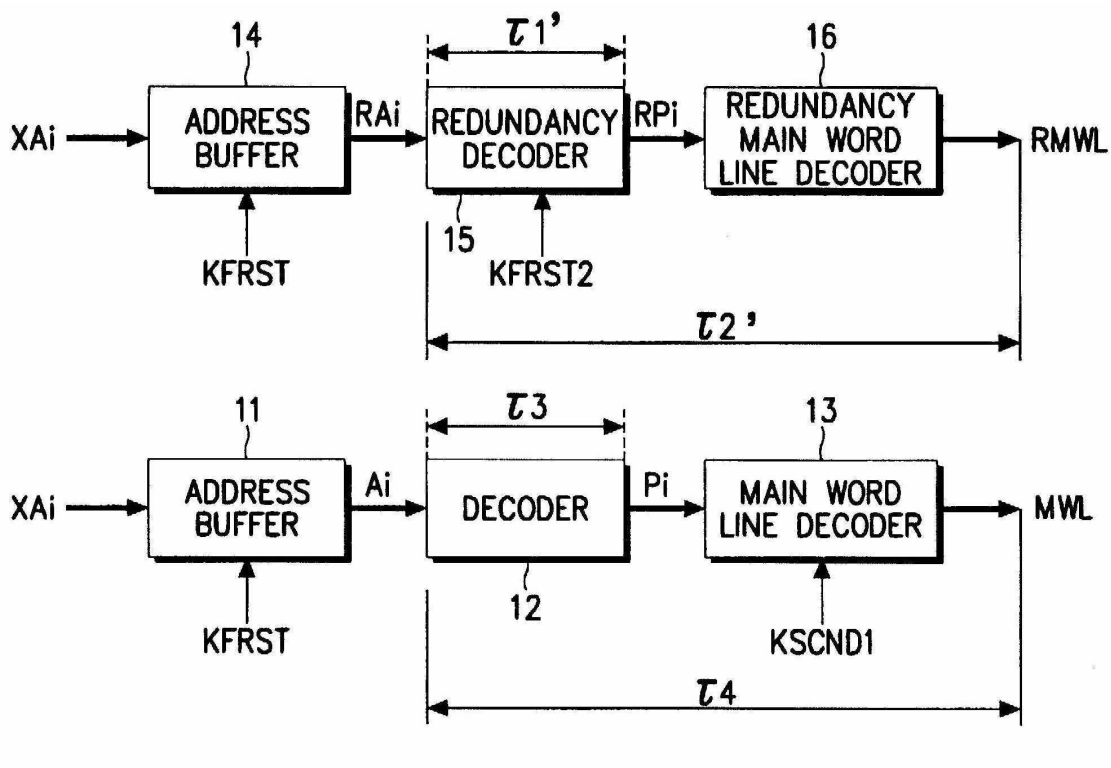
G11C 29/842

[N: by introducing a delay in a signal path]

Definition statement

This subclass/group covers:

The trick here usually is to insert a delay element in the faster path to make sure both paths (normal and redundant) are equally slow. This delay element usually consists of slower transistors in the path or a chain of inverters. See US5777931, fig.5.



G11C 29/844

[N: by splitting the decoders in stages]

Definition statement

This subclass/group covers:

A normal/redundant selection signal is already obtained at a predecoding stage which allows to start some kind of preselection. See US5550776, fig.4.

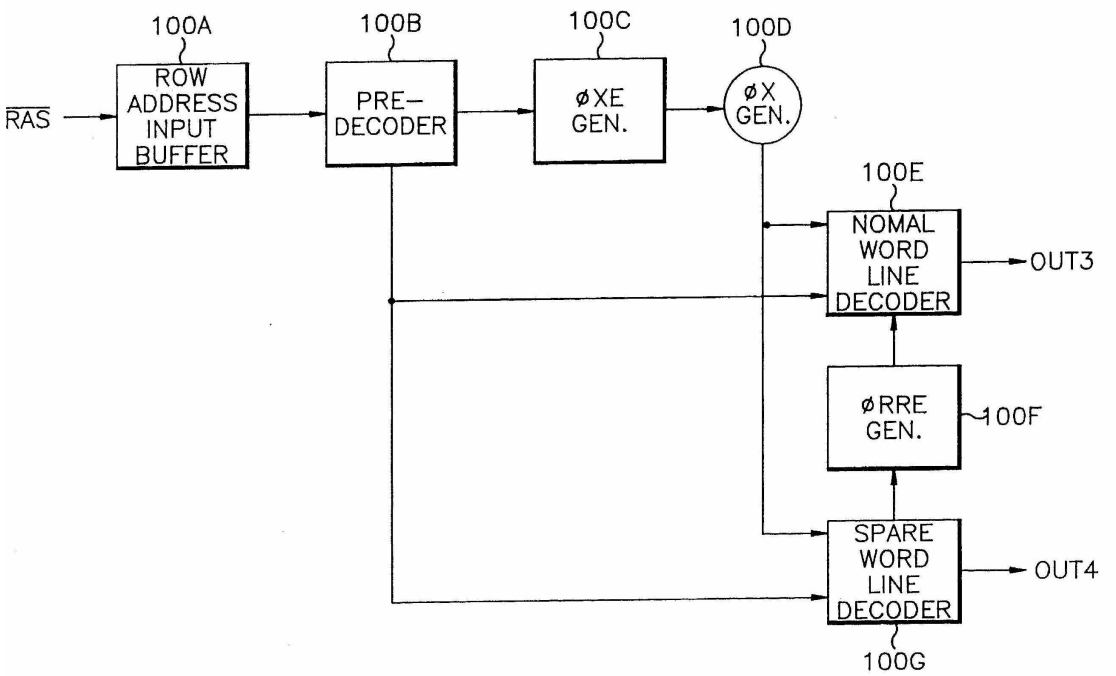


FIG. 4

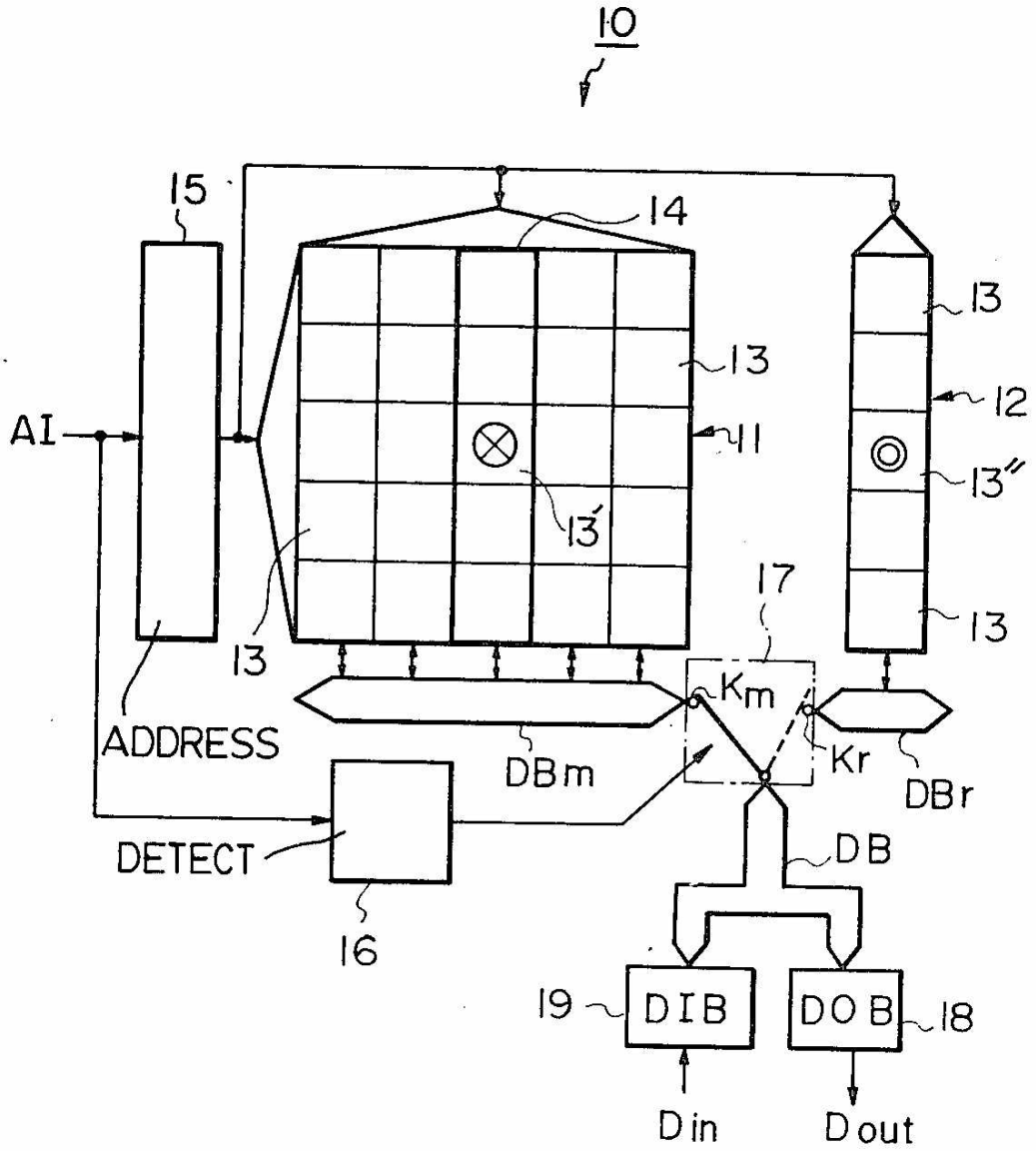
G11C 29/846

[N: by choosing redundant lines at an output stage]

Definition statement

This subclass/group covers:

Usually the case with column redundancy: Addresses are input simultaneously to faulty and normal column decoders and only at the output (usually by means of a multiplexer) it is decided whether a redundant replacement is pertinent. See US4473895, fig.1.



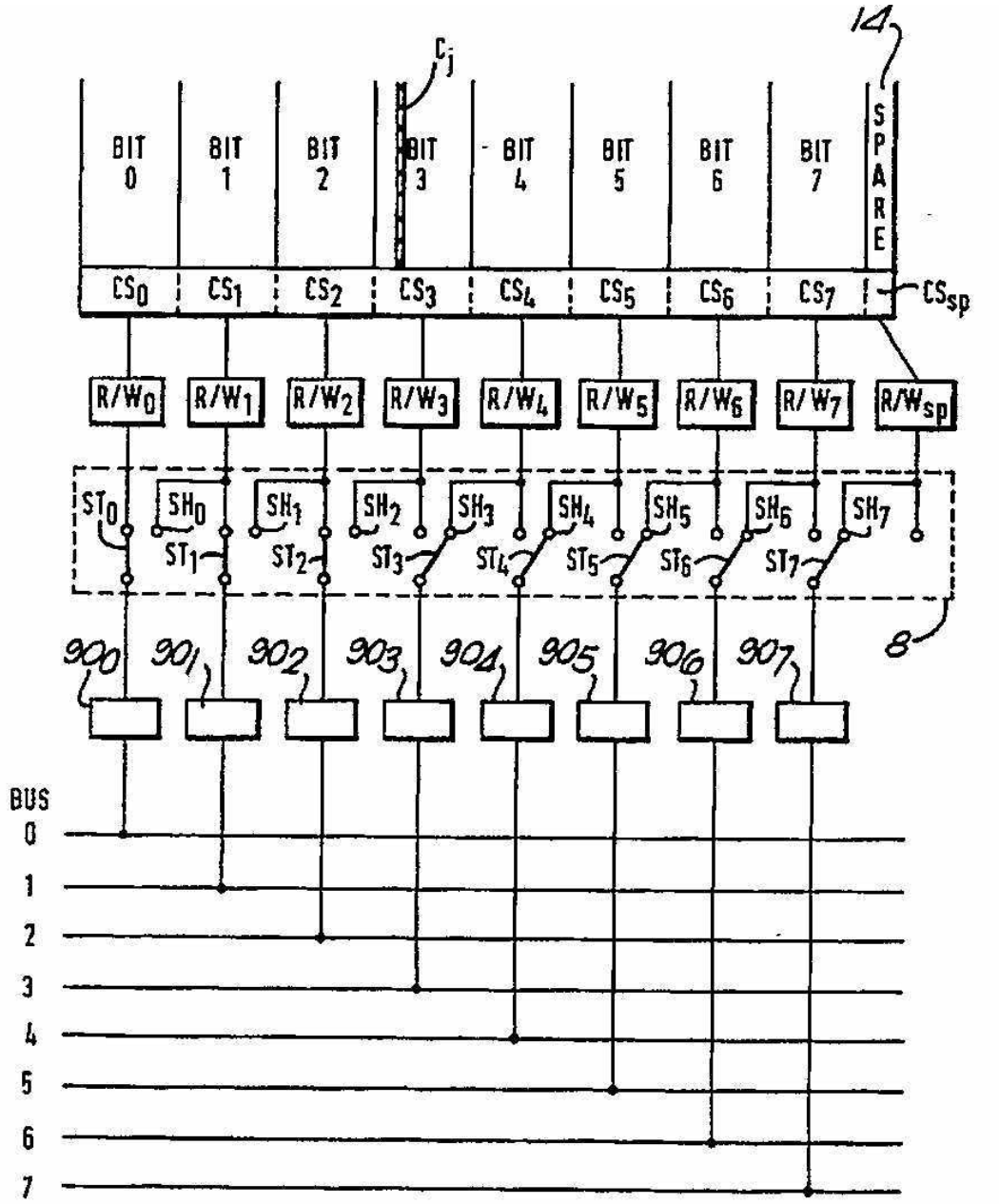
G11C 29/848

[N: by adjacent switching]

Definition statement

This subclass/group covers:

Columns are shifted one or more position skipping the faulty one(s). There are redundant columns at the end of the chain. See EP434200, fig. 4.



G11C 29/88

[N: with partially good memories]

Definition statement

This subclass/group covers:
Partially good memories, degraded memories.

Synonyms and Keywords

In patent documents the following abbreviations are often used:

DEP	Defective end product; (now G11C 29/883)
CDEP	Combining defective end product. (now G11C 29/886)

G11C 2229/723

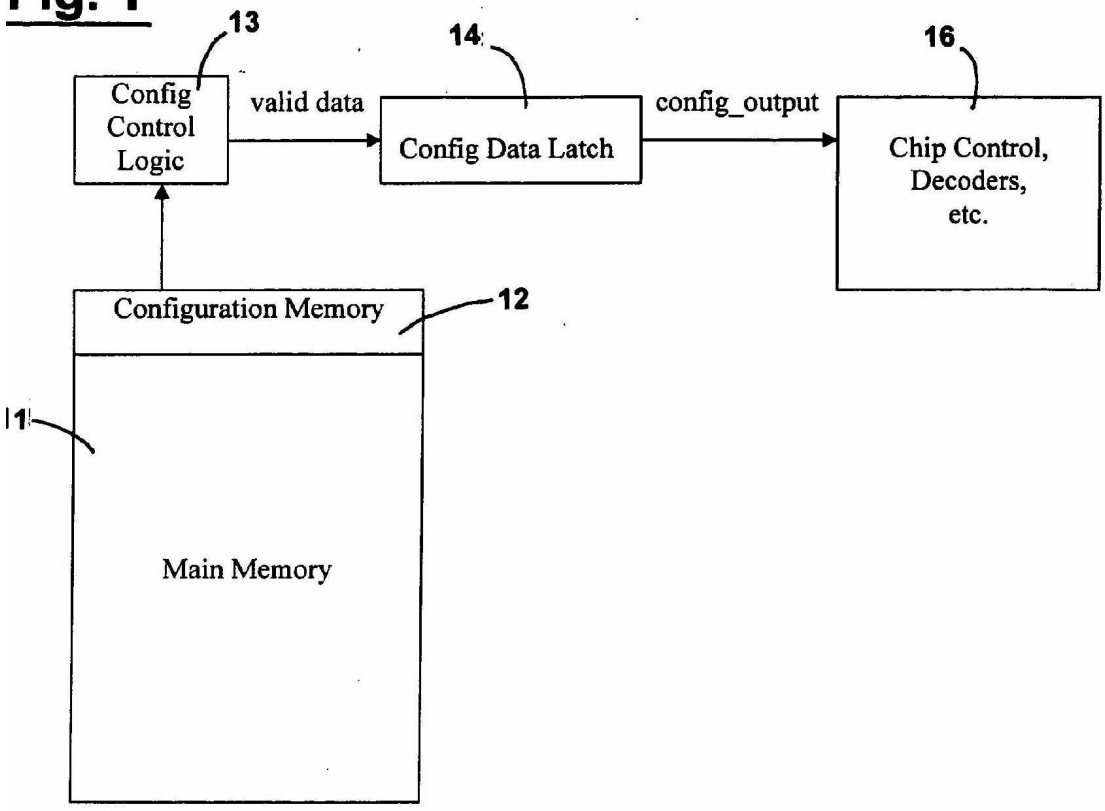
Redundancy information stored in a part of the memory core to be repaired.

Definition statement

This subclass/group covers:

See US2006190762 (figure 1 - shown), US2009067276.

Fig. 1

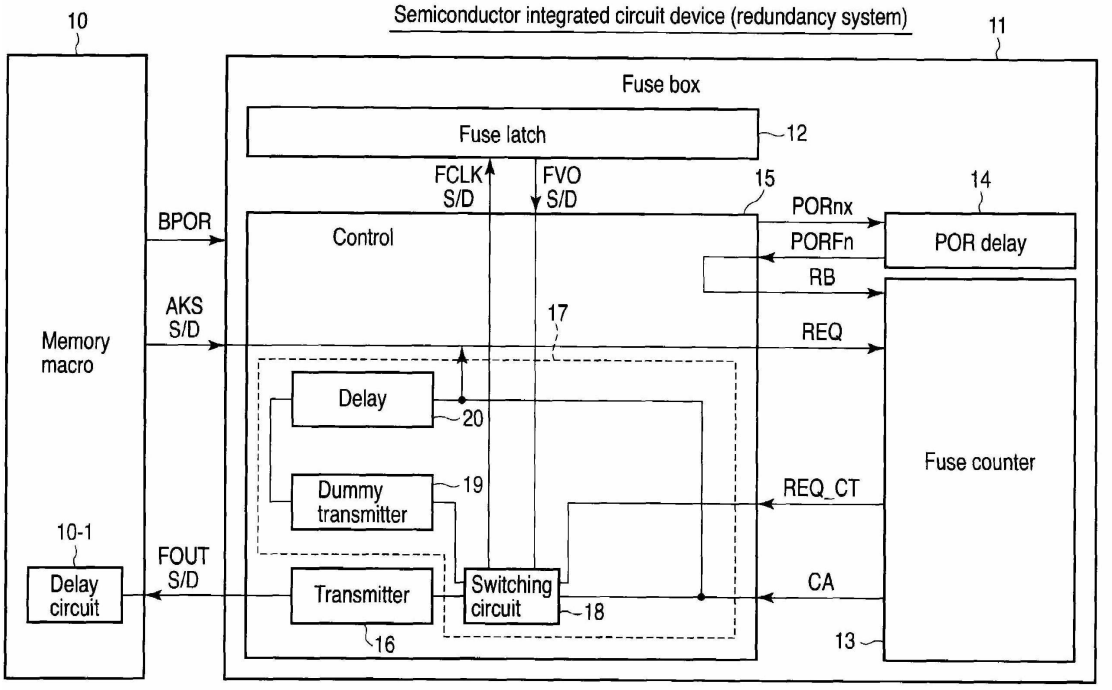


G11C 2229/726

Redundancy information loaded from the outside into the memory

Definition statement

This subclass/group covers:
See US2008307251 (fig.1), US2009072886 (fig.1 - shown).

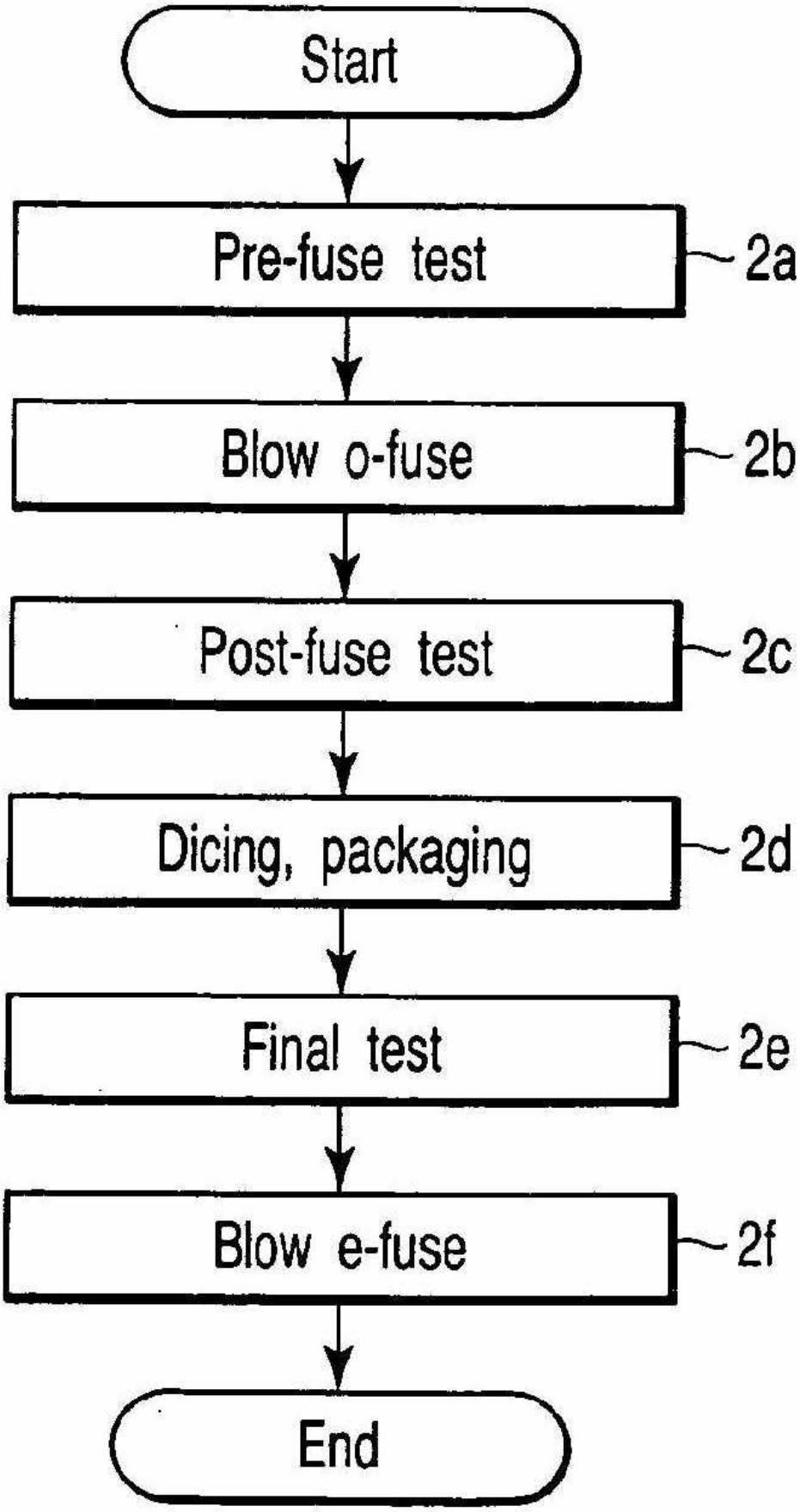


G11C 2229/746

Before packaging

Definition statement

This subclass/group covers:
See US2006221729, figure 2.

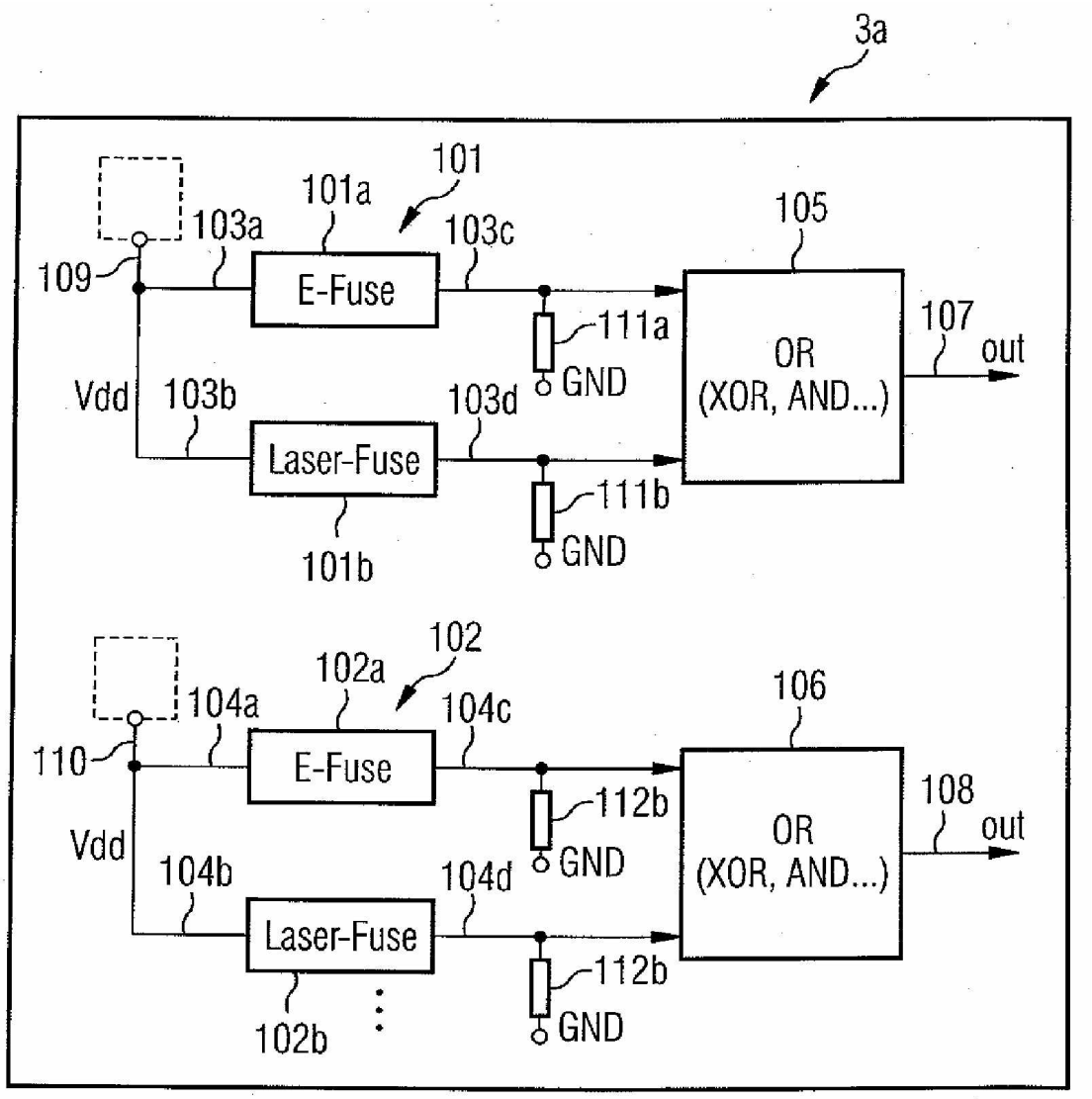

Start
Pre-fuse test
2a
Blow o-fuse
2b
Post-fuse test
2c
Dicing, packaging
2d
Final test
2e
Blow e-fuse
2f
End

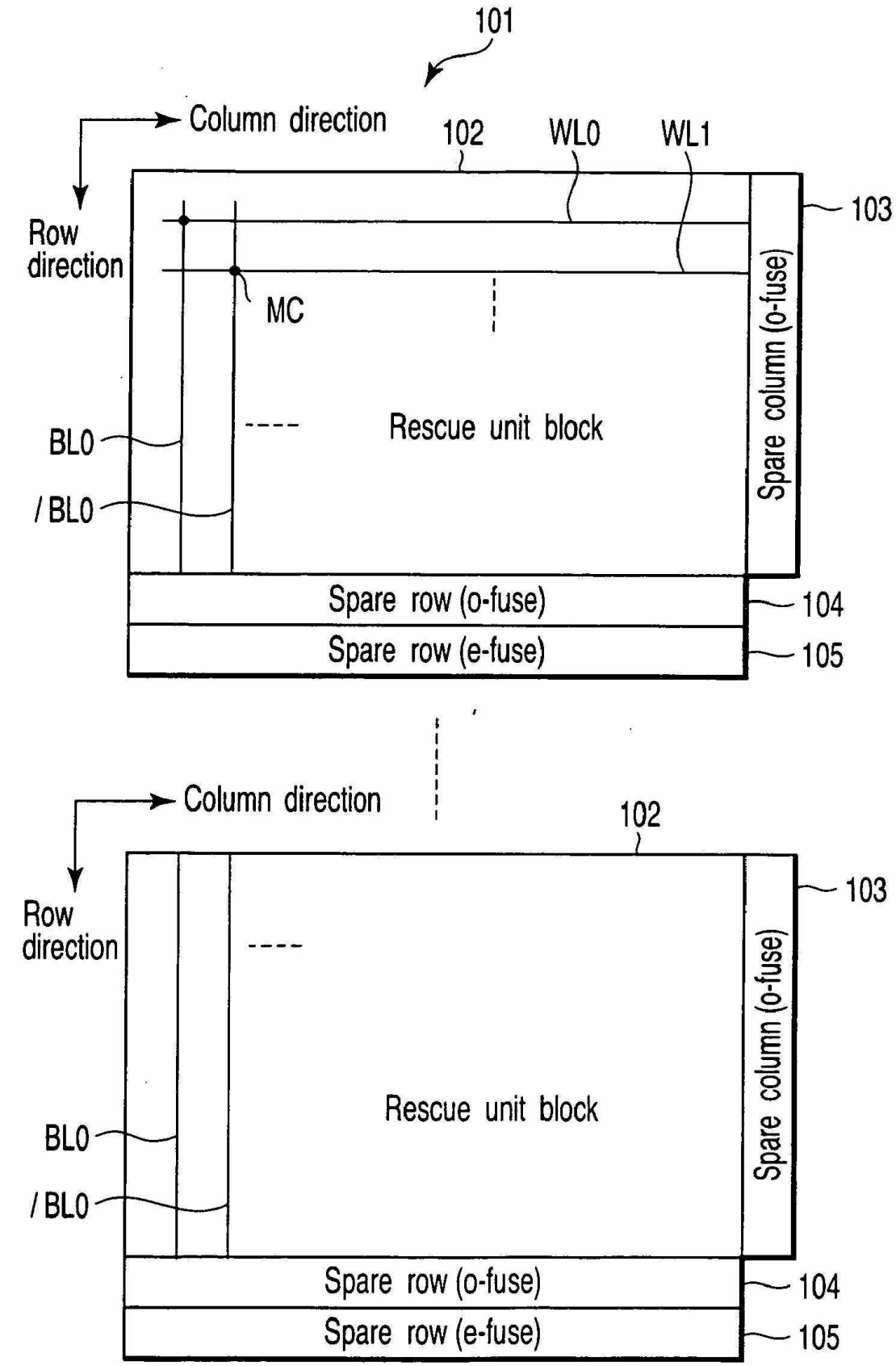
G11C 2229/766

Laser fuses

Definition statement

This subclass/group covers:
See US2008180983 (figure 2), US2006221729 (figure 3).




101
Column direction
102
WL0
WL1
Row direction
103
MC
BL0
/BL0
Rescue unit block
Spare column (o-fuse)
Spare row (o-fuse)
104
Spare row (e-fuse)
105
Column direction
102
Row direction
103
BL0
/BL0
Rescue unit block
Spare column (o-fuse)
Spare row (o-fuse)
104
Spare row (e-fuse)
105