G11C  STATIC STORES (information storage based on relative movement between record carrier and transducer G11B; semiconductor devices for storage H01L, e.g. H01L 27/108 - H01L 27/11597; pulse technique in general H03K, e.g. electronic switches H03K 17/00)

NOTES
1. This subclass covers devices or arrangements for storage of digital or analogue information in which no relative movement takes place between an information storage element and a transducer; which incorporate a selecting-device for writing-in or reading-out the information into or from the store
2. This subclass does not cover elements not adapted for storage and not provided with such means as referred to in Note (3) below, which elements are classified in the appropriate subclass, e.g. of H01, H03K.
3. In this subclass, the following terms are used with the meaning indicated:
   - "storage element" is an element which can hold at least one item of information and is provided with means for writing-in or reading-out this information;
   - "memory" is a device, including storage elements, which can hold information to be extracted when desired.

WARNING
The following IPC groups are not used in the CPC scheme. Subject matter covered by these groups is classified in the following CPC groups:

G11C 8/02 covered by G11C 8/00, H03K 17/00
G11C 11/4193 covered by G11C 11/00
G11C 11/4195 covered by G11C 11/00
G11C 11/4197 covered by G11C 11/00

5/00 Details of stores covered by G11C 11/00
5/005 . . (Circuit means for protection against loss of information of semiconductor storage devices (manufacturing semi-conductor by using bombardement with radiation H01L 21/26; error detection, monitoring G06F 11/00))
5/02 . . Disposition of storage elements, e.g. in the form of a matrix array
5/025 . . . (Geometric lay-out considerations of storage-and peripheral-blocks in a semiconductor storage device (geometrical lay-out of the components in integrated circuits, H01L 27/0207))
5/04 . . . Supports for storage elements, Supports for storage elements, [e.g. memory modules]: Mounting or fixing of storage elements on such supports
5/05 . . . Supporting of cores in matrix
5/06 . . . Arrangements for interconnecting storage elements electrically, e.g. by wiring
5/063 . . . (Voltage and signal distribution in integrated semi-conductor memory access lines, e.g. word-line, bit-line, cross-over resistance, propagation delay)
5/066 . . . (Means for reducing external access-lines for a semiconductor memory clip, e.g. by multiplexing at least address and data signals)
5/08 . . . for interconnecting magnetic elements, e.g. toroidal cores
5/10 . . for interconnecting capacitors
5/12 . . Apparatus or processes for interconnecting storage elements, e.g. for threading magnetic cores
5/14 . . Power supply arrangements (in general G05F, H02L, H02M), [e.g. Power down/chip (de)selection, layout of wiring/power grids, multiple supply levels]
5/141 . . . (Battery and back-up supplies (back-up supplies per se H021 J 9/061))
5/142 . . . (Contactless power supplies, e.g. RF, induction, IR (in general H02J 5/00))
5/143 . . . (Detection of memory cassette insertion/removal; Continuity checks of supply and ground lines (in general G01R 31/02); Detection of supply variations/interruptions/levels (G11C 5/148 takes precedence); Switching between alternative supplies (back-up supplies per se H02J 9/061); (G11C 5/141 takes precedence))
5/144 . . . (Detection of predetermined disconnection or reduction of power supply, e.g. power down or power standby)
5/145 . . . (Applications of charge pumps (charge pumps per se H02M 3/07); Boosted voltage circuits (for logic circuits or inverting circuits H03K 19/00); Clamp circuits therefor (G11C 5/141 takes precedence))
5/146 . . . (Substrate bias generators (G11C 5/141 takes precedence; in general G05F 3/205))
G11C 11/4063
G11C 11/413

Arrangements for writing information into, or reading information out from, a digital store (G11C 5/00 takes precedence; auxiliary circuits for stores using semiconductor devices G11C 11/4063, G11C 11/413)

7/005 . . . [with combined beam-and-individual cell access]
7/002 . . . with means for avoiding parasitic signals
7/004 . . . with means for avoiding disturbances due to temperature effects

7/006 . . . Sense amplifiers; Associated circuits, [e.g. timing or triggering circuits] (amplifiers per se H03F, H03K)
7/002 . . . [Differential amplifiers of non-latching type, e.g. comparators, long-tailed pairs]
7/005 . . . [Differential amplifiers of latching type]
7/007 . . . [Single-ended amplifiers]
7/008 . . . Control thereof

7/10 . . . Input/output (I/O) data interface arrangements, e.g. I/O data control circuits, I/O data buffers (level conversion circuits in general H03K 19/0175)

7/1003 . . . [Interface circuits for daisy chain or ring bus memory arrangements]
7/1006 . . . [Data managing, e.g. manipulating data before writing or reading out, data bus switches or control circuits therefor]
7/1009 . . . [Data masking during input/output]
7/1012 . . . [Data reordering during input/output, e.g. crossbars, layers of multiplexers, shifting or rotating]

7/1015 . . . [Read-write modes for single port memories, i.e. having either a random port or a serial port]
7/1018 . . . [Serial bit line access mode, e.g. using bit line address shift registers, bit line address counters, bit line burst counters]
7/1021 . . . [Page serial bit line access mode, i.e. using an enabled row address stroke pulse with its associated word line address and a sequence of enabled column address stroke pulses each with its associated bit line address]

7/1024 . . . [Extended data output [EDO] mode, i.e. keeping output buffer enabled during an extended period of time]
7/1027 . . . [Static column decode serial bit line access mode, i.e. using an enabled row address stroke pulse with its associated word line address and a sequence of enabled bit line addresses]

7/103 . . . [using serially addressed read-write data registers (G11C 7/1036 takes precedence)]
7/1033 . . . [using data registers of which only one stage is addressed for sequentially outputting data from a predetermined number of stages, e.g. nibble read-write mode]
7/1036 . . . [using data shift registers]

7/1039 . . . [using pipelining techniques, i.e. using latches between functional memory parts, e.g. row/column decoders, I/O buffers, sense amplifiers]
11/00 Digital stores characterised by the use of particular electric or magnetic storage elements; Storage elements therefor

11/02 . using magnetic elements { (using multibit magnetic storage elements G11C 11/5607; counters with magnetic elements H03K 23/76; pulse generators, static switches, logic circuits with such elements H03K 3/45, H03K 17/80, H03K 19/16; measurement of magnetic variables G01R 33/00) }

11/04 . using rod-type storage elements { (contains no documents; see G11C 11/06085, G11C 11/14, G11C 11/151) }

11/06 . using single-aperture storage elements, e.g. ring core; using multi-aperture plates in which each individual aperture forms a storage element

11/06007 . . . . [using a single aperture or single magnetic closed circuit]

NOTE

Provisionally contains the following details; control write -, read -, address circuitry (pulse generators in general H03K 5/80, H03K 17/00); arrangements for temperature compensation; checking of the correct functioning and repair arrangements (checking methods in general G06F 11/00, G06F 11/28; testing magnetic elements per se G01R 33/00); magnetic properties, choice of materials or the like (materials per se H01F 1/00)

11/06014 . . . . [using one such element pro bit]
11/06021 . . . . . [. with destructive read-out]
11/06028 . . . . . . [Matrixes]
using electric elements (containing no documents, see G11C 11/20)

using parametrons, i.e. ferroresonant triggers; with overcritica feedback magnetic amplifiers or similar (pulse generators using parametrons and ferroresonant devices H03K 19/162, H03K 19/164; counters using such elements H03K 23/001)

using electric elements (using multibit ferroelectric storage elements G11C 11/5657; pulse generators using ferroelectric elements H03K 3/45; counters using such elements H03K 23/76)

using ferroelectric elements (using ferroelectric capacitors)

using MOS with ferroelectric gate insulating film

using non-linear reactive devices in resonant circuits (contains no documents, see G11C 11/20)

using parametrons, i.e. ferroresonant triggers; with overcritica feedback magnetic amplifiers or similar (pulse generators using parametrons and ferroresonant devices H03K 19/162, H03K 19/164; counters using such elements H03K 23/001)

using electric elements (using semiconductor devices (processes or apparatus for the manufacture or treatment of semiconductor or solid states devices H01L 21/00; integrated circuit devices H01L 27/00; generating electric pulses, e.g. bistable devices using semiconductor devices H03K 3/00))

using charge storage in a depletion layer, e.g. charged coupled devices (in shift registers G11C 19/282)

using diodes, e.g. as threshold elements (i.e. diodes assuming a stable ON-stage when driven above their threshold (S- or N-characteristic))

using tunnel diodes

using thyristors (or the avalanche or negative resistance type, e.g. PNPN, SCR, SCS, UJT)

using transistors

forming cells needing refreshing or charge regeneration (i.e. dynamic cells)

with charge regeneration individual to each memory cell, i.e. internal refresh

using field effect transistors

using bipolar transistors

with charge regeneration common to a multiplicity of memory cells, i.e. external refresh

with one charge-transfer gate, e.g. MOS transistor, per cell

using a plurality of serially connected access transistors, each having a storage capacitor

WARNING
Not complete, see also G11C 11/404

using three charge-transfer gates, e.g. MOS transistors, per cell

Management or control of the refreshing or charge-regeneration cycles

[Arbitration, priority and concurrent access to memory cells for read/write or refresh operations]

[Refresh operations in memory devices with an internal cache or data buffer]

[External triggering or timing of internal or partially internal refresh operations, e.g. auto-refresh or CAS-before-RAS triggered refresh]

[Internal triggering or timing of refresh, e.g. hidden refresh, self refresh, pseudo-SRAMs]

[Refresh operations over multiple banks or interleaving]

[Partial refresh of memory arrays]

[Temperature related aspects of refresh operations]

Auxiliary circuits, e.g. for addressing, decoding, driving, writing, sensing or timing

for memory cells of the bipolar type

for memory cells of the field-effect type

Circuits or initialisation, powering up or down, clearing memory or resetting.
Schmitt trigger regeneration, e.g. bistable multivibrator or 

timing, power reduction (in general 
decoding, driving, writing, sensing, 
Auxiliary circuits, e.g. for addressing, 
- G11C 8/00

image memory G11C 7/20

for memory cells of the bipolar type 

protection against loss of information (in 
{Cells incorporating circuit means for 
protection against loss of information (in 
general G11C 5/00)}

T2L, ECL}

transistors or via multiple emitters, e.g. 
{with at least one cell access to base 
and/or collector of at least one of said 
transistors, e.g. via access diodes, access 
transistors)}

using bipolar transistors only 

form (static) cells with positive feedback, 
i.e. cells not needing refreshing or charge 
regeneration, e.g. bistable multivibrator or 
Schmitt trigger

using field-effect transistors only ((latent 
image memory G11C 7/20; multi-port 
cells G11C 8/16))

{Cells incorporating circuit means for 
protection against loss of information (in 
general G11C 5/00/5)}

Auxiliary circuits, e.g. for addressing, 
decoding, driving, writing, sensing, 
timing, power reduction (in general 
G11C 5/00 - G11C 5/00)

for memory cells of the bipolar type 

Address circuits

Read-write circuits

for memory cells of the field-effect type 

Address circuits

Read-write circuits

using opto-electronic devices, i.e. light-emitting 
and photoelectric devices electrically - or 
 optically - (feedback) coupled

using super-conductive elements, e.g. cryotron 
{(pulse generators using such elements 
H03K 3/38; counters H03K 23/001)}

using thermoplastic elements

using placeable coupling elements, e.g. 
ferromagnetic cores, to produce change between 
different states of mutual or self-inductance 
[(contains no documents; see G11C 17/00 and 
subgroups)]

using actuation of electric contacts to store the 
information (mechanical stores G11C 23/00; 
switches providing a selected number of 
consecutive operations of the contacts by a single 
manual actuation of the operating part H01H 41/00)

using electromagnetic relays

using elements simulating biological cells, e.g. 
neuron

using storage elements with more than two 
stable states represented by steps, e.g. of voltage, 
current, phase, frequency (counting arrangements 
comprising multi-stable elements of this type 
H03K 25/00), H03K 29/00)

using magnetic storage elements

using conductive bridging RAM [CBRAM] or 
programming metallization cells [PMC]

using charge storage in a floating gate

[Programming or writing circuits; Data input 
circuits]

[Erasing circuits]

[Reading or sensing circuits; Data output 
circuits]

using capacitive charge storage elements]

using ferroelectric storage elements]

using organic memory material storage 
elements]

using charge trapping in an insulator]

using amorphous/crystalline phase transition 
storage elements]

using storage elements comprising metal oxide 
memory material, e.g. perovskites]

(read-only digital stores using storage elements 
with more than two stable states)

Digital stores characterised by the use of storage 
elements not covered by groups G11C 11/00, 
G11C 23/00 - G11C 25/00

using resistance random access memory [RRAM] 
elements]

comprising amorphous/crystalline phase 
transition cells]

comprising metal oxide memory material, e.g. 
perovskites]

[RRAM elements whose operation depends upon 
chemical change]

comprising conductive bridging RAM 
[CBRAM] or programming metallization cells 
[PMCs]}

G11C
Digital stores characterised by arrangements of cells having volatile and non-volatile storage properties for back-up when the power is down

14/00

14/0009 . . . (in which the volatile element is a DRAM cell)
14/0018 . . . (and the nonvolatile element is an EEPROM element, e.g. a floating gate or MNOS transistor)
14/0027 . . . (and the nonvolatile element is a ferroelectric element)
14/0036 . . . (and the nonvolatile element is a magnetic RAM [MRAM] element or ferromagnetic cell)
14/0045 . . . (and the nonvolatile element is a resistive RAM element, i.e. programmable resistors, e.g. formed of phase change or chalcogenide material)
14/0054 . . . (in which the volatile element is a SRAM cell)
14/0056 . . . (and the nonvolatile element is an EEPROM element, e.g. a floating gate or MNOS transistor)
14/0072 . . . (and the nonvolatile element is a ferroelectric element)
14/0081 . . . (and the nonvolatile element is a magnetic RAM [MRAM] element or ferromagnetic cell)
14/009 . . . (and the nonvolatile element is a resistive RAM element, i.e. programmable resistors, e.g. formed of phase change or chalcogenide material)

15/00

Digital stores in which information comprising one or more characteristic parts is written into the store and in which information is read-out by searching for one or more of these characteristic parts, i.e. associative or content-addressed stores (in which information is addressed to a specific location G11C 11/00; selection information using addressing means, e.g. hashing, tree addressing, chaining G06F 11/22; information retrieval systems using a computer G06F 17/30)
16/00 Erasable programmable read-only memories
(G11C 14/00 takes precedence)

16/02 . . . electrically programmable ((programmable multibit digital storage elements G11C 11/5621))

16/04 . . . using variable threshold transistors, e.g. FAMOS

16/0408 . . . . [comprising cells containing floating gate transistors (G11C 16/0483; G11C 16/0491 take precedence)]

16/0416 . . . . [comprising cells containing a single floating gate transistor and no select transistor, e.g. UV EPROM]

16/0425 . . . . [comprising cells containing a merged floating gate and select transistor]

16/0433 . . . . [comprising cells containing a single floating gate transistor and one or more separate select transistors]

16/0441 . . . . [comprising cells containing multiple floating gate devices, e.g. separate read-and-write FAMOS transistors with connected floating gates]

16/045 . . . . . {Floating gate memory cells with both P and N channel memory transistors, usually sharing a common floating gate}

16/0458 . . . . . {comprising plural independent floating gates which store independent data (for storage of more than two stable states at a single floating gate G11C 11/5621)}

16/0466 . . . . . [comprising cells with charge storage in an insulating layer, e.g. MNOS, SNOS (G11C 16/0483; G11C 16/0491 take precedence)]

16/0475 . . . . . [comprising plural independent storage sites which store independent data (for storage of more than two stable states at a single storage site G11C 11/5621)]

16/0483 . . . . . [comprising cells having several storage transistors connected in series]

16/0491 . . . . . [Virtual ground arrays]

16/06 . . . . . . Auxiliary circuits, e.g. for writing into memory (in general G11C 7/00)

16/08 . . . . . . Address circuits; Decoders; Word-line control circuits

16/10 . . . . . . Programming or data input circuits

16/102 . . . . . . [External programming circuits, e.g. EPROM programmers; In-circuit programming or reprogramming; EPROM emulators]

16/105 . . . . . . {Circuits or methods for updating contents of nonvolatile memory, especially with ‘security’ features to ensure reliable replacement, i.e. preventing that old data is lost before new data is reliably written]

16/107 . . . . . . [Programming all cells in an array, sector or block to the same state prior to flash erasing]

16/12 . . . . . . Programming voltage switching circuits

16/14 . . . . . . Circuits for erasing electrically, e.g. erase voltage switching circuits

16/16 . . . . . . for erasing blocks, e.g. arrays, words, groups
16/3468  . . . .  [Prevention of overerasure or overprogramming, e.g. by verifying whilst erasing or writing]
16/3472  . . . . .  [Circuits or methods to verify correct erasure of nonvolatile memory cells whilst erasing is in progress, e.g. by detecting onset or cessation of current flow in cells and using the detector output to terminate erasure]
16/3477  . . . . .  [Circuits or methods to prevent overerasing of nonvolatile memory cells, e.g. by detecting onset or cessation of current flow in cells and using the detector output to terminate erasure]
16/3481  . . . . .  [Circuits or methods to verify correct programming of nonvolatile memory cells whilst programming is in progress, e.g. by detecting onset or cessation of current flow in cells and using the detector output to terminate programming]
16/3486  . . . . .  [Circuits or methods to prevent overprogramming of nonvolatile memory cells, e.g. by detecting onset or cessation of current flow in cells and using the detector output to terminate programming]
16/349  . . . .  [Arrangements for evaluating degradation, retention or wearout, e.g. by counting erase cycles]
16/3495  . . . . .  [Circuits or methods to detect or delay wearout of nonvolatile EPROM or EEPROM memory devices, e.g. by counting numbers of erase or reprogram cycles, by using multiple memory areas serially or cyclically]

17/00  Read-only memories programmable only once; Semi-permanent stores, e.g. manually-replaceable information cards  ([multibit read-only memories G11C 11/5692; erasable programmable read-only memories G11C 16/00; coding, decoding or code conversion, in general H03M; combination of ROM and RAM G11C 11/005, G11C 14/00; for electrical control of combustion engines F02D 41/2406])
17/005 . . . .  [with a storage element common to a large number of data, e.g. perforated card (G11C 17/02, G11C 17/04 take precedence)]
17/002 . . . .  [using magnetic or induction elements (G11C 17/14 takes precedence)]
17/004 . . . .  [using capacitive elements (G11C 17/06, G11C 17/14 take precedence)]
17/006 . . . .  [using diode elements (G11C 17/14 takes precedence)]
17/008 . . . .  [using semiconductor devices, e.g. bipolar elements (G11C 17/06, G11C 17/14 take precedence)]
17/010 . . . . .  [in which contents are determined during manufacturing by a predetermined arrangement of coupling elements, e.g. mask-programmable ROM]
17/12 . . . . .  [using field-effect devices]
17/123 . . . . .  [comprising cells having several storage transistors connected in series]
17/126 . . . . .  [Virtual ground arrays]
17/14 . . . . .  in which contents are determined by selectively establishing, breaking or modifying connecting links by permanently altering the state of coupling elements, e.g. PROM
17/143 . . . .  [using laser-fusible links]
17/146 . . . .  [Write once memory, i.e. allowing changing of memory content by writing additional bits]
17/16 . . . . .  [using electrically-fusible links]
17/165 . . . . .  [Memory cells which are electrically programmed to cause a change in resistance, e.g. to permit multiple resistance steps to be programmed rather than conduct to or from non-conduct change of fuses and antifuses (digital stores using resistance random access memory elements G11C 13/0002)]
17/178 . . . .  Auxiliary circuits, e.g. for writing into memory (in general G11C 7/00)
19/001  Digital stores in which the information is moved stepwise, e.g. shift register (counting chains H03K 23/00; stack stores, push-down stores (linear pulse counters H03K 23/54, pulse distributors H03K 5/15, methods and arrangements for shifting data G06F 5/01))
19/005 . . . .  [with ferro-electric elements (condensers)]
19/02 . . . . .  [using magnetic elements (G11C 19/14 takes precedence)]
19/04 . . . . .  [using cores with one aperture or magnetic loop]
19/06 . . . . .  [using structures with a number of apertures or magnetic loops, e.g. transflectors (laddic)]
19/08 . . . . .  [using thin films in plane structure (thin magnetic films and apparatus or processes specially adapted for manufacturing or assembling the same H01F 10/00, H01F 41/14)]
19/0808 . . . . .  [using magnetic domain propagation]
19/0816 . . . . .  [using a rotating or alternating coplanar magnetic field]
19/0825 . . . . .  [using a variable perpendicular magnetic field]
19/0833 . . . . .  [using magnetic domain interaction]
19/0841 . . . . .  [using electric current]
19/085 . . . . .  [Generating magnetic fields therefor, e.g. uniform magnetic field for magnetic domain stabilisation (coil construction H01F 5/00; electromagnets H01F 7/00)]
19/0858 . . . . .  [Generating, replicating or annihilating magnetic domains (also comprising different types of magnetic domains, e.g. “Hard Bubbles”) (G11C 19/0866 takes precedence)]
19/0866 . . . . .  [Detecting magnetic domains (measuring or detecting magnetic fields in general G01R 3/02)]
19/0875 . . . . .  [Organisation of a plurality of magnetic shift registers (FIFO G06F 5/06; LIFO G06F 7/78)]
19/0883 . . . . .  [Means for switching magnetic domains from one path into another path, i.e. transfer switches, swap gates, decoders (logic circuits using magnetic domains H03K 19/168)]
19/0891 . . . . .  [using hybrid structure, e.g. ion doped layers]
19/090 . . . . .  [using thin films on rods; with twistors]
19/0912 . . . . .  [using non-linear reactive devices in resonant circuits (e.g. parametrons; magnetic amplifiers with overcritical feedback)]
using magnetic elements in combination with active elements, e.g. discharge tubes, semiconductor elements {contains no documents, see provisionally G11C 19/02 - G11C 19/10)

using capacitors as main elements of the stages {if capacitors are used as auxiliary stage in between main stages with other elements, the latter take precedence; G11C 19/005 takes precedence)

in combination with semiconductor elements, e.g. bipolar transistors, diodes)

with field-effect transistors, e.g. MOS-FET

using only one transistor per capacitor, e.g. bucket brigade shift register)

Organisation of a multiplicity of shift registers, e.g. regeneration, timing, input-output circuits (FIFO G06F 5/06; LIFO G06F 7/78)

using discharge tubes (G11C 19/14 takes precedence)

using gas-filled tubes (G11C 19/207 takes precedence)

using super-conductive elements

using storage elements with more than two stable states represented by steps, e.g. of voltage, phase, frequency {in RAM multistable cells G11C 11/55; in capacitive analog stores G11C 27/04)}

two-dimensional, e.g. horizontal and vertical shift registers

Digital stores in which the information circulates {continuously} (stepwise G11C 19/00)

using electrical delay line (construction of such lines H03H 7/30, H03H 11/26)

using electromechanical delay lines, e.g. using a mercury tank {construction of such lines H03H 9/00)

using piezo-electro transducers, e.g. mercury tank

using magnetostriction transducers, e.g. nickel delay line

Digital stores characterised by movement of mechanical parts to effect storage, e.g. using balls; Storage elements therefor (storing by actuating contacts G11C 11/50)

Digital stores characterised by the use of flowing media; Storage elements therefor {multiple fluid-circuit element arrangements for performing digital operations F15C 11/12)}

Electric analogue stores, e.g. for storing instantaneous values {integrating circuits acting as stores G06G 7/18; pulse counters with step by step integration and static storage H03K 25/00)

with non-volatile charge storage, e.g. on floating gate or MNOS

Sample-and-hold arrangements (G11C 27/04 takes precedence; sampling electrical signals, in general H03K)

using a magnetic memory element

using a capacitive memory element (G11C 27/04 takes precedence)

associated with an amplifier (G11C 27/028 takes precedence)

Current mode circuits, e.g. switched current memories

Shift registers (charge coupled devices per se H01L 29/76)

Checking stores for correct operation; Subsequent repair; Testing stores during standby or offline operation {testing of electronic circuits in general G01R 31/28; error detection or error correction in computer memories during normal operation G06F 11/1008, G06F 11/1666; testing of computers during standby G06F 11/223)

in serial memories)

at wafer scale level, i.e. WSI (for test and configuration during manufacture H01L 22/00)

Detection or location of defective auxiliary circuits, e.g. defective refresh counters

in voltage or current generators

in I/O circuitry

in clock generator or timing circuitry

in decoders

in signal lines

in sense amplifiers

in fuses

with adaption or trimming of parameters

Detection or location of defective memory elements, e.g. cell constructio details, timing of test signals

in embedded memories

during or with feedback to manufacture

comprising complete test loop

on power on

{Online test}

Online error correction

Acceleration testing

Functional testing, e.g. testing during refresh, power-on self testing [POST] or distributed testing

Test algorithms, e.g. memory scan (MScan) algorithms; Test patterns, e.g. checkerboard patterns

Built-in arrangements for testing, e.g. built-in self testing [BIST] {or interconnection details

comprising voltage or current generators

comprising I/O circuitry

comprising clock generation or timing circuitry

Word line control

Bit line control

Location of test circuitry on chip or wafer
29/1208 . . . . [Error catch memory]
29/14 . . . . Implementation of control logic, e.g. test mode decoders
29/16 . . . . using microprogrammed units, e.g. state machines
29/18 . . . . Address generation devices; Devices for addressing circuits
29/1802 . . . . [Address decoder]
29/1804 . . . . [Manipulation of word size]
29/1806 . . . . [Address conversion or mapping, i.e. logical to physical address]
29/20 . . . . using counters or linear-feedback shift registers [LFSR]
29/22 . . . . Accessing serial memories
29/24 . . . . Accessing extra cells, e.g. dummy cells or redundant cells
29/26 . . . . Accessing multiple arrays (G11C 29/24 takes precedence)
29/2602 . . . . [Concurrent test]
29/28 . . . . Dependent multiple arrays, e.g. multi-bit arrays
29/30 . . . . Accessing single arrays
29/32 . . . . Serial access; Scan testing
29/3202 . . . . [Scan chain]
29/34 . . . . Accessing multiple bits simultaneously
29/36 . . . . Data generation devices, e.g. data inverters
29/3602 . . . . [Pattern generator]
29/38 . . . . Response verification devices
29/40 . . . . using compression techniques
29/4002 . . . . [Comparison of products, i.e. test results of chips or with golden chip]
29/42 . . . . using error correcting codes [ECC] or parity check
29/44 . . . . Indication or identification of errors, e.g. for repair
29/4401 . . . . [for self repair]
29/4402 . . . . [Internal storage of test result, quality data, chip identification, repair information]
29/46 . . . . Test trigger logic
29/48 . . . . Arrangements in static stores specially adapted for testing by means external to the store, e.g. using direct memory access [DMA] or using auxiliary access paths (external testing equipment G11C 29/56)
29/50 . . . . Marginal testing, e.g. race, voltage or current testing
29/50004 . . . . [of threshold voltage]
29/50008 . . . . [of impedance]
29/50012 . . . . [of timing]
29/50016 . . . . [of retention]
29/5002 . . . . [Characteristic]
29/5004 . . . . [Voltage]
29/5006 . . . . [Current]
29/52 . . . . Protection of memory contents; Detection of errors in memory contents
29/54 . . . . Arrangements for designing test circuits, e.g. design for test [DFT] tools
29/56 . . . . External testing equipment for static stores, e.g. automatic test equipment [ATE]; Interfaces therefor
29/56004 . . . . [Pattern generation]
29/56008 . . . . [Error analysis, representation of errors]
29/56012 . . . . [Timing aspects, clock generation, synchronisation]
29/56016 . . . . [Apparatus features]
29/5602 . . . . [Interface to device under test]
29/5604 . . . . [Display of error information]
29/5606 . . . . [Error catch memory]
29/70 . . . . [Masking faults in memories by using spares or by reconfiguring]
29/702 . . . . [by replacing auxiliary circuits, e.g. spare voltage generators, decoders or sense amplifiers, to be used instead of defective ones]
29/72 . . . . [with optimized replacement algorithms]
29/74 . . . . [with duplex memories, i.e. using dual copies]
29/76 . . . . [using address translation or modifications]
29/765 . . . . [in solid state disks]
29/78 . . . . [using programmable devices]
29/781 . . . . [combined in a redundant decoder]
29/783 . . . . [with refresh of replacement cells, e.g. in DRAMs]
29/785 . . . . [with redundancy programming schemes]
29/787 . . . . [using a fuse hierarchy (for memories using fuses in general G11C 17/16)]
29/789 . . . . [using non-volatile cells or latches (erasable programmable memory cells in general G11C 16/00)]
29/80 . . . . [with improved layout]
29/802 . . . . [by encoding redundancy signals]
29/804 . . . . [to prevent clustered faults]
29/806 . . . . [by reducing size of decoders]
29/808 . . . . [using a flexible replacement scheme]
29/81 . . . . [using a hierarchical redundancy scheme]
29/812 . . . . [using a reduced amount of fuses]
29/814 . . . . [for optimized yield]
29/816 . . . . [for an application-specific layout]
29/818 . . . . [for dual-port memories]
29/82 . . . . [for EEPROMs]
29/822 . . . . [for read only memories]
29/824 . . . . [for synchronous memories]
29/83 . . . . [with reduced power consumption]
29/832 . . . . [with disconnection of faulty elements]
29/835 . . . . [with roll call arrangements for redundant substitutions]
29/838 . . . . [with substitution of defective spares]
29/84 . . . . [with improved access time or stability]
29/842 . . . . [by introducing a delay in a signal path]
29/844 . . . . [by splitting the decoders in stages]
29/846 . . . . [by choosing redundant lines at an output stage]
29/848 . . . . [by adjacent switching]
29/86 . . . . [in serial access memories, e.g. shift registers, CCDs, bubble memories]
29/88 . . . . [with partially good memories]
29/883 . . . . [using a single defective memory device with reduced capacity, e.g. half capacity]
29/886 . . . . [combining plural defective memory devices to provide a contiguous address range, e.g. one device supplies working blocks to replace defective blocks in another device]
99/00 Subject matter not provided for in other groups of this subclass
G11C

Indexing scheme relating to arrangements for writing information into, or reading information out from, a digital store

- Isolation gates, i.e. gates coupling bit lines to the sense amplifier
- Transfer gates, i.e. gates coupling the sense amplifier output to data lines, I/O lines or global bit lines
- Register arrays
- Sense amplifier related aspects
- Sense amplifier enabled by a address transition detection related control signal
- Current sense amplifiers
- Sense amplifier drivers
- Frequency reading type sense amplifier
- Integrator type sense amplifier
- Aspects relating to interfaces of memory device to external buses
- Analog or multilevel bus
- Compression or decompression of data before storage
- Embedded memory devices, e.g. memories with a processing device on the same die or ASIC memory designs
- Aspects related to pads, pins or terminals
- Serial-parallel conversion of data or prefetch
- Wide data ports
- Equalization of bit lines
- Solid state audio (deprecated, only for historical reasons, G06F 3/16, G11B)
- Control and timing of internal memory operations
- Concurrent read and write (for multi-port memory G11C 7/1075)
- Late write
- Standby or low power modes
- Copy
- Memory devices with an internal cache buffer
- Calibration
- Write conditionally, e.g. only if new data and old data differ
- Latency related aspects
- Timing of a read operation (sense amplifier timing G11C 7/06, G11C 7/08)
- Timing of a write operation (sense amplifier timing G11C 7/06, G11C 7/08)

Indexing scheme relating to digital stores characterized by the use of particular electric or magnetic storage elements; Storage elements therefor

- Indexing scheme relating to cells needing refreshing or charge regeneration, i.e. dynamic cells
- Memory devices with multiple cells per bit, e.g. twin-cells
- Memory devices with silicon-on-insulator cells
- Refreshing of dynamic cells
- Calibration or ate or cycle tuning
- Parity or ECC in refresh operations
- Interleaved refresh operations
- Low level details of refresh operations
- Pseudo-SRAMs
- Refresh in standby or low power modes
- Voltage or leakage in refresh operations

Indexing scheme relating to G11C 13/00 for features not covered by this group

- Resistive cells; Technology aspects
Resistive cell structure aspects

Array wherein each memory cell has more than one access device

Non-metal ion trapping, i.e. using memory material trapping non-metal ions given by the electrode or another layer during a write operation, e.g. trapping, doping

Dissociation, i.e. using memory material including molecules which, during a write operation, are dissociated in ions which migrate further in the memory material

Use of different molecule structures as storage states, e.g. part of molecule being rotated

Memory cell being a nanotube, e.g. suspended nanotube

Memory cell being a nanowire transistor

Memory cell being a nanowire having RADIAL composition

Memory cell comprising at least a nanowire and only two terminals

Resistive cell, memory material aspects

Material including silicon

Material includes an oxide or a nitride

Material having simple binary metal oxide structure

Material including carbon, e.g. graphite, graphene

Resistive cell structure aspects

Structure including a barrier layer preventing or limiting migration, diffusion of ions or charges or formation of electrolytes near an electrode

Structure characterized by the electrode material, shape, etc.

Structure wherein the resistive material being in a transistor, e.g. gate

Structure including a tunneling barrier layer, the memory effect implying the modification of tunnel barrier conductivity

Structure including two electrodes, a memory active layer and at least two other layers which can be a passive or source or reservoir layer or a less doped memory active layer

Structure including two electrodes, a memory active layer and a so called passive or source or reservoir layer which is NOT an electrode, wherein the passive or source or reservoir layer is a source of ions which migrate afterwards in the memory active layer to be only trapped there, to form conductive filaments there or to react with the material of the memory active layer in redox way

Resistive array aspects

Three dimensional array

Array wherein the access device being a diode

Array where access device function, e.g. diode function, being merged with memorizing function of memory element

Array wherein each memory cell has more than one access device

Array having a NAND structure comprising, for example, memory cells in series or memory elements in series, a memory element being a memory cell in parallel with an access transistor

Array using an access device for each cell which being not a transistor and not a diode

Array wherein the memory element being directly connected to the bit lines and word lines without any access device being used

Array wherein the memory cells of a group share an access device, all the memory cells of the group having a common electrode and the access device being not part of a word line or a bit line driver

Array wherein the access device being a transistor

Array wherein the substrate, the cell, the conductors and the access device are all made up of organic materials

Array wherein the array conductors, e.g. word lines, bit lines, are made of nanowires

Array having, for accessing a cell, a word line, a bit line and a plate or source line receiving different potentials

Resistive cell, memory material aspects

Array having multiple OTP blocks permitting limited update

Current-voltage curve

Use of different molecule structures as storage states, e.g. part of molecule being rotated

Material including silicon

Material includes an oxide or a nitride

Material having simple binary metal oxide structure

Material including carbon, e.g. graphite, graphene

Resistive cell structure aspects

Structure including a barrier layer preventing or limiting migration, diffusion of ions or charges or formation of electrolytes near an electrode

Structure characterized by the electrode material, shape, etc.

Structure wherein the resistive material being in a transistor, e.g. gate

Structure including a tunneling barrier layer, the memory effect implying the modification of tunnel barrier conductivity

Structure including two electrodes, a memory active layer and at least two other layers which can be a passive or source or reservoir layer or a less doped memory active layer

Structure including two electrodes, a memory active layer and a so called passive or source or reservoir layer which is NOT an electrode, wherein the passive or source or reservoir layer is a source of ions which migrate afterwards in the memory active layer to be only trapped there, to form conductive filaments there or to react with the material of the memory active layer in redox way

Resistive array aspects

Three dimensional array

Array wherein the access device being a diode

Array where access device function, e.g. diode function, being merged with memorizing function of memory element

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Array having a NAND structure comprising, for example, memory cells in series or memory elements in series, a memory element being a memory cell in parallel with an access transistor

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Array wherein the access device being a transistor

Array wherein the substrate, the cell, the conductors and the access device are all made up of organic materials

Array wherein the array conductors, e.g. word lines, bit lines, are made of nanowires

Array having, for accessing a cell, a word line, a bit line and a plate or source line receiving different potentials
Floating gate memory programmed by reverse programming, e.g. programmed with negative gate voltage and erased with positive gate voltage or programmed with high source or drain voltage and erased with high gate voltage.

Reduction of number of input/output pins by using a serial interface to transmit or receive addresses or data, i.e. serial access memory.

Indexing scheme relating to checking stores for correct operation, subsequent repair or testing stores during standby or offline operation.

Indexing scheme relating to G11C 29/70, for implementation aspects of redundancy repair.

Location of redundancy information.

Redundancy information stored in a part of the memory core to be repaired.

Redundancy information loaded from the outside into the memory.

Time at which the repair is done.

After packaging.

Before packaging.

Storage technology used for the repair.

E-fuses, e.g. electric fuses or antifuses, floating gate transistors.

Laser fuses.