

## H10B

### ELECTRONIC MEMORY DEVICES

#### Definition statement

*This place covers:*

Memory devices consisting of multiple semiconductor or solid-state components. This includes the multiple memory cells constituting the memory core region and logic components within the immediate peripheral region surrounding the memory core region. The memory cells have storage components therein, which may be accessed by selection components.

This includes the following kind of devices:

Volatile Memory Devices:

- Static random access memory
- Dynamic random access memory

Non-Volatile Memory Devices:

- Read-only memory [ROM]
- Programmable ROM [PROM]
- Erasable and programmable ROM [EPROM]
- Electrically erasable and programmable ROM [EEPROM]
- Ferroelectric memory, e.g. FeRAM or FeFET
- Magnetic random access memory [MRAM]
- Resistive random access memory [ReRAM or RRAM], phase change RAM [PRAM or PCRAM]

Assemblies of multiple devices comprising at least one memory device of this subclass.

Processes and apparatus specially adapted for the manufacture or treatment of such devices.

#### Relationships with other classification places

When the focus of the invention is on the structure of the device, classification is made in [H10B](#). When the focus of the invention is on the structures used for accessing the device, such as structures or circuits for reading, writing, or erasing data in the device, classification is made in [G11C](#).

#### References

##### Informative references

*Attention is drawn to the following places, which may be of interest for search:*

Circuits (e.g. data buffers, decoders, sense amplifiers) and accessing (e.g. read, write, and erase operations) of memory devices	<a href="#">G11C</a>
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#### Glossary of terms

*In this place, the following terms or expressions are used with the meaning indicated:*

Programming	Setting a desired state of a memory cell.
Writing, erasing	Changing the state of a memory cell, in a memory cell wherein programming can occur as many times as desired.

Core, core region	The portion of a memory cell having storage components, select components, or data lines such as bit lines and word lines. The core also includes devices for local accessing (e.g. reading, writing or erasing) of the storage elements, for example, select transistors of NAND strings or read/write ports of SRAM.
Peripheral region, periphery	The portion of a memory device outside the core region having devices or parts for global accessing (e.g. reading, writing, erasing) of the devices of the core region. It includes, e.g. word line drivers, multiplexers or sense amplifiers.
Boundary region between the core region and peripheral circuit region	The portion of a memory device that contains neither core devices (e.g. storage components or select components) nor peripheral devices (e.g. word line drivers or multiplexers), typically comprising structural parts such as bit line fan-outs between the core region and the peripheral region, or dummy elements or staircase structures for 3D NAND.

### Synonyms and Keywords

*In patent documents, the following abbreviations are often used:*

RAM	Random access memory
SRAM	Static RAM
DRAM	Dynamic RAM
ReRAM, RRAM	Resistive RAM
PRAM, PCRAM	Phase change RAM
FeRAM, FRAM	Ferroelectric RAM
CBRAM	Conductive-bridging RAM
MRAM	Magnetoresistive RAM
ROM	Read-only memory
PROM	Programmable ROM
MPROM	Mask-programmed ROM
OTPROM	One-time programmable ROM
EPROM	Erasable-and-programmable ROM
Volatile memory	Memory requiring power supply to maintain the stored information: it loses any written data when the system is turned off
Non-volatile memory	Memory not requiring power supply to maintain the stored information: it retains the written data even when the system is turned off
Ferroelectric memory capacitor	Capacitor with ferroelectric memory properties
Ferroelectric memory transistor	Transistor with ferroelectric memory properties embedded in a layer of the gate electrodes, e.g. in a MFS or MFMS layer
MFS	Metal-ferroelectric-semiconductor
MFIS	Metal-ferroelectric-insulator-semiconductor
MFMS	Metal-ferroelectric-metal-insulator-semiconductor

## H10B 10/00

### Static random access memory [SRAM] devices

#### Definition statement

*This place covers:*

Memory devices having multiple volatile memory cells, wherein, in each cell, the logic state is stored in one of two stable states of a cross-coupled inverter. SRAM cells commonly have four or more transistors.

#### References

##### Informative references

*Attention is drawn to the following places, which may be of interest for search:*

Circuits (e.g. data buffers, decoders, amplifiers) and accessing (e.g. read, write and erase operations) of SRAM devices	<a href="#">G11C 11/41</a>
Resistors for integrated circuits, and manufacturing or treatment thereof	<a href="#">H01L 28/20</a>

#### Synonyms and Keywords

*In patent documents, the following words/expressions are often used with the meaning indicated:*

Vcc or Vdd	High voltage supply
Vss	Low voltage (or ground) supply
Pull-up [PU]/Load	Refers to components in the flip-flop that are connected to Vcc
Pull-down [PD]/Drive	Refers to components in the flip-flop that are connected to Vss
Pass-gate [PG], access transistor/gate, select transistor/gate, transfer transistor/gate	Refers to transistors that control access to the flip-flop
Cross-coupled inverter (or Flip-flop or latch)	Bi-stable circuit used to store information

## H10B 12/00

### Dynamic random access memory [DRAM] devices

#### Definition statement

*This place covers:*

Dynamic memory devices having multiple volatile memory cells, wherein, each cell has:

- a storage component (e.g. capacitor) whose stored charge determines the logic state of the device; and
- at least one selection component (e.g. access transistor) for accessing the storage component.

#### References

##### Informative references

*Attention is drawn to the following places, which may be of interest for search:*

Circuits (e.g. data buffers, decoders, amplifiers) and accessing (e.g. read, write and erase operations) of DRAM devices	<a href="#">G11C 11/24</a> , <a href="#">G11C 11/401</a>
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Capacitors for integrated circuits, and manufacture or treatment thereof	<a href="#">H01L 28/40</a>
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## H10B 20/00

### Read-only memory [ROM] devices

#### Definition statement

*This place covers:*

Memory devices wherein data is stored even when power is removed (non-volatile), wherein the cells have components (e.g. fuses or anti-fuses) that are irreversibly changed during programming.

The group [H10B 20/00](#) itself covers memory devices wherein, after manufacturing, the operations are limited to read-only (e.g. mask ROM), because the programming thereof was performed during manufacturing. The groups [H10B 20/20](#) - [H10B 20/25](#) cover programmable ROM [PROM] wherein the memory may be programmed after manufacturing by a user.

ROM and PROM devices are typically programmable only once (though in some situations, a cell may have more than one element that may be irreversibly changed, so a very limited amount of "corrective" programming may occur). This is contrasted with EPROM and EEPROM devices, which can be writable or erasable many (e.g. millions of) times.

#### References

##### Informative references

*Attention is drawn to the following places, which may be of interest for search:*

Circuits (e.g. data buffers, decoders, amplifiers) and accessing (e.g. read, write and erase operations) of ROM devices	<a href="#">G11C 17/00</a>
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## H10B 20/20

### Programmable ROM [PROM] devices comprising field-effect components ([H10B 20/10](#) takes precedence)

#### Definition statement

*This place covers:*

Non-volatile ROM devices comprising multiple memory cells that can be programmed after their manufacture ("programmable ROM" or "PROM"), wherein the memory cell comprises field-effect components as either the access component or the storage component.

The group [H10B 20/20](#) itself covers PROM wherein individual memory cells may each be programmed more than once, e.g. a "corrective programming" may occur because the cells have more than one element that may be irreversibly-changeable element. The groups indented under [H10B 20/20](#) cover PROM wherein each cell may only be programmed once.

Illustrative example for this group: a cell is constructed from an anti-fuse programming transistor M0, an electronic fuse EF, and a control transistor MN1, such that the normal programming of M0 by

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breaking down its gate-source insulation layer (which decreases its initial large resistance) can be followed by "correction programming" by fusing the effuse (increasing the resistance).

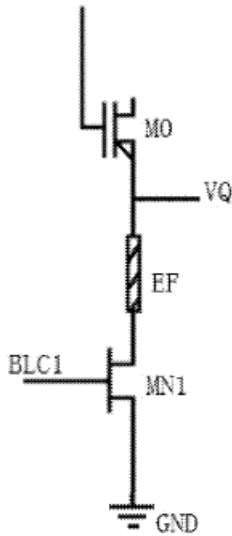


FIG. 2

**References**

**Limiting references**

*This place does not cover:*

ROM devices comprising bipolar components	<a href="#">H10B 20/10</a>
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**Informative references**

*Attention is drawn to the following places, which may be of interest for search:*

Circuits (e.g. data buffers, decoders, amplifiers) and accessing (e.g. read, write and erase operations) of ROM devices	<a href="#">G11C 17/00</a>
Anti-fuses, i.e. connections having their state changed from non-conductive to conductive	<a href="#">H01L 23/5252</a>
Fuses, i.e. connections having their state changed from conductive to non-conductive	<a href="#">H01L 23/5256</a>

**H10B 20/25**

**One-time programmable ROM [OTPROM] devices, e.g. using electrically-fusible links**

**Definition statement**

*This place covers:*

Non-volatile programmable ROM (PROM) devices comprising multiple memory cells wherein, after their manufacture, each cell can only be programmed once (e.g. by permanently connecting or disconnecting a fuse or an anti-fuse).

## References

### Informative references

Attention is drawn to the following places, which may be of interest for search:

Circuits (e.g. data buffers, decoders, amplifiers) and accessing (e.g. read, write and erase operations) of one-time PROM devices	<a href="#">G11C 17/14</a>
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## H10B 41/00

### Electrically erasable-and-programmable ROM [EEPROM] devices comprising floating gates

#### Definition statement

*This place covers:*

Non-volatile memory devices having multiple memory cells, wherein in each cell, the logic state is stored as charge on a floating gate of a transistor. The memory cell can be electrically erased and reprogrammed.

## References

### Informative references

Attention is drawn to the following places, which may be of interest for search:

EEPROM devices comprising charge-trapping gate insulators	<a href="#">H10B 43/00</a>
Ferroelectric memory devices comprising ferroelectric memory transistors	<a href="#">H10B 51/00</a>
Circuits (e.g. data buffers, decoders, amplifiers) and accessing (e.g. read, write and erase operations) of EEPROM devices	<a href="#">G11C 16/04</a>
Gate electrodes comprising a conductor-insulator-conductor-insulator-semiconductor structure	<a href="#">H01L 29/40114</a>
Floating-gate transistors per se	<a href="#">H01L 29/788</a>

## H10B 43/00

### EEPROM devices comprising charge-trapping gate insulators

#### Definition statement

*This place covers:*

Non-volatile memory devices having multiple memory cells, wherein in each cell, the logic state is stored as charge on a charge-trapping gate dielectric. The memory cell can be electrically erased and reprogrammed.

## References

### Informative references

Attention is drawn to the following places, which may be of interest for search:

EEPROM devices comprising floating gates	<a href="#">H10B 41/00</a>
Ferroelectric memory devices comprising ferroelectric memory transistors	<a href="#">H10B 51/00</a>
Circuits (e.g. data buffers, decoders, amplifiers) and accessing (e.g. read, write and erase operations) of EEPROM devices	<a href="#">G11C 16/04</a>

Gate electrodes comprising a charge-trapping insulator	<a href="#">H01L 29/40117</a>
Memory transistors in which the charge is stored in an insulating charge-trapping layer per se	<a href="#">H01L 29/792</a>

## H10B 51/00

### Ferroelectric RAM [FeRAM] devices comprising ferroelectric memory transistors

#### Definition statement

*This place covers:*

Non-volatile memory devices having multiple memory cells, wherein in each cell, the logic state is stored as a polarisation state of a ferroelectric material within a transistor, e.g. in a ferroelectric gate dielectric. The memory cell can be electrically erased and reprogrammed.

#### References

##### Informative references

*Attention is drawn to the following places, which may be of interest for search:*

EEPROM devices comprising floating gates	<a href="#">H10B 41/00</a>
EEPROM devices comprising charge-trapping gate insulators	<a href="#">H10B 43/00</a>
Ferroelectric memory devices comprising ferroelectric memory capacitors	<a href="#">H10B 53/00</a>
Circuits (e.g. data buffers, decoders, amplifiers) and accessing (e.g. read, write and erase operations) of FeRAM devices with ferroelectric transistors	<a href="#">G11C 11/223</a>
Gate electrodes therefor	<a href="#">H01L 29/40111</a>
Memory transistors with a ferroelectric layer in the gate stack	<a href="#">H01L 29/78391</a>

## H10B 53/00

### Ferroelectric RAM [FeRAM] devices comprising ferroelectric memory capacitors

#### Definition statement

*This place covers:*

Non-volatile memory devices having multiple memory cells, wherein in each cell, the logic state is stored as a polarisation state of a ferroelectric material within a capacitor, e.g. in a ferroelectric capacitor dielectric. The cell is accessed by a selection component and can be electrically erased and reprogrammed.

#### References

##### Informative references

*Attention is drawn to the following places, which may be of interest for search:*

DRAM	<a href="#">H10B 12/00</a>
Ferroelectric memory devices comprising ferroelectric memory transistors	<a href="#">H10B 51/00</a>

Circuits (e.g. data buffers, decoders, amplifiers) and accessing (e.g. read, write and erase operations) of FeRAM devices with ferroelectric capacitors	<a href="#">G11C 11/221</a>
Ferroelectric capacitors comprising a perovskite structure material	<a href="#">H01L 28/55</a>

## H10B 61/00

### Magnetic memory devices, e.g. magnetoresistive RAM [MRAM] devices

#### Definition statement

*This place covers:*

Non-volatile memory devices having multiple memory cells, wherein in each cell, the logic state is stored in magnetic domains of magnetic layers in a storage component. The memory cell can be electrically erased and reprogrammed. Examples include MTJ-based memory and STT-MRAM.

#### Relationships with other classification places

Aspects of the individual galvanomagnetic devices (e.g. structure, materials or manufacturing) are covered by group [H10N 50/00](#).

#### References

##### Informative references

*Attention is drawn to the following places, which may be of interest for search:*

Circuits (e.g. data buffers, decoders, or amplifiers) and accessing (e.g. read, write and erase operations) of MRAM	<a href="#">G11C 11/14</a> , <a href="#">G11C 11/16</a> , <a href="#">G11C 11/18</a>
Thin magnetic films	<a href="#">H01F 10/00</a>
Galvanomagnetic devices (e.g. MTJs, spin valves)	<a href="#">H10N 50/00</a>
Hall effect devices	<a href="#">H10N 52/00</a>

#### Synonyms and Keywords

*In patent documents, the following abbreviations are often used:*

GMR	Giant magnetoresistance
MR	Magnetoresistance
MTJ	Magnetic tunnel junction, MR tunnel junction
TMR	Tunnel magnetoresistance
MRAM	Magnetoresistive RAM
STT	Spin-transfer torque



## H10B 63/00

### Resistance change memory devices, e.g. resistive RAM [ReRAM] devices

#### Definition statement

*This place covers:*

Non-volatile memory devices having multiple memory cells, wherein in each cell, the logic state is stored as a high or low resistance state. The memory cell can be electrically erased and reprogrammed. Examples include:

- conductive bridge memory [CBRAM],
- bulk electronic defect-based memory,
- phase change memory [PCRAM], and
- Ovonic threshold devices.

#### Relationships with other classification places

Aspects of the individual resistance switching devices (e.g. structure, materials or manufacturing) are covered by group [H10N 70/00](#).

#### References

##### Informative references

*Attention is drawn to the following places, which may be of interest for search:*

Programmable ROM, e.g. involving fuses or anti-fuses	<a href="#">H10B 20/20</a>
Circuits (e.g. data buffers, decoders, amplifiers) and accessing (e.g. read, write and erase operations) of variable-resistance memory devices	<a href="#">G11C 13/00</a> , <a href="#">G11C 11/56</a>
Circuits and accessing of programmable memory involving anti-fuses	<a href="#">G11C 17/16</a>
Resistance change memory cells (e.g. memristors or phase change devices)	<a href="#">H10N 70/20</a>

## H10B 69/00

### Erasable-and-programmable ROM [EPROM] devices not provided for in groups [H10B 41/00](#) - [H10B 63/00](#), e.g. ultraviolet erasable-and-programmable ROM [UVEPROM] devices

#### Definition statement

*This place covers:*

Non-volatile memory devices having multiple memory cells, wherein in each cell, the logic state is erasable and reprogrammable, other than those covered by [H10B 41/00](#)- [H10B 63/00](#). Examples include:

- EPROM devices such as those that are erased by UV exposure ("UV-EPROM")
- Types of EEPROM devices that are not covered by groups [H10B 41/00](#)- [H10B 63/00](#), such as those that are globally erased by applying a high voltage.

#### References

##### Informative references

*Attention is drawn to the following places, which may be of interest for search:*

Circuits and accessing of EEPROMs	<a href="#">G11C 16/00</a>
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## H10B 80/00

### Assemblies of multiple devices comprising at least one memory device covered by this subclass

#### Relationships with other classification places

Class [H10](#) contains many groups for assemblies. If an assembly has multiple element devices therein, multiple classification should be used to classify the assembly in each appropriate group.

For example, if an assembly of multiple devices has the elements of, e.g. a memory chip, an integrated processor chip and a superconducting integrated chip, multiple classification should be made in [H10B 80/00](#) for the memory chip, in [H01L 25/00](#) for the integrated processor chip and in [H10N 69/00](#) for the superconducting chip.

Furthermore, classification of generic aspects of the assembly (e.g. the chips are stacked, or have interposers therebetween) should be made in [H01L 25/00](#) and [H01L 2225/00](#).

#### References

##### *Informative references*

*Attention is drawn to the following places, which may be of interest for search:*

Assemblies consisting of multiple individual semiconductor or other solid state devices	<a href="#">H01L 25/00</a>
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