# H03M

## CODING; DECODING; CODE CONVERSION IN GENERAL (using fluidic means F15C 4/00; optical analogue/digital converters G02F 7/00; coding, decoding or code conversion, specially adapted for particular applications, see the relevant subclasses, e.g. G01D, G01R, G06F, G06T, G09G, G10L, G11B, G11C, H04B, H04L, H04M, H04N; ciphering or deciphering for cryptography or other purposes involving the need for secrecy G09C)

## Definition statement

*This place covers:*

The scope of the subclass H03M is so broad that a detailed description of the subject matter appropriate for this place is correctly possible only at the main-group level, e.g. H03M 7/00.

Provisions that are valid at a general level (e.g. of a kind appropriate to more than one of the main groups) are provided in the sections that follow.

The user is otherwise referred to the IPC definitions for the individual main groups of H03M which follow hereinafter. The following list is intended to assist the user.

Coding and decoding

| | |
|---|---|
| In general | H03M 1/00 |
| To or from differential modulation | H03M 3/00 |
| In connection with keyboards | H03M 11/00 |

Conversion

| | |
|---|---|
| Of the form of individual digits | H03M 5/00 |
| Of the sequence of digits | H03M 7/00 |
| Parallel/series or vice versa | H03M 9/00 |

Others

| | |
|---|---|
| Error detection or error correction | H03M 13/00 |
| Subject matter not provided for in other groups of this subclass | H03M 99/00 |

## Relationships with other classification places

See the application places listed below the subclass title.

## References

### *Limiting references*

*This place does not cover:*

| | |
|---|---|
| Using fluidic means | F15C 4/00 |
| Coding, decoding or code conversion, specially adapted for particular applications, see the relevant subclasses | G01D, G01R, G06F, G06T, G09G, G10L, G11B, G11C, H04B, H04L, H04M, H04N |

| | |
|---|---|
| Optical analogue/digital converters | G02F 7/00 |
| Ciphering or deciphering for cryptography or other purposes involving the need for secrecy | G09C |

# H03M 1/00

## Analogue/digital conversion; Digital/analogue conversion (conversion of analogue values to or from differential modulation H03M 3/00)

### Definition statement

*This place covers:*

- A/D or D/A converters as such.
- A/D or D/A conversion systems, e.g. systems comprising one or more A/D or D/A converters working together or systems comprising A/D or D/A converters in combination with other components such as gain stages, filters or which contribute to the overall A/D or D/A conversion.
- Position or velocity encoders insofar as their coding aspects are relevant.

Note: For the purpose of conciseness, within this FCR the acronyms A/D and D/A will be used for analogue/digital and digital/analogue respectively.

Further information:

H03M 2201/00

Documents published prior to 1990 have been classified using deep-indexing scheme H03M 2201/00, which was derived from an older, non-IPC-based deep-indexing scheme (ICIREPAT scheme RM03) and for these documents replaces the use of subgroups H03M 1/001 through H03M 1/88. All these documents have main group symbol H03M 1/00 as the mandatory but - for search purposes - dummy EC classification symbol.

Since indexing scheme H03M 2201/00 has been closed, it should not be used for classifying new documents.

For the search in these documents, it is noted that, as this scheme is obtained by conversion from said deep indexing system RM03 it reflects the three disjunct editions of that system in the following way:

code symbols added or amended in subsequent editions are indicated by numbers [2] or [3] in square brackets, the code symbols present from the first edition on having no indication;

headers which did not have a code symbol in the RM03 system and thus could not be assigned to documents, but which need a code symbol in the Indexing Code system for the purpose of a correct hierarchical order, are indicated by the symbol [H];

the edition according to which a particular document has been indexed is indicated by the assignment of one of code symbols H03M 2201/01 through H03M 2201/03 to that document.

In principle, therefore, a search should include a separate combination of appropriate code symbols for each edition, each combination including one of codes H03M 2201/01 through H03M 2201/03. On an incidental base, however, code symbols from later editions have been allocated to documents indexed according to an earlier edition.

H03M 1/001

This group deals with circuits for converting an analogue signal into a digital one and directly back to analogue.

H03M 1/002

This group deals with the provision of special means for saving power, e.g. for allowing a sleep mode. Thus the group should not be used for overall designs using less power than prior ones.

H03M 1/02

This group covers converters which are truly reconfigurable between A/D and D/A conversion as well as CODEC's having separate A/D and D/A converters with at least partially common control.

H03M 1/04

This group covers converters in which the conversion process as such has a stochastical nature or which convert the analogue or digital signal to a (possibly intermediate) signal in which the information content is represented by stochastic parameters. (Signals of the latter type are for example used for calculations of the type classified in G06F 7/70.) It does not cover the use of dither or the random selection among identical elements for averaging out errors.

H03M 1/1235

This group is residual to A/D converters having an intentionally non-linear transfer characteristic and not falling within the scope of anyone of groups H03M 1/367, H03M 1/464, H03M 1/58 or H03M 1/62.

H03M 1/36

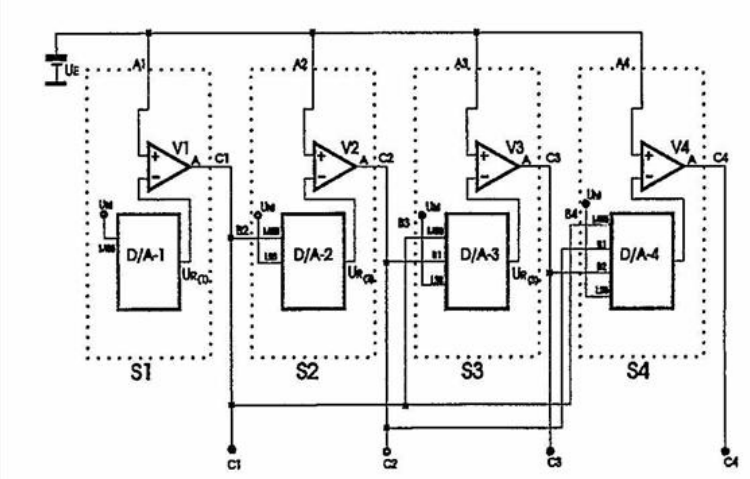
It is noted that some patent documents deal with converters stated by the inventor to be "parallel converters using n comparators for n bits" or similar but in which in fact the reference values of the second and further comparators are modified according to the outputs of one or more preceding comparators. Thus in reality these converters are not parallel but asynchronous serial converters falling within the scope of H03M 1/42.

H03M 1/42

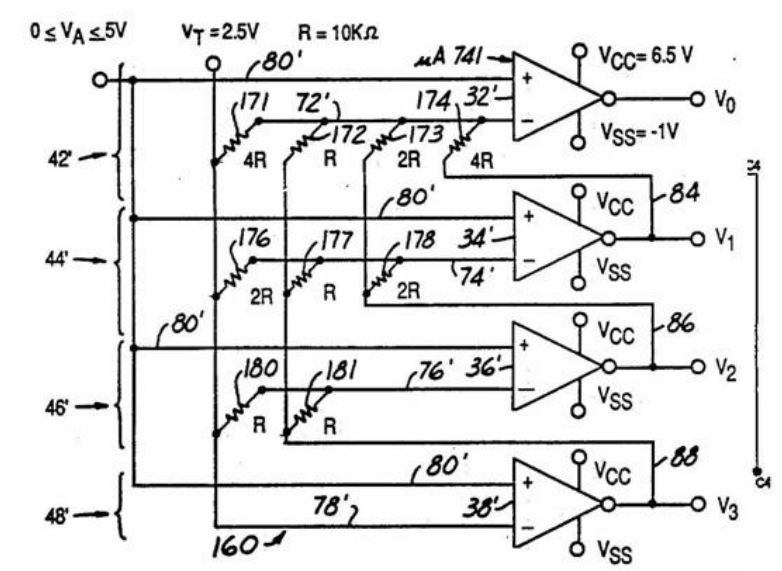
Multiple stage A/D converters in which the input signal is broadcasted to all stages while the reference value applied to each stage but the first one is modified by the output of one or more preceding stages.

Examples:

DE4402952 to Sander



US4965579 to Liu et al (erroneously called a parallel converter)



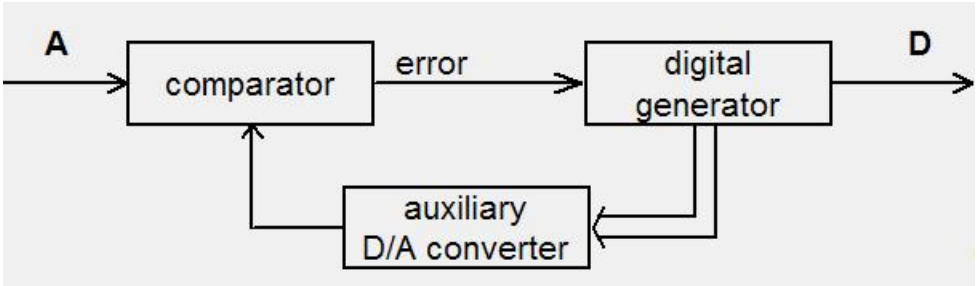

[H03M 1/44](#)

Multiple stage A/D converters in which the input signal is broadcasted to all stages while the reference value applied to each stage but the first one is modified by the output of one or more preceding stages.

[H03M 1/48](#)

A/D converters in which the output signal continuously tracks the input signal by means of reconversion of the output signal to an analogue feedback signal which is compared to the input signal.

Block diagram:



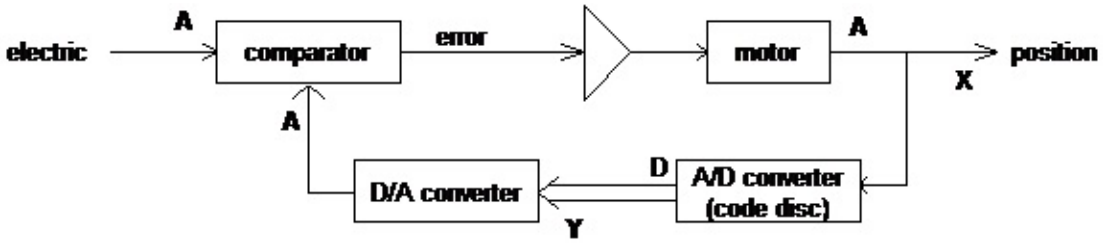

Source: "ICIREPAT SYSTEM 03 (+ Addendum), A-D CONVERTERS", Manual with Definitions and Term List, 3d edition, Institut International des Brevets, October 1976.

The error signal usually adjusts the digital generator in one or the other direction, in dependence upon the sign of the error, in order to reach the correct position along the shortest route. However, occasionally the digital generator can be adjusted in one direction only; then it has to move circularly through nearly a full cycle in order to obtain a change in the other direction. It is difficult sometimes to distinguish the latter systems from the range sweeping type ([H03M 1/56](#)) in which, however, the digital generator returns to a datum position between successive conversions. US3026033 to Spooner gives an example of both and clearly shows the difference. The "successive approximation" type converters ([H03M 1/46](#)) are sometimes called "feedback converters" as well but are also reset between conversions.

Also, it is sometimes difficult to distinguish servo-type converters from A/D converters using differential modulation (H03M 3/00) which, however, deliver an output signal having a reduced number of bits at an oversampling rate, thus needing a decimation filter for converting it to a final result at full resolution and Nyquist rate.

General analogue servo-systems using only digital feedback, for example as shown in the following block diagram, do, strictly spoken, not fall within the definition of an A/D conversion system.

However, they are very similar to an A/D conversion system using a D/A converter in a feedback arrangement (output Y instead of X) and therefore these systems are classified in H03M 1/48 unless the converters are merely shown as black boxes.



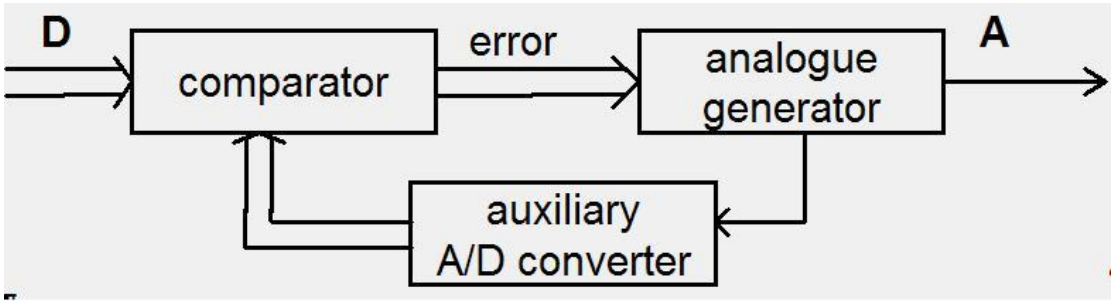

H03M 1/664

This group is residual to D/A converters having an intentionally non-linear transfer characteristic and not falling within the scope of anyone of groups H03M 1/84 or H03M 1/88.

H03M 1/668

D/A converters in which the output signal continuously tracks the input signal by means of reconversion of the output signal to an digital feedback signal which is compared to the input signal.

Block diagram:




The error signal usually adjusts the analogue generator in one or the other direction, in dependence upon the sign of the error, in order to reach the correct position along the shortest route. However, occasionally the analogue generator can be adjusted in one direction only; then it has to move circularly through nearly a full cycle in order to obtain a change in the other direction. It is difficult sometimes to distinguish the latter systems from the range sweeping type (H03M 1/82) in which, however, the analogue generator returns to a datum position between successive conversions.

H03M 1/78

Networks comprising impedances in series as well as parallel branches.

| | |
|---|---|
| Networks having impedances in series branches only | H03M 1/76 |
| Networks having impedances in parallel branches only | H03M 1/80 |

Classification of successive approximation type A/D converters.

For the classification of the different types of successive approximation type A/D converters the following table can be helpful:

| no. of stages | no. of evaluated bits per step or stage | input/residue modified | reference modified |
|---|---|---|---|
| single stage, multiple iteration steps: | single bit per step: | H03M1/40 | H03M1/46 |
| | multiple bits per step: | H03M1/16R | H03M1/14R |
| multiple stages, single iteration step per stage: | single bit per stage: | H03M1/44 | H03M1/42 |
| | multiple bits per stage: | H03M1/16S | H03M1/14S |

## Relationships with other classification places

The structural association with components such as transducers, sensors, gain stages or filters can be classified either in H03M 1/00 or in the subclass covering the component (or in both the subclasses), depending on which aspect is more relevant.

In particular A/D or D/A converters represented as “black boxes” in a specific application (e.g. a measuring or telecommunication system) are in general not classified in H03M.

Relations between H03M 1/00 and H03M 3/00

A/D and D/A converters using differential modulation are classified in H03M 3/00. According to the reference out following main group symbol H03M 1/00, for all A/D and D/A converters using differential modulation, e.g. delta modulation, DPCM and nowadays in particular delta-sigma modulation, main group H03M 3/00 has precedence over H03M 1/00. Note however, that inventions actually relating to "normal" converters which are used as components within such differential modulators are classified in H03M 1/00 again (because they can be more widely applied than only in the "differential" context). An example of the latter is dynamic element matching in D/A converters used in feedback paths of multi-bit delta-sigma A/D converters or in feedforward paths of multi-bit delta-sigma D/A converters, which is classified in group branch H03M 1/066.

Position or velocity encoders

In principle the classification in H03M 1/00 is directed to the coding aspects, whereas that in G01D or G01P is directed to the transducer aspects, but in practice they also appear to have subgroups directed to coding aspects.

Electro-optical A/D or D/A converters

In many cases inventors state to have invented an optical A/D or D/A converter though in fact only the sampling or signal conditioning is optical but the conversion itself is electronic. In principle both these cases and true electro-optical converters are classified in H03M while true optical converters are classified in G02F 7/00, but in practice many electro-optical converters appear to have been classified in G02F 7/00 as well.

## References

### *Limiting references*

*This place does not cover:*

| | |
|---|---|
| A/D or D/A conversion using differential modulation | H03M 3/00 |
| Digital delta-sigma modulators per se | H03M 7/3002 |
| A/D or D/A converters using fluidic means (e.g. pneumatic, hydraulic) | F15C 4/00 |
| All-optical A/D or D/A converters | G02F 7/00 |

| | |
|---|---|
| Time-to-digital converters | G04F 10/005 |
| Current or voltage sources | G05F 3/00 |
| Digital pulse width modulators per se, i.e. resulting in a discrete PWM signal | G06F 1/025, H03M 5/08 |
| Interfacing or handshaking between A/D or D/A converters on the one hand and computers on the other hand | G06F 3/05 |
| Comparators : for comparing digital (multi-bit) signals for comparing logic signalsfor comparing analogue signals | G06F 7/02, H03K 3/00, H03K 5/24 |
| A/D or D/A converters performing calculations (i.e. on two or more input signals) | G06J 1/00 |
| Transmission of measurement or control data | G08C |
| S/H circuits in general | G11C 27/02 |
| Chip layout of an array of impedances, current sources, switches etc. | H01L 27/00, H01L 29/00 |
| Resolvers or synchros per se | **H02M24/00** |
| Operational amplifiers | H03F |
| Sample rate conversion | H03H 17/0416, H03H 17/0621 |
| Analogue pulse width modulators per se | H03K 7/08 |
| Current switches | H03K 17/00 |
| Multiplexers per se | H03K 17/00 |
| Multiplex transmission systems | H04J |
| Pulse-shaping in general | H04L 25/03 |
| DC level restoring in generalin television receivers | H04L 25/06, H04N 5/18 |

### *Informative references*

*Attention is drawn to the following places, which may be of interest for search:*

| | |
|---|---|
| Documents in this main group published before 1990 (see "Further information" in the Definition Statement above) | H03M 2201/00 |
| Position encoders | G01D 5/00 |
| Speed encoders | G01P 3/00 |
| Measuring electric variables using an A/D converter | G01R 19/25 |
| Testing combined analogue and digital circuits in general | G01R 31/3167 |
| Electro-optical A/D or D/A converters | G02F 7/00 |
| Display devices, e.g. LCD displays, using D/A converters | G09G 3/00 |
| Recording or reproducing data using A/D or D/A converters | G11B 20/10 |
| Multi-position switches | **H01H21/62** |
| Transmission systems using pulse modulation | H04B 14/02 |
| Imagers using A/D converters | H04N 5/335 |

## Special rules of classification

Classification of additional information:

- The invention as such as well as additional information shall be classified.
- The use of the Indexing Codes for classification is compulsory (except for main group H03M 2201/00, as explained in the "Further information" in the Definition Statement above) and shall be used in addition to the appropriate ECLA code.
- In particular Indexing Code scheme H03M 1/00-H03M 1/88 is used for indicating the type(s) of the (sub)convert(s) to which the invention is applied, when the invention information is to be classified in one of the ranges H03M 1/001-H03M 1/1095, H03M 1/1205-H03M 1/208 or H03M 1/661-H03M 1/687. These types can be indicated using one or more symbols from group branches H03M 1/12 or H03M 1/66.
- In cases where a conversion system includes both standard and differential (sub)converters, also the appropriate type of the differential (sub)converter(s) should be indicated using symbols from the Indexing Code main group H03M 3/00 or group branch H03M 7/3002 .
- For the search in main group H03M 1/00 it is noted that additional information has been classified in this group from 01--01--1990 onwards.

## Glossary of terms

*In this place, the following terms or expressions are used with the meaning indicated:*

| | |
|---|---|
| Pattern shifting code | Serial multiple bit code in which the first n--1 bits of each combination are identical to the last n-- 1 bits of the preceding<br>E.g. 000<br>001<br>010<br>101<br>011<br>111<br>110<br>100<br>combination. |
| Quantisation value generator | Component generating an analogue value corresponding to an elementary digital value, i.e. to a single bit or digit |
| Reconfigurable | The converter can be set to operate in different ways by setting switches to a particular position |

## Synonyms and Keywords

*In patent documents the following abbreviations are often used:*

English:

| | |
|---|---|
| ADC | A/D converter |
| CODEC | coder and decoder |
| DAC | D/A converter |
| DEM | dynamic element matching |
| DWA | data weighted averaging |
| PWM | pulse width modulation |
| S/H circuit | sample/hold circuit |
| SAR | successive approximation register |
| SA-ADC | successive approximation type A/D converter |

French:

| | |
|---|---|
| CAD, CAN | A/D converter |
| CDA, CNA | D/A converter |

German:

| | |
|---|---|
| ADU, ADW | A/D converter |
| DAU, DAW | D/A converter |

*In patent documents the following expressions are often used as synonyms:*

English:

| | |
|---|---|
| Chain code | pattern shifting code |
| Encoder, digitiser, quantiser, binariser, voltage-to-digital converter | A/D converter |
| Flash converter | simultaneous A/D converter |
| Pipeline converter | synchronous multiple stage SA-ADC each stage of which operates on a different sample |
| Half -flash convertersemi-flash converter | multiple bits per stage type SA-ADC converting the input value either in two steps in a single flash converter or sequentially in two series-connected flash converters |
| Two -pass convertertwo-step converter | multiple bits per stage recirculation type SA-ADC converting the input value in two steps in a single flash converter |
| Dual rank converter extended-flash converter serial-parallel convertertwo-stage converter | multiple bits per stage type SA-ADC converting the input value sequentially in two series-connected flash converters |
| Algorithmic converter | recirculation type SA-ADC |
| Tracking converter | servo-type converter |

French:

| | |
|---|---|
| Convertisseur A/N, codeur, numériseur, quantificateur | A/D converter |
| Convertisseur N/A | D/A converter |
| Convertisseur instantané | parallel A/D converter |

German:

| | |
|---|---|
| A/D-Wandler, A/D-Übersetzer | A/D converter |
| D/A-Wandler, D/A-Übersetzer | D/A converter |

# H03M 3/00

## Conversion of analogue values to or from differential modulation

### Definition statement

*This place covers:*

- Analogue differential modulators, e.g. delta modulators, differential pulse code modulators, delta-sigma modulators;
- A/D and D/A converters or conversion systems using differential modulation.

### Relationships with other classification places

The structural association with components such as transducers, sensors, gain stages or filters can be classified either in H03M 3/00 or in the subclass covering the component (or in both the subclasses), depending on which aspect is more relevant.

In particular differential modulators represented as “black boxes” in a specific application (e.g. a measuring or telecommunication system) are in general not classified in H03M.

### References

#### *Limiting references*

*This place does not cover:*

| | |
|---|---|
| Digital delta-sigma modulators | H03M 7/3002 |

#### *Informative references*

*Attention is drawn to the following places, which may be of interest for search:*

| | |
|---|---|
| Recording or reproducing data using A/D or D/A converters | G11B 20/10 |
| Transmission systems using differential modulation | H04B 14/06 |

### Special rules of classification

Classification of additional information:

- The invention as such as well as additional information shall be classified.
- The use of the Indexing Codes for classification is compulsory and shall be used in addition to the appropriate ECLA code.
- For the search in main group H03M 3/00 it is noted that additional information has been classified in this group from 01--11--2004 onwards.

### Synonyms and Keywords

*In patent documents the following abbreviations are often used:*

| | |
|---|---|
| ADM | Adaptive Delta Modulator |
| ADPCM | Adaptive Differential Pulse Code Modulator |
| ADSM | Adaptive Delta-Sigma Modulator |
| DM | Delta Modulator |
| DPCM | Differential Pulse Code Modulator |
| DPWM | Differential Pulse Width Modulator |
| DSM | Delta-Sigma Modulator |

| | |
|---|---|
| MASH | Multiple Stage Noise Shaping Delta-Sigma Modulator |
| SDM | Sigma-Delta Modulator |

*In patent documents the following expressions are often used as synonyms:*

| | |
|---|---|
| Bitstream converter | A/D converter using single bit delta-sigma modulation |
| Noise-shaper | delta-sigma modulator |
| Sigma-delta modulator | delta-sigma modulator |

# H03M 5/00

## Conversion of the form of the representation of individual digits

### Definition statement

*This place covers:*

Conversion of codes where one aspect is the representation of the code as a signal, e.g. a code embodied by pulses or other shapes (e.g. sinusoidal). Examples are modulation codes (like Manchester coding).

Further information:

H03M 5/14

This groups covers run-length coding, i.e. codes with run-length constraints.

### References

#### *Limiting references*

*This place does not cover:*

| | |
|---|---|
| A/D or D/A conversion | H03M 1/00 |
| Differential modulation | H03M 3/00, H03M 7/3002 |

### Special rules of classification

In groups H03M 5/02 - H03M 5/22, in the absence of an indication to the contrary, an invention is classified in the last appropriate place.

Classification of additional information:

- The invention as such as well as additional information shall be classified.
- The use of the Indexing Codes for classification is compulsory and shall be used in addition to the appropriate ECLA code.
- For the search in main group H03M 5/00 it is noted that additional information has been classified in this group from 01--04--2004 onwards.

# H03M 7/00

## Conversion of a code where information is represented by a given sequence or number of digits to a code where the same information {or similar information or a subset of information} is represented by a different sequence or number of digits

### Definition statement

*This place covers:*

A sequence of numerical or textual symbols representing a code and transformations/conversions thereof into a different sequence of numbers or textual symbols. It comprises in particular code conversions resulting in shorter codes (data compression and decompression).

The sequence of textual symbols could be part of a structured text document, for example an XML document.

Also covered are devices which provide for such code conversion, e.g. hardware implemented code converters and code converters based on logic circuit and programmable converters.

Furthermore, data reduction methods in order to get a short representation of a signal or of digital data in general are also covered. An example would be methods for reducing the number of necessary samples in data acquisition.

Further information:

H03M 7/26

This subgroup deals solely with data compression and is not to be used for run-length-limited modulation techniques.

H03M 7/30

This group branch in general deals with all types of data compression unless the data compression is specified merely as a "black box". It also deals with precoding before the actual compression stage in order to get better compression results (e.g. Burrows-Wheeler transform).

H03M 7/3002

This group branch deals with digital differential modulation, e.g. delta modulation [DM], differential pulse code modulation [DPCM], delta-sigma modulation [DSM], and replaces IPC subgroups **H03M7/32** - **H03M7/38**.

### Relationships with other classification places

Relations between H03M 7/46 and H03M 5/145:

- H03M 7/46 deals with data compression by replacing a sequence of same digits/characters with the value of the digit/character and a specification of its number (run-length code/compression).
- H03M 5/145 deals with run-length-limited codes, i.e. modulation schemes which contain a maximum number of same digits.

Relations between H03M 7/30 and H04N 19/00:

Use of data compression bandwidth reduction for in video coding (H04N 19/00) when the data compression is merely represented as a "black box" are not in the scope of H03M 7/30. However, if a certain data compression scheme for video bandwidth reduction is detailed and goes beyond conventional compression algorithms, this new aspect can be classified in H03M 7/30. An example is the use of arithmetic coding in video coding (e.g. CABAC) where specific aspects should be classified under H03M 7/30.

In general, data compression schemes merely represented as "black boxes" in a certain application field should not be classified under H03M 7/00.

## References

### *Limiting references*

*This place does not cover:*

| | |
|---|---|
| Audio coding | G10L 19/00 |
| Video coding | H04N 19/00 |

### *Informative references*

*Attention is drawn to the following places, which may be of interest for search:*

| | |
|---|---|
| Use of compressive sensing | G01L 1/00, G01L 5/00 |
| Processing of structured documents, e.g. xml, also for the purpose of size reduction | G06F 17/22 |
| Source coding for video and arithmetic data compression for video coding | H04N 19/00 |

## Special rules of classification

- In groups H03M 7/02 - H03M 7/50, in the absence of an indication to the contrary, an invention is classified in the last appropriate place.
- IPC subgroups **H03M7/32** - **H03M7/38** are not used. Their subject-matter is covered by H03M 7/3002 .

Classification of additional information:

- The invention as such as well as additional information shall be classified.
- The use of the Indexing Codes for classification is compulsory and shall be used in addition to the appropriate ECLA code.
- For the search in main group H03M 7/00 it is noted that in general additional information has been classified in this group from 01--04--2004 onwards. However, in group branch H03M 7/3002 it has been classified for all documents.

## Synonyms and Keywords

*In patent documents the following abbreviations are often used:*

| | |
|---|---|
| ADM | Adaptive Delta Modulator |
| ADPCM | Adaptive Differential Pulse Code Modulator |
| ADSM | Adaptive Delta-Sigma Modulator |
| CABAC | Context-Adaptive Binary Arithmetic Coding |
| CAVLC | Context-Adaptive Variable Length Coding |
| DM | Delta Modulator |
| DPCM | Differential Pulse Code Modulator |
| DPWM | Differential Pulse Width Modulator |
| DSM | Delta-Sigma Modulator |
| LZ | Lempel-Ziv |
| MASH | Multiple Stage Noise Shaping Delta-Sgma Modulator |
| SDM | Sigma-Delta Modulator |

| | |
|---|---|
| VLC | Variable-Length Coding |

*In patent documents the following expressions are often used as synonyms:*

| | |
|---|---|
| Error quantiser | error feedback type delta-sigma modulator |
| Noise-shaper | delta-sigma modulator |
| Sigma-delta modulator | delta-sigma modulator |

# H03M 9/00

## Parallel/series conversion or vice versa (digital stores in which the information is moved stepwise per se G11C 19/00)

### Definition statement

*This place covers:*

Parallel/series conversion or vice-versa, in general;

Timing and synchronisation aspects thereof.

### References

#### *Limiting references*

*This place does not cover:*

| | |
|---|---|
| Parallel/series conversion or vice-versa of bits, or groups of bits, which are specifically adapted for transmission in telecommunication or data communication apparatus | H04J 3/047 |

#### *Informative references*

*Attention is drawn to the following places, which may be of interest for search:*

| | |
|---|---|
| Generation or distribution of clock signals, per se | G06F 1/04 |
| Regularising the speed of data flow, e.g. using first in first out registers for implementing a data queue, per se | G06F 5/06 |
| Frequency multipliers or dividers, per se | G06F 7/68 |
| Digital stores in which the information is moved stepwise, per se | G11C 19/00 |
| Synchronisation of pulse signals to a clock signal, per se | H03K 5/135 |
| Multiplexer switches, per se | H03K 17/002, H03K 17/62, H03K 17/693, H03K 17/76 |
| Frequency dividers using counters, per se | H03K 21/00 - H03K 29/00 |
| Phase locked loops or delay locked loops, per se | H03L 7/00 |
| Synchronisation of a data receiver with a transmitter, per se | H04L 7/00 |
| Line transmission arrangements where a single bit stream is divided between several channels and reassembled at the receiver, per se | H04L 25/14 |

## H03M 11/00

**Coding in connection with keyboards or like devices, i.e. coding of the position of operated keys (keyboard switch arrangements, structural association of coders and keyboards H01H 13/70, H03K 17/94)**

### References

#### *Limiting references*

*This place does not cover:*

| | |
|---|---|
| Mapping, i.e. converting a generated code set to a different one | G06F 3/023 |
| Virtual, i.e. software generated keyboards | G06F 3/023 |
| Constructional details of keys or keyboards | H01H 13/70 |
| Electrical details of keyboard switches | H03K 17/94 |

### Synonyms and Keywords

*In patent documents the following expressions are often used as synonyms:*

| | |
|---|---|
| Ghost key | Phantom key |

## H03M 13/00

**Coding, decoding or code conversion, for error detection or error correction; Coding theory basic assumptions; Coding bounds; Error probability evaluation methods; Channel models; Simulation or testing of codes (error detection or error correction for analogue/digital, digital/analogue or code conversion H03M 1/00 - H03M 11/00; specially adapted for digital computers G06F 11/08, for information storage based on relative movement between record carrier and transducer G11B, e.g. G11B 20/18, for static stores G11C; {use of error detection or error correction in transmission systems H04L 1/004, in television systems H04N 7/0357})**

### Definition statement

*This place covers:*

Encoding, decoding, coding or decoding schemes for the correction or detection of errors, i.e. error control coding (ECC) or forward error correction (FEC)

- Codes for the correction or detection of errors, e.g. block codes, convolutional codes or concatenated codes
- Construction or design (including modification of existing codes by e.g. puncturing or extension) of codes for the correction or detection of errors
- Algorithms, methods or devices for encoding or decoding of codes for the correction or detection of codes
- Unequal error protection codes or schemes, i.e. codes or coding schemes that provide several levels of error protection

Coded modulation for error detection or correction.

Combination of error correction coding and techniques for the efficient use of the spectrum, e.g. modulation codes with error correction properties

Synchronisation by means of error correction codes

Further information:

It follows a brief explanation of those ECLA subgroups, where it might not be clear from the wording alone what technical features are meant to fall within their scope:

H03M 13/005

- denotes punctured codes in general when no particular details about puncturing are provided
- subgroup H03M 13/6362 should be used for documents that disclose particular details regarding a strategy/scheme for rate matching by puncturing that extends beyond the mere use of punctured codes
- H03M 13/6368 H03M 13/6393 should be used when a particular type of puncturing is used, viz. rate compatible or complementary puncturing

H03M 13/033

- this subgroup covers methods for the construction of codes, wherein the generic term construction covers the design of generator and parity-check matrices, the design of generator polynomials, the design of mapping schemes, the design of puncturing schemes etc.
- if the design includes a computer search or a random component with subsequent optimisation, then the subgroup H03M 13/033 shall be allocated

H03M 13/091

- this subgroup covers the calculation of CRCs (either during encoding or decoding) when the calculation is performed in a parallel or partly parallel manner, e.g. by 8 or 32 bit parallel processing
- in contrast to partly parallel or parallel processing, there is serial processing in which a CRC is calculated 1 bit by 1 bit as it is done with a conventional linear feed-back shift register

H03M 13/093

- in some applications a CRC is calculated over an information word of n bits
- during transmission over a plurality of hops, the information word may be updated, e.g. some bits in the header are changed, which requires a recalculation of the CRC
- methods that do not fully recalculate the CRC but update the CRC only in respect to the changes of the information word (by exploitation of the linearity of the CRC code) are to be classified here
- examples can be found in e.g. XP000291536, WO2004013973

H03M 13/1114

- known in the literature as "Memory-Aware Decoder Architectures" and "Merged-Schedule Message-Passing (MSMP) algorithm"
- see XP011104612 page 980, Section C for a detailed description
- the memory efficiency is mainly due to eliminating the storage required to save every bit-to-check messages or check-to-bit messages as in the standard message passing decoding algorithm

H03M 13/1125

XP011027872 p. 512 or CA2310186 pages 17-18 disclose an overview on the several possible domains.

H03M 13/1131

- XP002370625 provides on pages 37-40 and 60-67 a good overview on the different schedules for belief propagation or message passing decoding
- scheduling is the order in which the messages of the graph should be propagated
- the "classical" scheduling is the so-called flooding schedule, where all nodes of one class, e.g. all messages send from bit nodes to check nodes, are updated before the nodes of the other class,

e.g. all messages send from variable nodes to check nodes, are updated; this can be done one node at a time (serially) or in parallel.

- full parallel flooding schedule processing should be classified under H03M 13/1134 (Remark: any full parallel schedule is implicitly a flooding schedule) and partly parallel flooding schedule processing under H03M 13/1137
- note that serial flooding schedules are not explicitly classified
- the "shuffled" scheduling mixes check node and variable node processing, e.g. check node processing of some check nodes is started before all variable nodes have been updated; this again can be performed serially, i.e. one node after the other, or partly-parallel, i.e. several nodes in parallel.
- serial "shuffled" scheduling should solely be classified under H03M 13/114.
- partly-parallel "shuffled" scheduling should be classified under H03M 13/1137 and H03M 13/114.

H03M 13/1168

- EP2051386 discloses in figure 15 such a matrix comprising the sum of permutation sub-matrices

H03M 13/1174

- XP011010719 discloses an example of a generalized LDPC code construction using a Hamming code

H03M 13/1188

- see WO2006039801, figure 6 for a typical example of such a parity check matrix

H03M 13/155

- only for shortened or extended codes that fit into H03M 13/151; these codes include in particular Reed-Solomon and BCH codes
- code shortening or extension for codes other than that, i.e. for codes that are not associated with error location and error correction polynomials, are to be classified under H03M 13/618; these codes include, for instance, Hamming codes or LDPC codes

H03M 13/1555

- decoder implementations that comprise a set of data processing elements connected in series, so that the output of one element is the input of the next one and so that the elements of a pipeline are often executed in parallel or in time-sliced fashion
- for instance, Reed-Solomon decoders are often implemented using a pipeline with 3 stages for syndrome calculation, calculation of the error locator polynomial and Chien search; cf. e.g. US2003140303

H03M 13/1565

- a cyclic block code with minimum hamming distance d can correct up to (d-1)/2 errors
- however, as long as the code is not perfect, i.e. does not meet the Hamming bound, there exist error patterns with weight greater than (d-1)/2 that can be corrected
- algorithms that provide decoding beyond (d-1)/2 errors are to be classified using H03M 13/1565
- for an example, cf. e.g. XP010670838

H03M 13/157

- evaluation of polynomial equations, e.g. syndrome evaluation using a blockwise parallelized Horner scheme as in WO9937029

H03M 13/1575

- direct decoding denotes decoding methods/decoders that do not require the calculation and evaluation of the error locator polynomial by means of complex algorithms like Berlekamp-Massey decoding or Chien search
- direct decoding is limited to small error weights or codes with small minimum Hamming distance

- by means of direct decoding the error locator polynomial or its roots or even the error values can be directly determined from the syndromes
- examples can be found in e.g. US6145112 and XP000859074

H03M 13/158

Methods and arrangements for finite field processing when applied in an encoder or decoder for error correcting codes, e.g. a finite field multiplier.

Examples can be found in e.g. US7178091, EP1217751 and US2004059989.

If the finite field processing is not disclosed in the context of error control coding, then this class is not to be given.

Methods and arrangements for finite field arithmetic are always to be circulated to G06F 7/72.

H03M 13/25

Coded modulation.

the subgroups H03M 13/251 - H03M 13/258 provide details as to the type of code that is used.

The type of code can be further refined by using the appropriate Indexing Code or ECLA subgroup; e.g. coded modulation with a Reed-Muller code would be classified using H03M 13/251 (coded modulation with block coding) and H03M 13/136 (Reed-Muller codes).

H03M 13/27

For a complete classification of a document concerning interleaving, it may be required to allocate more than one subgroup of H03M 13/27 to the document.

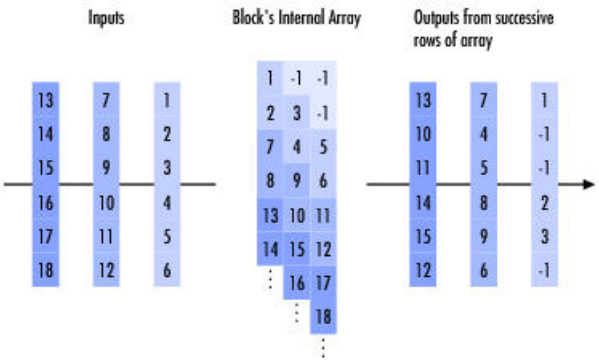
H03M 13/2703 H03M 13/2757 relate to different types of interleavers, whereas H03M 13/2771 - H03M 13/2796 relate to characteristics other than the type of interleaving.

Hence, a document relating to interleaving should usually have a designation of the type of interleaving (H03M 13/2703 - H03M 13/2757) and optionally one or more classes relating to the other characteristics (H03M 13/2771 - H03M 13/2796).

H03M 13/2771 indicates that the document deals with interleavers/interleaving for turbo codes (so-called turbo code internal interleavers).

H03M 13/2728

The principle underlying a helical type interleaver becomes clear from the following figure (with -1 denoting dummy bits):




Source: http://www.kxcad.net/cae_MATLAB/toolbox/commblks/ref/newblockinternalarray.gif

H03M 13/2753

The principle underlying an ARP interleaver is explained on page 1034 of XP031243772.

H03M 13/276

This subgroup covers the actual calculation of interleaving addresses

Note that the principle underlying a particular interleaving type may be described without actually providing details about how the address or index calculation is performed or implemented.

if a document does not only relate to a particular type of interleaver but provides in addition details about the calculation of interleaver addresses or indices, then this class should be given in addition.

H03M 13/2764

circuits/hardware implementations for the calculation of interleaver addresses or indices.

see also the comments w.r.t. H03M 13/276.

H03M 13/2767

cf. XP010656732 for an example.

H03M 13/2792

For an example, see EP1045522, EP1261161.

H03M 13/2796

are performed jointly). For an example, see EP1603247 (multiplexing and two stages of interleaving

H03M 13/2912

Product codes in which the sub-block comprising the checks-on-checks or parity-on-parity is not present (as it is either not generated or removed).

H03M 13/2921

For an example, cf. e.g. WO0169797 and EP0198702.

H03M 13/2927

Turbo decoding of concatenated block codes is to be classified in H03M 13/2963 .

If the decoding strategy involves iterative decoding different from turbo decoding, e.g. sub-sequent decoding of rows and columns of a product code, then this feature (iterative decoding) is to be classified using H03M 13/2948.

H03M 13/2939

Coding schemes including any concatenation of two or more convolutional codes, wherein decoding is not based on the turbo principle, e.g. serial concatenation of convolutional codes without turbo decoding.

H03M 13/2942

Typical examples can be found in e.g.

- US5838267; cf. Fig. 2; from an information word I, a first parity P1 is calculated; from P1 only, a second parity P2 is calculated.
- WO03085839, cf. Fig. 4; in a product code with horizontal and vertical parities, an additional level of parity is produced as follows: from an information block L1, two new blocks U1 and U2

are determined; U1 and U2 are XORed hence halving the block size; then, a parity block V2 is determined from the XORed block as additional level of redundancy

- US2005160350; cf. Fig. 1; the global row parity is obtained by XORing the row parity

H03M 13/2948

If the decoding strategy involves iterative decoding different from turbo decoding, e.g. decoding without exchange of extrinsic soft-decision information between decoders, then this feature (iterative decoding) is to be classified using H03M 13/2948.

H03M 13/2957

Note that H03M 13/2957 is also to be allocated when a component code is replaced by a non-coded constraint, e.g. turbo equalisation (cf. also the Glossary of terms and the comments on H03M 13/63).

H03M 13/296

Typical examples falling within the scope of this subgroup are e.g. zigzag codes (EP1926216, WO2007029114) or the hybrid concatenated codes of WO2007029114 or XP001034844.

H03M 13/333

Feedback from the channel decoder to a synchronisation unit is used to establish synchronisation with respect to a frame or block of bits, e.g. US2007245216.

H03M 13/336

Phase recovery in combination with channel decoding, wherein feedback from the channel decoder to phase estimation is used to achieve or improve the recovery/estimation of the symbol phase, cf. e.g. WO2006068367 or US2004240481.

H03M 13/3707

Decoding methods or techniques providing more than one decoding algorithm for one code and selection of the appropriate decoding method or technique

Adaptive decoding in which decoding is adapted to some extrinsic or intrinsic parameter, e.g. setting of internal thresholds.

Examples can be found in e.g. WO2007135657

H03M 13/3715

The extrinsic or intrinsic parameter is the number of estimated errors or information about the state of the channel (e.g. SNR).

Examples can be found in e.g. US6511280, DE19963683, EP1612949, US2002186798.

H03M 13/3723

Initialisation is meant to denote the configuration of the decoder (e.g. setting of internal variables) prior to decoding

Examples can be found in e.g. WO2006059280 (initialisation of MAP decoders for turbo decoding using the result of the previous iteration), US2004148561 (initialisation of variable nodes for LDPC code decoding), WO9740583 (initialisation of state probabilities for a tail-biting MAP decoder)

H03M 13/3776

Typical examples can be found in e.g. WO2009005332 (cf. Fig. 1), US2008155372 (cf. Fig. 5).

Note that re-encoding is often performed to estimate error rates but is not integral to decoding as such

H03M 13/3792

For examples and definitions of real number codes, see XP000217558, XP010192693, XP010240026.

H03M 13/3994

For trellis decoding, some bits may be known (e.g. during decoding of concatenated codes, padding bits) to the decoder, which exploits this information as a priori information.

The trellis decoder is forced to take the a priori known decision, for instance, by adding to the ACS circuit a decision-overriding logic or by saturating state or branch metrics.

This technique is sometimes referred to by state pinning or decision forcing or trellis pruning.

Examples can be found e.g. in XP418485, XP2174972.

H03M 13/451

For decoding, the optimum code word (in terms of a metric) is searched in a set of possible code words

The set of possible code words is often denoted by candidate code words

A typical example for this type of decoding is ordered statistics decoding, cf. e.g. XP011026535.

Other examples can be found in e.g. US2007214402, XP010601855, US2010058149.

H03M 13/456

This subgroup includes maximum likelihood or MAP decoding, wherein a list of all code words of the code or its dual code is processed, as disclosed e.g. in XP011026493 or XP000834637.

H03M 13/458

An example can be found in e.g. EP1475893, which discloses SISO decoding of block codes with updating of hard decisions of most reliable symbols using extrinsic information from least reliable symbols.

Another example can be found in XP011054757.

H03M 13/613

Use of properties of the code to be encoded or decoded that relate to its dual code.

This includes, for instance, decoding using the trellis of the dual code instead of that of the code itself (cf. e.g. XP011071039 or XP010560872).

H03M 13/63 and its subgroups:

These subgroups are intended to cover the combination of error control coding and other techniques.

These subgroups are in particular important when the so-called turbo principle is applied to e.g. demodulation (turbo demodulation) or equalisation (turbo equalisation); then, H03M 13/2957 is to be used to indicate the use of the turbo principle and H03M 13/6325 and H03M 13/6331, respectively, are used to indicate the non-coded constraint.

H03M 13/65 and its subgroups:

- These subgroups are in general independent of the error control code/scheme and relate to implementation aspects and the intended application (in terms of standardized communication systems)

- H03M 13/6569 is used for documents that are specific to implementations on processors or in software (e.g. software defined radio)
- H03M 13/6575 covers implementations using circuits without memory, e.g. boolean circuits; these type of circuits are often applied to encoding and decoding when the operations can be expressed by means of boolean algebra (cf. e.g. XP000354258)

## Relationships with other classification places

H03M 13/00 has relationships with a plurality of different other technical areas, wherein the relationships are characterised in that the other technical areas relate to applications and frameworks to which the H03M 13/00 specific techniques are applied.

Techniques for error control coding and forward error correction, which are characterised by their intrinsic nature, which is independent of its field of use, are to be classified in H03M 13/00. This makes H03M 13/00 a function-oriented place.

The application of techniques for error control coding or forward error correction in the sense that a function is plugged into an application without modification of the intrinsic properties of the function itself is only to classified in the respective application place (e.g. the use of a CRC check to determine whether data read from a memory is error free, the use of Reed-Solomon codes on a recording medium, the use of LDPC coded modulation in a transmitter arrangement).

If the application requires an adaptation of the techniques for error control coding or forward error correction to a particular application place, which involves a modification of the intrinsic properties of the function as well, then the classification in the function-oriented place and the application place is obligatory (e.g. the use of a CRC in a memory wherein the CRC calculation is parallelized in order to increase the read speed; this modification involves an intrinsic property of the CRC calculation; e.g. the design of an LDPC code having particular distance properties for a LDPC coded modulation scheme in a transmitter arrangement).

The application places that have relationships with H03M 13/00 are as follows:

- The mere application of error control coding or forward error correction to memories and computers: G06F 11/00, in particular G06F 11/08;
- The mere application of error control coding or forward error correction to recording: G11B 20/00, in particular G11B 20/18;
- The mere application of error control coding or forward error correction to static stores: G11C 29/00;
- The mere application of error control coding or forward error correction to arrangements at the transmitting and receiving sides of transmission systems: H04L 1/00
- The mere application of error control coding or forward error correction to packet switched networks (e.g. packet loss): H04L 12/00
- The mere application of error control coding or forward error correction to base band systems for channel estimation, detection (e.g. sequence estimation, MAP detection) and equalisation: H04L 25/00
- The mere application of error control coding or forward error correction to modulated carries systems: H04L 27/00
- The mere application of error control coding or forward error correction to signalling and control (for e.g. protocol aspects such as error control mechanisms in multimedia streaming protocols): H04L 29/00, for e.g. protocol aspects (e.g. error control mechanisms in multimedia streaming protocols)
- The mere application of error control coding or forward error correction to television systems: H04N 7/0357 and H04N 19/89
- H03M 13/00 is the application place for functions from G06F 7/00, e.g. finite field processing (G06F 7/00) for encoding or decoding of Reed-Solomon codes.

## References

### *Limiting references*

*This place does not cover:*

| | |
|---|---|
| Space-time coding | H04L 1/00 |
| Coding/decoding for MIMO systems | H04L 1/00 |
| Automatic repeat request schemes | H04L 1/00 |
| Network coding | H04L 1/00 |

### *Informative references*

*Attention is drawn to the following places, which may be of interest for search:*

| | |
|---|---|
| Implementation aspects regarding operations, e.g. finite field processing | G06F 7/00 |
| Application places in which specially adapted ECC/FEC techniques may be found | G06F 11/00, G11B 20/00, G11C 29/00, H04L 1/00, H04L 12/00, H04L 25/00, H04L 27/00, H04L 29/00, H04N 7/00 |

## Special rules of classification

The invention as such as well as additional information shall be classified

H03M 13/61 - H03M 13/65 are used to introduce a so-called 2nd dimension to the classification and are, thus, always to be used in combination with one of the subgroups of the range H03M 13/00-H03M 13/45 or the corresponding Indexing Codes

Component or constituent codes within a particular scheme are to be classified by means of the appropriate Indexing Codes; for instance, a product code built from a Reed-Muller code and a BCH code should be classified using H03M 13/2909 (product code) and H03M 13/136 and H03M 13/152 to indicate its component codes

For the search in main group H03M 13/00 it is noted that additional information has been classified in this group from 01-04-2004 onwards.

## Glossary of terms

*In this place, the following terms or expressions are used with the meaning indicated:*

| | |
|---|---|
| Product | mathematical operation |
| Turbo | the term turbo denotes the principle that soft-decision information is exchanged in an iterative manner between two decoders or between one decoder and another unit like e.g. a demodulator or equaliser;turbo is also used to denote a code (turbo code) that can be turbo decoded, e.g. a parallel concatenated convolutional code or a serial concatenated convolutional code |

## Synonyms and Keywords

*In patent documents, the following abbreviations are often used:*

| | |
|---|---|
| ACS | Add-Compare-Select |
| APP | A Posteriori Probability |

| | |
|---|---|
| BCM | Block Coded modulation |
| BP | Belief Propagation |
| CC | Convolutional Code |
| DED | Double Error Detecting |
| ECC | Error Control Codes/Coding |
| EDC | Error Detection/Detecting Code |
| EG | Euclidian Geometry |
| EXIT | EXtrinsic Information Transfer |
| FEC | Forward Error Correction |
| GF | Galois Field |
| GMD | Generalised Minimum Distance |
| LDPC | Low-Density Parity-Check |
| MAP | Maximum A Posteriori |
| LLR | Log-Liklihood Ratio |
| MDS | Maximum Distance Separable |
| ML | Maximum Likelihood |
| MLD | Maximum Likelihood Decoding |
| PCCC | Parallel Concatenated Convolutional Code |
| QC | Quasi-Cyclic |
| OSD | Ordered Statistics Decoding |
| RM | Reed-Muller |
| RS | Reed-Solomon |
| RSC | Recursive Systematic Convolutional code |
| SCCC | Serial Concatenated Code |
| SEC | Single Error Correcting |
| SISO | Soft-In Soft-Out |
| SOVA | Soft-Output Viterbi Algorithm |
| SPA | Sum-Product Algorithm |
| TB | Tail-Biting |
| TCM | Trellis-Coded Modulation |
| UEP | Unequal Error Protection |
| VA | Viterbi Algorithm |

*In patent documents, the following words/expressions are often used as synonyms:*

- "CRC", "FCS" and "BCS"
- "message passing", "sum-product algorithm", "belief propagation"
- "APP", "MAP", and "BCJR"
- "Max-LOG-MAP", "maxlogMAP", "maxAPP"
- "LDPC codes" and "Gallager codes"

# H03M 99/00

## Subject matter not provided for in other groups of this subclass

## References

### *Limiting references*

*This place does not cover:*

| | |
|---|---|
| Analogue/digital conversion; Digital/analogue conversion | H03M 1/00 |
| Conversion of analogue values to or from differential modulation | H03M 3/00 |
| Conversion of the form of the representation of individual digits | H03M 5/00 |
| Conversion of a code where information is represented by a given sequence or number of digits to a code where the same information is represented by a different sequence or number of digits | H03M 7/00 |
| Parallel/series conversion or vice versa | H03M 9/00 |
| Coding in connection with keyboards or like devices, i.e. coding of the position of operated keys | H03M 11/00 |
| Coding, decoding or code conversion, for error detection or error correction; Coding theory basic assumptions; Coding bounds; Error probability evaluation methods; Channel models; Simulation or testing of codes | H03M 13/00 |