CLASS 257, ACTIVE SOLID-STATE DEVICES (E.G.,TRANSISTORS, SOLID-STATE DIODES)

SECTION I - CLASS DEFINITION

This class provides for active solid-state electronic devices, that is, electronic devices or components that are made up primarily of solid materials, usually semiconductors, which operate by the movement of charge carriers - electrons or holes - which undergo energy level changes within the material and can modify an input voltage to achieve rectification, amplification, or switching action, and are not classified elsewhere.

SCOPE OF THE CLASS

Active solid-state electronic devices include diodes, transistors, thyristors, etc., but exclude pure resistors, capacitors, inductors, or combinations solely thereof. The latter class of devices is characterized as passive.

The subject matter to be found here includes only active solid-state devices, per se. It may include one or more such devices combined with contacts or leads, or structures configured to be tested on a semiconductor chip, or merely semiconductor material without contacts or leads where the sole disclosed use is an active solid-state device. This subject matter **does not** include active solid-state devices combined with significant circuits.

Claims reciting an integrated circuit nominally with significant metallization will be classified in Class 257, whereas otherwise, nominal recitation of an integrated circuit (i.e., without significant active solid-state device recitation) will not be sufficient to permit the device to be classified in Class 257.

KEY CONCEPTS

See Subclass References to the Current Class, below, for references that relate to key concepts and terms found in Class 257. An indication that a particular concept or term occurs in one or more subclasses does not mean that the indicated subclass or subclasses are the only places that subject matter may be found. That subject matter may possibly be found elsewhere in Class 257 listed under a related term or concept that may be broader or narrower or of the same scope.

OTHER CLASSIFICATION SYSTEMS

Each subclass definition may contain an OTHER CLASSIFICATION SYSTEMS listing that is to be used for informational purposes only. These classification listings may change at any time after their publication and are therefore not guaranteed to be current. In addition, the classification listing does not necessarily indicate the sole relationship between the U.S. Patent Classification System and foreign classifications. Even where a single classification is listed for a single U.S. subclass, a one-to-one correlation should not be inferred. As a result, information contained therein is considered to be only a guide to related subject matter.

SECTION II - LINES WITH OTHER CLASSES AND WITHIN THIS CLASS

A. Classes related to Class 257 subject matter in the sense that they employ active solid-state devices in electronic circuits and the relationship of these classes to Class 257 is mainly that of a combination to a subcombination or of a genus to a specie. See References to Other Classes, below, referencing this section.

B. Classes related to Class 257 subject matter in the sense that they employ active solid-state devices in electronic circuits and the use of active solid-state electronic devices primarily as a perfecting feature. See References to Other Classes, below, referencing this section.

C. See References to Other Classes below for classes that provide for materials used in active solid-state electronic devices.

D. See References to Other Classes, below, for classes related to Class 257 because they provide for methods of making, cleaning, coating, etc., active solid-state devices, e.g., Class 438, Semiconductor Device Manufacturing: Process.

E. See References to Other Classes, below, for Classes related to Class 257 because they provide for active solid-state electronic devices structures with a specified use, e.g., Class 136, Batteries: Thermoelectric and Photoelectric.

F. See References to Other Classes, below, for classes providing for provide for subcombination subject matter that can be used as component part of active solid-state electronic devices (e.g., lead frames) or perfect the device (e.g., a heat sink).

G. Classes which provide for passive solid-state electronic devices with names that may refer to either active or passive solid-state electronic devices, e.g., coherers, varistors, varactors. luminescent or electroluminescent

devices. The devices may be part of the main subject matter of the class or may be used as circuit elements in circuits or control or measuring systems which form the main subject matter of the class.

See References to Other Classes, below, referencing this section.

SECTION III - SUBCLASS REFERENCES TO THE CURRENT CLASS

SEE OR SEARCH THIS CLASS, SUBCLASS:

1, through 8, for bulk effect device.
2, - 5, 16, 52-63, and 646, for amorphous semiconductor material.
4, 72, 91, 144, 150, 151, 175-177, 181, 182, 207-211, 246-250, 276, 309, 317, 401, 448, 457, 459, 503, 508, 573, 584, 587, 602, 621, 625, 666-676, and 692-697, for configuration of electrode, contact, lead or pad.
4, 32, 33, 81, 91, 99, 144, 150-153, 177-179, 181, 182, 203, 207-211, 276, 377, 382-385, 459, 503, 522, 554, 573, 576, 584, 602, 621, 625, 661-677, 690-700, and 734-786, for electrical contact or lead.
6, through 8, for Gunn effect (intervalley transfer).
7, for intervalley transfer (e.g., Gunn) device in integrated circuit.
10, through 11, and 407, for controlled work function material.
10, and 11, for electron emissive layer.
10, through 27, and 104-106, for heterojunction involving quantum-mechanical tunneling.
10, and 11, for photocathode.
10, 54, 73, 155, 192-195, 217, 260, 267, 269, 275-277, 280-284, 449-457, 471-486, and 928, for Schottky barrier.
10, 11, 30-39, and 314-326, for tunneling-insulator layer.
10, 11, and 407, for work function of material, controlled, e.g., low.
13, 76, 78, 85, 90, and 94-97, for heterojunction light emitter.
13, 79-103, and 918, for light emitting device.
13, through 25, for quantum well device.
15, through 22, and 28, for superlattice.
16, 55, 63, and 65, for heterojunction in non-single-crystal material.
18, 19, and 190, for mismatched or strained lattice.
18, 19, and 190, for mismatch of lattice constant.
18, and 19, for strained layer superlattice heterojunction.
19, 76, 78, 103, 200-201, and 613-616, for alloy of two different semiconductors (e.g., $Ga_xIn_{1-x}As$).
20, 24, 27, 57-61, 66-72, 133-145, 192-195, 202-211, 213, and 252-413, for field effect devices.
20, 24, and 194, for HEMT (High electron mobility transistor).
20, 27, 187, and 192-195, for heterojunction FETs.
21, 85, 184-189, for heterojunction in light responsive device.
21, for light responsive or activated device (superlattice quantum well heterojunction).
21, 53-56, 59, 72, 80-85, 113-118, 184-189, 222, 223, 225-234, 257, 258, 290-294, 325, 428-466, 680, 681, and 749, for radiation responsive.
21, and 187, for light responsive heterojunction transistor.
21, 187, 443, and 462, for photosensitive bipolar transistor.
26, 27, and 29, for ballistic transport device.
26, 27, and 29, for ballistic transport transistor.
31, through 36, for Josephson device.
31, through 36, and 661-663, for superconductive element/device.
31, through 36, 468, and 661-663, for thermal device operated at cryogenic temperature.
33, for high temperature (30 K) Josephson device.
40, for organic semiconductor material.
41, for point contact device.
42, for Selenium (elemental).
44, through 47, for alloyed junction.
45, for thermal gradient zone melting (TGZM).
46, 104, and 105, for Esaki diode.
46, and 104-106, for p-n junction type (Esaki type) tunneling.
47, 197, 205, 273, 350, 361, 370, 378, 423, 462, 477 though 479, 511, 512, 517, 518, 525, 526, 539-543, and 552-593, for bipolar transistor structure.
47, for alloyed junction bipolar transistor.
48, and 797, for calibration or test structure.5, for array of bulk effect amorphous switches.
48, for test structures.
49, through 75, for non-single crystal, as active layer.
49, through 51, 64-75, 359, 377, 380-382, 385, 412, 505, 518, 520, 524-527, 538, 554, 576, 581, 588, and 754-757, for polycrystalline semiconductor material.
49, through 51, and 64-75, for polycrystalline active junction material.

49, through 51, and 64-75, for recrystallized active semiconductor layer.
50, and 530, for anti-fuse component or element.
50, 530, and 928, for shorted devices, in general, e.g., anti-fuse elements.
53, through 56, for amorphous semiconductor material device.
53, through 56, 108, 225, 252, and 414, for responsiveness to nonelectric signal.
55, and 63, for **alloy** of amorphous semiconductor materials.
55, 63, and 65, and 646, for silicon nitride to increase band gap of amorphous or polycrystalline silicon.
56, 58, 62, and 65, for for dangling bond.
56, 58, 62, and 68, for passivation of dangling bonds in nonsingle crystal semiconductor.
57, through 61, 66-72, and 368-401, for insulated gate FET in integrated circuit.
57, through 61, and 66-72, for FET in non-single crystal or recrystallized semiconductor material (e.g., amorphous or polycrystalline semiconductor as channel).
59, 72, and 88-93, for array as imager, or with transparent electrode, or as display (with plural light emitters).
59, 72, 449-457, and 749, for electrical contact or lead transparent to light.
59, 72, and 293, for photoresistor combined with accessing FET.
59, 72, 453, and 749, for transparent electrode.
60, 135, 136, 263-267, 302, and 328-334, for vertical channel field effect device.
64, 255, 521, 627, and 628, for crystal axis or plane.
65, for alloy of polycrystalline semiconductor materials.
66, 67, 69, 379-381, 903, and 904, for static memory cell using FET.
67, through 70, for stacked FETs.
67, 69, 70, and 74, for stacked FETs.
68, through 71, 296-313, 296, 298, 300, 906, and 908, for capacitance combined with insulated gate device. (e.g., DRAM).
68, 71, and 295-313, for insulated gate device (capacitor or combined with capacitor).
68, 71, 296-313, and 905-908, for memory device component involving a capacitor (e.g., dynamic memory cell).
68, 71, 303, and 306-309, for stacked capacitors in DRAM cell.
68, and 301-305, for capacitor in trench.
68, 283, 284, 330-334, 374, 397, 513, 514, 622, 647, and 648, for vertical walled groove in semiconductor.
69, 195, 204, 206, 338, 350, 351, 357-359, and 365-377, for CMOS.
69, 195, 204, 206, 274, 338, 350, 351, 357-359, and 369-377, for complementary field effect transistors.
74, and 278, for three-dimensional integrated circuit.
76, through 78, and 183-201, for heterojunction, generally.
76, through 78, for wide band gap semiconductor material other than GaAsP or GaAlAs.
80, through 85, for light responsive or activated device combined with light emitting device.
81, 99, 177-181, 584, 625, 675, 688, 689, 705, 707, 712-722, and 796, for heat sink.
81, 82, and 99, for housing or package for light emitter.
81, and 82, for housing or package for light emitter combined with light receiver.
81, 82, 433, 434, 680, 681, for housing or package for light responsive device.
81, 99, and 666-677, for lead frame.
83, for light coupled transistor structure.
86, and 87 for indirect band gap active layer - light emitter.
87, 131, 156, 439, 523, 590, and 608-612, for deep level dopant/impurity.
87, 126, 131, 156, 523, 590, 609-612, and 617, for recombination centers.
91, 98, 151, 175, 176, 249, 250, 276, 282-284, 309, 317, 401, 418, 435, 448, 457, 459, 503, 508, 534, 573, 587, 602, 621, 662, and 664, for shape(d) contact, electrode, conductor, or terminal.
91, 98, 294, 323, 435, and 659, for optical shield.
93, for plural light emitters in integrated circuit.
93, 374, 446, 499 and 564, for electrical isolation of components in integrated circuit.
95, 117, 118, 127, 170, 244, 283, 284, 301-305, 330-334, 418, 419, 447, 460, 466, 496, 534, 571, 586, and 618-628, for grooves, generally.
95, 170, 171, 452, 466, 496, 571, 586, 594, 600, 618, and 623-626, for mesa structure.
95, for shaped contact, electrode, etc., external of heterojunction light emitter.
98, 116, 117, 294, and 432, for light fiber, guide, or pipe.
98, for luminescent material used with light emitter.
98, 181, 418, 688, 710, 711, 728, and 730, for shaped housing or package.

98, 99, 116, 434, 680, and 681, for window (optical) for housing.
100, 433, 434, 667, 687, 767-and 796, for encapsulated.
101, 194, 219-221, 264, 269, 285, 335-345, 404, 430, 450, 458, 463, 492, 493, 497, 498, 543, 545, 548, 558, 583, 591, 592, 596, 597, 605, 606, 655-657, 927, and 929, for dopant/impurity concentration, incl., graded profile.
102, 227, 439, and 607-612, for specified, generally (e.g., photoionizable).
106, for reverse conducting diode (tunnel diode).
106, for Zener diode.
107, through 182, and 918, for regenerative switching device.
108, 252, and 421-427, for magnetic field responsive.
108, 225, 254, and 415 and-419, for device responsive to pressure.
108, 222, 225, 254, and 417-419, for strain sensor.
108, 225, 252, and 467-470, for passivating device responsive to temperature.
109, for Shockley diode.
110, and 119-131, for bidirectional device (diac, rectifier).
113, through 118, for regenerative-type switching device.
115, 123, and 157-161, for amplified gate in thyristor.
121, for reverse conducting thyristor.
121, for Static Induction Transistor (SIT) - Bipolar transistor as reverse path of bidirectional conducting thyristor.
122, 141, 146, and 162, for lateral structure in regenerative device.
124, 125, and 133-145, for FET in or combined with thyristor.
125, 137, 138, 143, and 149, for shunt, regenerative device.
125, 137, 138, 143, 149, and 154, for shorted emitter, anode or cathode, in thyristor.
127, 446, 510-522, 571, 577, and 594, for groove to define plural devices.
127, 170, 339, 372-376, 394-400, 409, 452, 484, 490, 493-495, and 605, for guard ring or region.
131, 156, 376, 424, 523, 590, and 617, for crystal damage.
133, 145, 195, 205, 273, 337, 350, 361, 362, 370, and 378, for field effect combined with bipolar type (including regenerative type) device.
134, through 136, 217, 256-287, and 504, for JFET.
136, 205, 264, 268, 269, 392, for enhancement mode.
139, through 145, and 212, for conductivity modulated transistor.
139, through 145, 147-153, for extended latching current device.
139, through 145, 147-153, and 372-376, for means to prevent latchup.
139, through 145, and 211, for conductivity modulated transistor.
142, 148, 376, 553, and 583, for doping for gain reduction.
146, 476-479, and 499-564, for structure with elec. isolated components.
150, 151, 177-181, for housing or package for regenerative type switching device.
154, 169, 194, 195, 218, 264, 523, 646, and 656, for high resistivity semiconductor region - see, also, intrinsic material; PIN device.
154, 350, 358, 359, 363, 379-381, 516, 533, 536-543, 571, 572, 577, 580-582, and 904, for resistive element (resistor) (passive device).
164, and 580-582, for ballasting of current (e.g., by resistors).
164, through 166, 560-561, 563, and 579- 581, for multiple/plural emitter.
170, for edge, beveled - preventing breakdown.
171, 496, 586, and 618+, for bevel.
171, 452, 483, and 484, for protection against edge breakdown.
171, and 496, for reverse bevels.
173, 174, 328, 355-363, 487-496, and 546, for protection against overcurrent or overvoltage.
173, 529, 665, and 910, for fuse/fusible link.
173, for overvoltage protection means in thyristor.
177, through 181, 467, 468, 573, 625, 675, 688, 705-707, and 712-722, for cooling.
178, 179, and 746-748, for stress avoidance between electrode and semiconductor.
178, through 179, 633, 747, and 748, for thermal expansion matching or compensation.
180, and 733, for stud-type mount for housing.
180, and 733, for stud mount.
181, 182, 688, 689, 726, 727, and 785 for press contact of electrode and semiconductor.
183.1, 193, 215-251, and 912, for charge transfer device.
184, through 189, for heterojunction.
185, and 191, for graded band gap.
185, for staircase (light responsive heterojunction).
187, 197, and 198, for heterojunction bipolar transistor.
198, for wide band gap emitter heterojunction bipolar transistor.
199, 481, 482, 551, and 603-606, for avalanche diode.

199, 482, and 604, for IMPATT.
199, 259, 275-277, 482, 523, 604, 624, 625, 659, 662, 664, and 728, for for microwave device component.
202+, and 909, for master slice (gate array).
202+, and 909, for gate arrays.
202, through 211, and 909, for gate arrays.
205, 273, 350, 361, 370, and 378, for bipolar combined with field effect type device.
205, 273, 350, 361, 370, and 378, for bipolar transistor structure combined with FET.
206, 208, 210, and 211, for configuration of elements in gate array.
209, for gate array with programmable signal paths.
210, and 758-760, for multi-level metallization.
212, for double-base diode (unijunction transistor).
212, for Static Induction Transistor (SIT) - Unijunction transistor.
212, for unijunction transistor.
214, for charge injection device.
215, 218, and 225-251, for surface channel charge transfer device.
216+, for bulk channel device.
216, and 285, for buried channel.
219, through 221, for nonuniform channel doping in buried channel CCD.
223, 230, and 445, for antiblooming.
223, 230, and 445, for suppression of blooming in light imager.
224, and 243, for channel confinement.
225, 253, and 414, for chemical sensor.
225, for CCD with fixed pattern memory as ROM.
228, 447, 460, for backside illumination.
239, for floating diffusion as CCD Output Tap.
239, 261, and 315-323, for floating gate.
240, for nonuniform channel thickness in CCD.
241, for parallel channels in CCD.
245, 364, and 489, for resistive electrode.
246, through 248, for nonuniform channel doping in CCD, for directionality.
249, 317, 359, 363, 364, 377, 380-382, 384, 385, 387, 407, 412, 413, 489, 505, 518, 520, 524-527, 538, 554, 576, 581, 588, 646, 754-756, 904, and 914, for polycrystalline material (including polysilicon contacts) other than active junction material.
251, for bucket-brigade device.
254, and 416, for **acoustic energy detector**.
256, and 257, for light responsive PIN device combined with JFET.
257, and 258, for JFET.
227, and 439, for photoionization.
258, 291-294, 443-448, and 911, for array of electrode field effect devices.
260, and 262, in or combined with a JFET device.
260, and 261, for memory device component involving a JFET (e.g., taper isolated or floating pn junction gate type).
265, for vertical current path JFET in integrated circuit.
266, 267, and 287, for parallel channels in JFET.
269, and 285, for nonuniform channel doping in JFET.
272, through 278, for JFET in integrated circuit.
275, through 278, 662, and 664, for stripline lead.
276, for air bridge electrical lead.
276, for air bridge contact.
283, and 284, for groove alignment of Schottky gate to source region in MESFET.
283, through 284, 330-334, for gate electrode of FET formed in groove.
286, for nonuniform channel thickness in JFET.
290, and 294, for IGFET.
291, through 294, 326, 334, 337, 338, 347-363, and 368-401, for insulated gate device (IGFET in integrated circuit).
294, 297, 340, 409, 435, 488-490, 503, 508, 630, 659-660, and 662, for shield electrode.
295, 298, and 314-326, for EPROM/EEPROM.
295, 298, 314, and 324-326, for MNOS insulated gate-type memory device component.
297, 349, 547, and 620, for means to prevent charge leakage or leakage current.
297, 349, 354, 372-376, 503, 547, and 620, for means to prevent leakage current or charge leakage.
297, 660, and 921, for protection against radiation (e.g., alpha particles).
297, 660, and 921, for radiation protection.
297, 422, and 659-660, for ionizing radiation shield, charged particles, electric or magnetic fields.
298, and 315-326, for insulated gate device (floating gate memory device).
298, and 315-323, for floating insulated gate memory-type memory device component.
299, for substrate bias (electrical generator.
301, through 305, 534, and 599, for groove involving a capacitor.
305, 354, 376, 398-400, 519, 620, 648, and 652, for channel stop.
305, 333, 374, 389, 395-399, 510-521, and 632-651, for field oxide.
312, 480, and 595-602, for voltage variable capacitance device.
314, through 326 for variable threshold insulated gate device (e.g., EEPROM, non-volatile memory MOSFET).

322, for programming of floating gate MISFET (avalanche breakdown).
323, 680, and 681, for light erasure of EPROM.
325, for oxynitride as insulator in MNOS memory IGFET.
327, through 346, for short channel.
328, and 355-363, for overvoltage protection means in IGFET.
328, and 355-363, for MOSFET gate protection.
331, 341, 342, and 401, for parallel channels in IGFET.
332, 346, 387, 388, 412, and 413, for self-aligned MOSFET gate.
333, 340, and 386-389, for reduction of gate capacitance (FET).
333, 346, 387, and 388, for overlap of gate electrode with source or drain in IGFET.
334, 337, and 338, for VMOS or DMOS short channel IGFET in integrated circuit.
336, 344, 408, and 900, for LDD (lightly doped drain) device.
339, 409, 483, 484, and 487-496, for preventing avalanche breakdown.
339, 409, and 488-490, for field relief electrode.
339, 409, 490, and 495, for floating pn junction guard region.
340, 394, and 630, for field shield electrode.
345, and 404, for nonuniform channel doping in IGFET. depletion mode.
347, through 354, and 507, for insulating substrate integrated circuit.
347, through 354, and 507, for single crystal insulating substrate.
347, through 354, and 507, for single crystal semiconductor layer on insulating substrate (SOI).
348, 391, 392, and 402-407, for depletion mode Insulated Gate FET.
349, 354, 372-376, 503, and 547, for controlling, reducing, etc. parasitics.
350, 511, 512, 525, and 555-562, for lateral bipolar transistor in integrated circuit.
354, through 374, 395-399, 501, and 506-527, for dielectric isolation.
355, through 363, for gate insulator breakdown protection in IGFET integrated circuit.
360, and 367, for insulated gate device (controlling pn junction breakdown).
361, 362, and 497-499, for punch-device.
366, for overlap of plural gate electrodes in IGFET.
368, through 401, for PN junction isolation in MOSFET integrated circuit.
374, 394-398, 626, 631-651, and 758-760, for insulating/passivating coating.
374, 396-398, 510-521, 647, and 648, for groove (dielectric isolation means).
377, 382-385, 388, 412, 413, 454-458, 486, 518, 554, 576, 588, 747, 748, 754-757, 761, 763-764, and 768-770, for refractory electrode material.
377, 382-384, 388, 412, 413, 454-456, 485, 486, 576, 587, 751, 754-757, and 768-770, for silicide.
379, through 381, and 903-904, for static RAM arrangement.
379, through 381, 516, 528-543, 903, 904, 919, and 924, for passive components in integrated circuits.
382, through 384, 576, 757, 768, and 769, for metal or silicide of platinum group metal, as ohmic contact.
383, 388, 412, 485, 486, 763, 764, and 770, for pure or alloyed titanium.
388, 407, 412, and 413, for metal or silicide of platinum group metal, as MOSFET gate.
390, and 391, for array of IGFETs.
390, and 391, for nonerasable (e.g., ROM).
390, and 391, for mask-programmed MOSFET ROM.
401, for nonuniform channel thickness in IGFET.
410, 411, 639-641, 649, and 760, for silicon nitride.
411, and 760, for composite insulator material.
411, for oxynitride as gate insulator in IGFET, in general.
422, and 659, for magnetic field shielding
423, 511, 512, 525, 526, 556, 557-562, 575, and 576, for lateral bipolar transistor structure.
423, for magnetic field sensing bipolar transistor.
426, and 469, for passivating means to reduce temperature sensitivity.
427, for magnetic field sensor in integrated circuit.
430, and 458, for light or radiation responsive PIN device, in general.
431, 466, for light responsive or activated device generally.
437, for anti-reflection coating.
444, for matrix or array of light sensor elements overlying active switching elements in integrated circuit.
446, for matrix or array of light sensors with specific isolation means in integrated circuit.
449, through 457, for Schottky barrier.
453, through 455, 485, and 486, for metal or silicide of platinum group metal, as Schottky barrier material.
458, 523, 538, and 656, for intrinsic material or region.
458, for PIN diode.

459, 676, and 786, for bonding flag or pad
465, 592, 599, 653, and 654, for configuration of junction geometry.
466, 496, 571, 586, 594, 599, 600, and 618-628, for configuration of external portion of active device.
474, for bipolar transistor with Schottky barrier transistor as emitter-base or base-collector junction.
474, through 479, 512, 525, 555, 556, and 574-576, for integrated injection logic.
477, through 479, for bipolar transistor in integrated circuit with Schottky barrier diode.
479, and 570, for anti-saturation diode.
479, for baker clamp.
486, 740, 751, and 767, for diffusion barrier.
491, and 492, for means to increase breakdown voltage in integrated circuit.
492, and 493, for RESURF device.
494, for reverse biased (electrical) pn junction guard region.
494, for reverse biased guard ring to prevent breakdown.
497, and 498, for punchthrough transistor.
504, for JFET isolation in integrated circuit (i.e., pinched-off region used for integrated circuit isolation).
509, through 521, 544-556, and 929, for isolated PN junction.
509, through 521, for PN junction isolation in integrated circuit combined with dielectric isolation.
511, 512, 525, 555, 556, 569, and 574-576, for complementary bipolar transistor structure.
511, 512, 525, 555, 556, 569, and 574-576, for complementary bipolar transistors.
511, 512, 514, 515, 517, 518, 525, 526, 539-543, and 552-563, for bipolar transistors in integrated circuit.
511, 512, 514, 517, 518, and 552-556, for bipolar transistors with pn junction isolation.
512, 569, and 574-576, for bipolar transistor structure with common active region.
512, 569, and 574-576, for complementary bipolar transistors with common active region.
512, 555, 556, and 574-576, for logic device (superintegrated) using Integrated Injection Logic (I^2L).
514, and 515, for walled emitter bipolar transistor.
522, for air isolation of integrated circuit.
531, for inductance in integrated circuit.
532, through 535, for capacitance as passive component in non-FET I.C.
540, for dynamic isolation pocket bias (electrical).
541, for pinch resistor.
544, through 556, for PN junction isolation in integrated circuit in general.
545, for reduction of isolation junction capacitance.
546, for overvoltage protection means in pn junction isolated integrated circuit.
546, for reverse voltage polarity protection, in pn junction isolated integrated circuit.
549, for collector diffused type isolation.
559, lateral transistor formed along groove.
560, through 564, for multiple/plural collectors.
560, 563, and 579-581, for plural emitters in bipolar transistor.
562, for logic device (superintegrated) using Current Hogging Logic (CHL).
565, through 593, for bipolar transistor structure, in general.
571, for groove resistor in Darlington bipolar device.
573, and 584, for housing or package for bipolar transistor devices.
592, for configuration of bipolar transistor base region.
602, for housing or package for voltage-variable capacitance device.
607, and 917, for plural dopants of same conductivity type.
610, for platinum (as deep level dopant).
620, for scribe line or region.
624, for prevention of skin effect, microwave device, by low resistance ohmic contact along mesa surface.
626, and 629-652, for passivation of semiconductor surface.
634, for passivating glass with ingredient to adjust softening or melting temperature.
639, and 649, for oxynitride as passivating insulating layer.
642, 643, and 759, for organic insulating material or layer.
643, 759, and 788, for polyamide.
643, 759, and 792, for polyimide.
653, 654, for shaped PN junction.
655, for reverse doping concentration gradient profile.
656, for PIN device in general.
657, for stepped profile.
657, for stepped dopant concentration profile.
660, for housing or package for radiation shielded device.
662, and 664, for transmission line lead.
663, for superconductive contact or lead on integrated circuit.

669, 670, 673, 674, 676, 688, 689, 692-697, 728, 735-739, 752, 758, 773-776, and 780-786, for shaped contact, electrode, etc.
669, for lead frame having stress relief.
676, for die bonding flag.
676, for lead frame-type mount for chip.
678, through 733, for housing or package, generally.
679, and 922, for smart card (e.g., “credit card” integrated circuit package).
686, for stacked housings.
700, 701, and 703-707, for ceramic housing or package material.
705, for high thermal conductivity ceramic for package.
711, for metal housing with mount for chip.
713, for cooling of housing or contents for integrated circuit.
714, through 716, for liquid coolant.
719, for press contact of heat sink and semiconductor.
720, for high thermal conductivity insert in heat sink.
731, for mount for housing.
732, for flanged type mount for housing.
735, through 739, 746, 758-760, 773-776, 780-781, 786, 920, 923, 926, for configuration of electrode, etc.
738, 780, and 781, for ball-shaped leads, contacts or bonds.
740, for prevention of spiking of contact metal.
741, through 745, and 751, for gold (deep level dopant as contact or electrode).
742, and 743, for dopant/impurity conductivity type in electrical contact material.
746, for composite electrode material.
746, for electrode material.
749, for electrode transparent to light.
751, 767, and 915, for titanium nitride.
758, through 760, for multiple metallization layers separated by insulating layer on integrated circuit.
760, for oxynitride between metal levels in integrated circuit.
764, 765, and 768-771, for alloy of materials forming electrical contacts.
767, for electromigration prevention or reduction.
777, for chip on chip mount for chip.
778, for flip chip mount for chip.
779, and 780-784, for die or lead bond.
782, and 783, for die bond.
900, for MOSFET type gate sidewall insulating spacer.
901, for MOSFET substrate bias (electrical).
901, for MOSFET substrate bias.
902, for FET with metal source region.
903, and 904, for configuration of FETs for Static Memory Cell (SRAM).
905, through 908, for configuration of Dynamic Memory (DRAM).
905, for trench shared by plural DRAM cells.
906, Electrode use for accessing capacitance, in DRAM.
910, for array of diodes.
911, for vidicon array (cross-reference collection).
915, for titanium nitride.
919, for parallel electrical connections to average out manufacturing variations.
920, for parallel electrical connections to reduce resistance.
922, for anti-tamper device.
922, for diode arrays.
922, for anti-tamper or inspection means for
923, for conductor aspect ratio.
925, for bridge rectifier module.
927, for shaped depletion layer.
930, for Peltier cooling (cross-reference collection).

SECTION IV - REFERENCES TO OTHER CLASSES

SEE OR SEARCH CLASS:

29, Metal Working, subclasses 25.01+ for process and apparatus for making barrier layer or semiconductor devices not elsewhere classified; subclass 25.35 for piezoelectric device making not elsewhere classified; subclasses 25.41+ for electric condenser making not elsewhere classified; subclasses 592.1+ for process of mechanical manufacture of electrical devices, not elsewhere classified; and subclasses 825+ for electrical conductor manufacturing processes, including subclass 827 regarding beam lead frames and beam leads. (class providing for methods of making, cleaning, coating, etc., active solid-state devices, See Lines With Other Classes and Within This Class, D).

29, Metal Working, subclass 612 for making thermally variable resistors. (See G, Lines With Other Classes and Within This Class, above).

29, Metal Working, appropriate subclasses for manufacturing methods of beam lead frame or beam lead devices. (Class providing for subcombination subject matter used as component part of active solid-state electronic devices. See Lines with Other Clases and Within This Class, F, above).

40, Card, Picture, or Sign Exhibiting, subclass 544 for electroluminescent signs. (See B, Lines With Other Classes and Within This Class, above.)

62, Refrigeration, subclasses 3.2+ for thermoelectric, e.g., Peltier effect cooling processes and apparatus. (See B, Lines With Other Classes and Within This Class, above.)

65, Glass Manufacturing, subclasses 138+ for Electronic envelope header, terminal, or stem making means and subclass 155 for electronic device making involving fusion bonding. (Class providing for methods of making, cleaning, coating, etc., active solid-state devices, See Lines With Other Classes and Within This Class, D).

73, Measuring and Testing, subclass 31.06 for gas analysis semiconductor detector details; subclass 777 for semiconductor stress sensor structure; and subclass 754 for semiconductor type fluid pressure gauges. (Class employing active solid-state devices in electronic circuits. See Lines With Other Classes and Within This Class, A, above).

84, Music, subclasses 676 and 678 for transistorized analog oscillator circuits. (See B, Lines With Other Classes and Within This Class, above.)

102, Ammunition and Explosives, subclass 202.4 for semiconductor voltage variable resistance shunts in devices used to prevent accidental fuse ignition. (See G, Lines With Other Classes and Within This Class, above)

102, Ammunition and Explosives, subclass 202.4 for semiconductor fuse shunts and subclass 220 for silicon controlled rectifier ignition or detonation switch devices. (See B, Lines With Other Classes and Within This Class, above.)

116, Signals and Indicators, digest 35 for electroluminescent dials. (See B, Lines With Other Classes and Within This Class, above.)

117, Single-Crystal, Oriented-Crystal, and Epitaxy Growth Processes; Non-Coating Apparatus Therefor, for processes and non-coating apparatus for growing therein-defined single-crystal of all types of materials, including those which may be suitable as or to produce an active solid-state device. Class 118 generally provides for coating apparatus, including single-crystal (e.g., epitaxy) coating means. (Class providing for methods of making, cleaning, coating, etc., active solid-state devices, See Lines With Other Classes and Within This Class, D).

118, Coating Apparatus, subclass 900 for semiconductor vapor doping. (Class providing for methods of making, cleaning, coating, etc., active solid-state devices, See Lines With Other Classes and Within This Class, D)

123, Internal-Combustion Engines, subclasses 650+ for ignition systems with power supplies having diode and transistor features. (See B, Lines With Other Classes and Within This Class, above.)

134, Cleaning and Liquid Contact With Solids, subclasses 1.2, 1.3, and 902 for semiconductor wafer cleaning. (Class providing for methods of making, cleaning, coating, etc., active solid-state devices, See Lines With Other Classes and Within This Class, D, above).

136, Batteries: Thermoelectric and Photoelectric, subclasses 203+ for Peltier effect device; subclasses 200+ for batteries which generate electricity under the action of heat (thermoelectric); and subclasses 243+ for batteries which generate electricity under the action of light, such as photovoltaic batteries, some of these batteries utilize potential barrier layers. (class providing for active solid-state electronic devices structures with a specified use.)

148, Metal Treatment, subclasses 33+ for PN type barrier layer stock material treatment and numerous digests concerning treatment of semiconductor materials, dopants, and active solid-state electronic devices. (Class providing for methods of making, cleaning, coating, etc., active solid-state devices, See Lines With Other Classes and Within This Class, D, above).

148, Metal Treatment, digest 171 for metal treatment involving varistors. (See G, Lines With Other Classes, above).

165, Heat Exchange, subclasses 80.2+ and 104.33 for electrical device or component heat exchangers. (Class providing for subcombination subject matter used as component part of active solid-state electronic devices. See Lines with Other Clases and Within This Class, F, above).

174, Electricity: Conductors and Insulators, subclasses 15.1 through 16.3 for fluid cooling of electrical conductors or insulator; subclasses 250-268 for printed circuit devices; and subclasses 520-64 for housings with electric devices or mounting means. (Class employing active solid-state devices in electronic circuits. See Lines With Other Classes and Within This Class, A, above).

178, Telegraphy, subclass 117 for coherer type AC systems. (See B, Lines With Other Classes and Within This Class, above.)

178, Telegraphy, subclass 117 for coherer type AC systems. (See G, Lines With Other Classes and Within This Class, above).

194, Check-Actuated Control Mechanisms, subclasses 216+ for value accumulator having solid-state circuitry. (See B, Lines With Other Classes and Within This Class, above.)

204, Chemistry: Electrical and Wave Energy, subclasses 400+ for active solid-state devices used in measuring and testing involving electrolytic analysis. (Class employing active solid-state devices in electronic circuits. See Lines With Other Classes and Within This Class, A, above).

204, Chemistry: Electrical and Wave Energy, subclass 192.25 for semiconductor coating, forming, or etching by sputtering. (Class providing for methods of making, cleaning, coating, etc., active solid-state devices, See Lines With Other Classes and Within This Class, D, above)

216, Etching a Substrate: Processes, subclass 16 for active solid state devices involved in an etching process. (Class providing for methods of making, cleaning, coating, etc., active solid-state devices, See Lines With Other Classes and Within This Class, D, above).

219, Electric Heating, subclass 501 for automatic regulation or control means for heating devices which include semiconductor, e.g., transistor, means. (See B, Lines With Other Classes and Within This Class, above.)

228, Metal Fusion Bonding, subclass 123 for processes of bonding metal to semiconductor-type material and subclasses 179+ for processes of bonding electrical device (e.g., semiconductor) joints. (Class providing for methods of making, cleaning, coating, etc., active solid-state devices, See Lines With Other Classes and Within This Class, D, above).

250, Radiant Energy, subclass 492.2 for irradiation of semiconductor devices. (Class providing for methods of making, cleaning, coating, etc., active solid-state devices, See Lines With Other Classes and Within This Class, D, above).

250, Radiant Energy, subclass 338.4 for infrared responsive semiconductor devices, subclasses 370.01-370.15 for invisible radiant energy responsive semiconductor devices; subclass 371 for invisible radiant energy responsive methods using semiconductor devices; subclass 492.2 for irradiation of semiconductor devices; subclasses 552 and 553 for photocell circuits and apparatus involving solid-state light sources; subclasses 211 for photocells including photosensitive junctions; and subclasses 208.1-208.6 for plural photosensitive elements, including arrays. (Class employing active solid-state devices in electronic circuits. See Lines With Other Classes and Within This Class, A, above).

264, Plastic and Nonmetallic Article Shaping or Treating: Processes, subclass 272.11 for electrical component encapsulating processes, including subclass 272.17 for encapsulating semiconductor or barrier layer device. (Class providing for methods of making, cleaning, coating, etc., active solid-state devices, See Lines With Other Classes and Within This Class, D, above).

252, Compositions, subclass 62.3 for barrier layer device compositions, e.g., N-material, P-material and, subclasses 500+ for electrically conductive or emissive compositions. (Class providing for materials used in active solid-state devices, Lines With Other Classes and Within This Class, C, above).

273, Amusement Devices: Games, digest 24 for luminescent devices. (See B, Lines With Other Classes, above.)

307, Electrical Transmission or Interconnection Systems, subclasses 401+ for nonlinear reactor systems which typically employ active solid-state devices; subclass 91 for magnetic or electrostatic field shielding; and subclasses 109+ for systems involving capacitors.

310, Electrical Generator or Motor Structure, subclass 303 for energy conversion devices employing pn semiconductor junction devices, and digest 3 for Hall effect generators and converters. (See B, Lines With Other Classes and Within This Class, above.)

313, Electric Lamp and Discharge Devices, subclasses 498+ for electric lamp and discharge devices having solid-state luminescent materials, including nominally recited luminescent semiconductor type materials; subclasses 329 and 367+ for mosaic electrodes; subclasses 366+ for semiconductor depletion layer type image pickup tubes; subclass 463 for electroluminescent cathoderay tube screens; subclasses 346 and 346 for photoemissive cathodes; and subclass 504 for solid-state organic phosphor material luminescent devices. (Class employ-

ing active solid-state devices in electronic circuits. See Lines With Other Classes and Within This Class, A, above).

315, Electric Lamp and Discharge Devices: Systems, subclass 12.1 for secondary emissive stage in a cathoderay tube; subclass 407 for a deflection coil circuit including a diode; subclass 408 for deflection coil circuits including a solid-state switch; and digest 7 for starting and control circuits using transistors. (Class employing active solid-state devices in electronic circuits. See Lines With Other Classes and Within This Class, A, above).

323, Electricity: Power Supply or Regulation Systems, subclasses 229+ for power supply or regulation systems using a diode in shunt with a source or load; subclasses 237+, 254, 257, 258, 263, 265+, and 292 for output level devices employing three or more terminal semiconductor devices; subclass 300 for input level devices or systems employing three or more terminal semiconductor devices; subclasses 311+ for self-regulating systems employing three or more terminal semiconductor devices; subclasses 325+, 339, 343, and 349+ for external or operator controlled systems employing three or more terminal semiconductor devices; subclass 360 for superconductor type transformers or inductors; digest 902 for device with optical coupling to a semiconductor; and digest 907 for temperature compensation of a semiconductor. (Class employing active solid-state devices in electronic circuits. See Lines With Other Classes and Within This Class, A, above).

318, Electricity: Motive Power Systems, subclass 681 for positional servomechanisms using solid-state servo amplifiers. (see B, Lines With Other Classes and Within This Class, above.)

315, Electric Lamp and Discharge Devices: Systems, subclass 311 for variable impedance device in automatic regulator in supply circuit of an electric lamp or discharge device. (See G, Lines With Other Classes and Within This Class, above).

318, Electricity: Motive Power Systems, subclass 662 for variable capacitor type positional servo systems and subclasses 788 and 792 for variable temperature impedance (e.g., resistor) elements in induction motor systems. (See G, Lines With Other Classes and Within This Class, above).

320, Electricity: Battery or Capacitor Charging or Discharging, appropriate subclass for an active solid-state device included in a charging or discharging circuit for a battery or capacitor. (See B, Lines With Other Classes, above.)

322, Electricity: Single Generator Systems, digest 5 for Hall effect elements. (see B, Lines With Other Classes and Within This Class, above.)

323, Electricity: Power Supply or Regulation Systems, subclass 298 for output level responsive devices including a variable resistor. (See G, Lines With Other Classes and Within This Class, above).

324, Electricity: Measuring and Testing, subclasses 765+ for diode, SCR and transistor testing and subclasses 244+ for magnetometers, many of which employ active solid-state devices, e.g., subclasses 248 (thin film), 251 (Hall plate) and 252 (semiconductor type solid-state or magneto resistive). (Class employing active solid-state devices in electronic circuits. See Lines With Other Classes and Within This Class, A, above).

327, Miscellaneous Active Electrical Nonlinear Devices, Circuits, and Systems, appropriate subclasses for miscellaneous nonlinear circuits utilizing an active device. (Class employing active solid-state devices in electronic circuits. See Lines With Other Classes and Within This Class, A, above).

327, Miscellaneous Active Electrical Nonlinear Devices, Circuits, and Systems, subclasses 185+ for a stable state circuit utilizing an electron tube and a transistor and subclasses 568+ for a miscellaneous negative resistance circuit. (See B, Lines With Other Classes and Within This Class, above.)

329, Demodulators, subclass 370 for diode demodulators and subclass 371 for coherer type demodulators. (See B, Lines With Other Classes and Within This Class, above.)

329, Demodulators, subclass 370 for diode demodulators and subclass 371 for coherer type demodulators. (See G, Lines With Other Classes and Within This Class, above).

330, Amplifiers, subclass 145 for diode type variable impedances for signal channel controlled by a separate control path and subclasses 282+ for semiconductor amplifier devices with gain control means and feedback means acting as a variable impedance.

330, Amplifiers, subclass 4.9 for semiconductor type parametric amplifiers; subclass 183 for DC interstage coupling with as nonlinear

device; and subclasses 250+ for semiconductor amplifying devices. (Class employing active solid-state devices in electronic circuits. See Lines With Other Classes and Within This Class, A, above).

331, Oscillators, subclass 51 for semiconductor type cascade or tandem connected oscillators and subclasses 107-117 for solid-state active element oscillators. (Class employing active solid-state devices in electronic circuits. See Lines With Other Classes and Within This Class, A, above).

331, Oscillators, subclasses 36+ for AFC devices using particular frequency control means, including reactance devices (e.g., variable capacitors) and subclass 177 for voltage sensitive capacitor type frequency adjusting means. (See G, Lines With Other Classes and Within This Class, above).

332, Modulators, subclasses 105, 116, 135+, 146, 152, 168, and 178 for modulators with discrete semiconductor devices (subclass 136 includes varactors). (See B, Lines With Other Classes and Within This Class, above.)

332, Modulators, subclasses 105, 116, 135+, 146, 152, 168, and 178 for modulators with discrete semiconductor devices (subclass 136 includes varactors). (See G, Lines With Other Classes and Within This Class, above).

333, Wave Transmission Lines and Networks, subclass 263 for variable impedance devices connected in circuit with a long line element or component. (See G, Lines With Other Classes and Within This Class, above).

333, Wave Transmission Lines and NetWorks, subclasses 103 and 104 for branched circuits with switching means having semiconductor operating means; subclass 165 for frequency or time domain filters using charge transfer devices; subclasses 216 and 217 for negative impedance devices; subclass 247 for semiconductor mounts for strip type long line elements; and subclass 99 for super conductive devices. (class employing active solid-state devices in electronic circuits. See Lines With Other Classes and Within This Class, A, above)

334, Tuners, subclasses 66 and 69 for series tuned circuits with variable impedance elements.

334, Tuners, subclass 15 for semiconductor reactance tuning circuits. (See B, Lines With Other Classes and Within This Class, above.)

338, Electrical Resistors, subclass 1 for coherer type resistors, subclass 22 for semiconductor type thermistors, and subclass 32 for magnetic field responsive devices, including Hall effect types and super conductive types. (Class employing active solid-state devices in electronic circuits. See Lines With Other Classes and Within This Class, A, above).

338, Electrical Resistors, subclass 1 for coherer type resistors; subclass 22 for semiconductor type thermistors; and subclass 32 for magnetic field responsive devices, including Hall effect types and superconductive types. (See G, Lines With Other Classes and Within This Class, above).

343, Communications: Radio Wave Antennas, subclass 745 for antennas with variable reactance tuning; subclass 750 for adjustable lumped reactance antenna tuning; and subclass 861 for adjustable impedance matching network leadins. (See G, Lines With Other Classes and Within This Class, above).

340, Communications: Electrical, subclass 598 for barrier layer thermal sensors in condition responsive device; subclass 815.03 for a visual indicator using a light emitting diode; subclasses 2.2-2.31 for a channel selecting matrix; and subclasses 14.1-14.69 for a decoder matrix.

341, Coded Data Generation or Conversion, subclasses 133+ for analog-to-digital conversion with particular solid-state devices; subclass 150 for digital to analog conversion using charge coupled devices or switched capacitances; and subclass 172 for analog to digital conversion using charge transfer devices. (See B, Lines With Other Classes and Within This Class, above.)

345, Computer Graphics Processing and Selective Visual Display Systems, subclasses 30+ for selective visual display systems which may employ active solid-state device light sources, including subclasses 44 and 82 for visual display systems having solid-state light emitters. (class employing active solid-state devices in electronic circuits. See Lines With Other Classes and Within This Class, A, above).

348, Television, subclasses 272+ and 294+ for solid-state image sensors in television cameras and subclasses 800+ for electroluminescent video display with solid-state scanned matrix. (class employing active solid-state devices in electronic circuits. See Lines With Other Classes and Within This Class, A, above).

358, Facsimile and Static Presentation Processing, subclasses 482 and 483 solid-state picture generators, including charge coupled devices. (Class employing active solid-state devices in

electronic circuits. See Lines With Other Classes and Within This Class, A, above).

359, Optical: Systems and Elements, subclass 248 for semiconductor polarization type light modulators and subclasses 321+ for modulators having significant chemical composition or structure. (Class employing active solid-state devices in electronic circuits. See Lines With Other Classes and Within This Class, A, above).

361, Electricity: Electrical Systems and Devices, subclass 2 for solid-state switch type arc suppressors; subclasses 98, 100, and 101 for current fault responsive sensors involving semiconductor active solid-state devices; subclasses 196+ for semiconductor time delay devices; subclass 205 for threshold devices including SCR thyratrons; subclasses 275.1+ for electrical, e.g., fuse element for electrolytic capacitors; subclasses 277+ for variable capacitor not involving active solid-state devices; subclasses 525 for solid electrolytic capacitors with significant semiconductor; subclasses 679+ for cooling devices, housings, supports, electrical contacts, etc., for diverse electrical components; subclass 421 for lead frames; and subclasses 523+ for solid electrolytic capacitors. (class employing active solid-state devices in electronic circuits. See Lines With Other Classes and Within This Class, A, above)

361, Electricity: Electrical Systems and Devices, subclass 188 for variable impedance condition responsive devices for relay or solenoid safety or protection; and subclasses 277+ for variable electrostatic capacitors. (See G, Lines With Other Classes and Within This Class, above)

361, Electricity: Electrical Systems and Devices, subclass 421 for lead frames. (Class providing for subcombination subject matter used as component part of active solid-state electronic devices. See Lines with Other Clases and Within This Class, F, above)

362, Illumination, subclass 84 for light source or light source support and luminescent material and subclass 800 (cross-reference art collection) for light emitting diode light sources. (See B, Lines With Other Classes and Within This Class, above.)

363, Electric Power Conversion Systems, subclasses 10+ for combined phase and frequency conversion using a semiconductor device converter, and subclasses 13-147 for current conversion devices many of which explicitly call for semiconductor active solid-state devices, and subclasses 159-163 for frequency conversion using semiconductor type devices. (See B, Lines With Other Classes and Within This Class, above.)

365, Static Information Storage and Retrieval, subclasses 52+ for hardware, including shields, for storage elements; subclass 71 for negative resistance; and subclass 72 for transistor or diode interconnection arrangement; subclass 96 for fusible link storage elements; subclasses 103-105 for semiconductive semipermanent read only systems; subclasses 106+ for systems involving radiant energy, including subclasses 109-115 for photoconductive, electroluminescent, amorphous, semiconductive and diode devices; subclasses 129+ for systems using a particular element, including subclasses 154-188 for systems using particular elements including active solid-state devices; subclasses 185.01+ for floating gate memory storage (e.g., flash memory); and subclasses 208 and 212 for semiconductive differential (e.g., thermal) noise suppression means in read/write circuits. (Class employing active solid-state devices in electronic circuits. See Lines With Other Classes and Within This Class, A, above).

367, Communications, Electrical: Acoustic Wave Systems and Devices, subclasses 140+ for signal transducers which may be active solid-state devices, and including support structures, diaphragm, and pressure compensation means. (See B, Lines With Other Classes and Within This Class, above.)

368, Horology: Time Measuring Systems or Devices, subclass 83 for solid body light emitters, e.g., diodes; subclasses 86 and 87 for transistorized pulse transforming means; subclasses 56+ for solid-state oscillating time base circuits; and subclasses 239+ for optical display devices, including subclass 241 for solid-state, e.g., LED light emitting displays. (See B, Lines With Other Classes and Within This Class, above.)

369, Dynamic Information Storage or Retrieval, subclass 44.12 for optical servo systems having solid-state optical elements; subclasses 121+ for light sources, including solid-state light source; subclass 145 for semiconductive information handling transducers. (class employing active solid-state devices in electronic circuits. See Lines With Other Classes and Within This Class, A, above)

372, Coherent Light Generator, subclasses 43 through 50 for semiconductor layers and subclass 75 for semiconductor optical laser pump devices. (class employing active solid-state devices in electronic circuits. See Lines With Other Classes and Within This Class, A, above).

374, Thermal Measuring and Testing, subclass 178 for barrier layer (e.g., semiconductor junction) heat sensors and subclasses 183+ for current modifying sensors. (Class employing active solid-state devices in electronic circuits. See Lines With Other Classes and Within This Class, A, above).

377, Electrical Pulse Counters, Pulse Dividers, or Shift Registers: Circuits and Systems, subclasses 57 through 63 for charge transfer device systems; subclass 74 for input circuits involving field-effect transistors; subclass 79 and 117 for transfer means including a field effect transistor; and subclass 93 for superconductive elements. (class employing active solid-state devices in electronic circuits. See Lines With Other Classes and Within This Class, A, above)

378, X-Ray or Gamma Ray Systems or Devices, subclass 104 for X-ray source power supplies with specified rectifier. (See B, Lines With Other Classes and Within This Class, above.)

379, Telephonic Communications, subclass 294 for semiconductor line finders. (See B, Lines With Other Classes, above.)

381, Electrical Audio Signal Processing Systems and Devices, subclass 100 for crossover filters with active devices and subclass 175 for semiconductor junction microphones. (see B, Lines With Other Classes and Within This Class, above.)

388, Electricity: Motor Control Systems, subclasses 917 through 920 for thyristor or SCR devices or control circuit elements and subclass 926 for a specific feedback control or device which controls a solid-state device in a motor circuit.

388, Electricity: Motor Control Systems, subclass 807 for variable impedance type field control circuits and subclasses 855+ for selectable or variable impedance armature control devices. (see G, Lines With Other Classes and Within This Class, above)

427, Coating Processes, subclasses 58 through 126.6 , especially subclasses 62 and 63, 66, 74-76, 79-81, 96.1-99.5, 100, and 101-103 for coating processes to make an electrical product (for methods of making, cleaning, coating, etc., active solid-state devices, see Lines With Other Classes and Within This Class, D., above).

428, Stock Material or Miscellaneous Articles, subclass 620 for composite metallic stock having a semiconductor component, subclasses 690 and 691 for fluorescent, phosphorescent or luminescent inorganic layer composites; subclasses 917 for electroluminescent material; and subclasses 928-931 for materials with special properties, including magnetic properties, electrical contact features and superconductivity. (Class providing for materials used in active solid-state devices, Lines With Other Classes and Within This Class, C, above).

430, Radiation Imagery Chemistry: Process, Composition, or Product Thereof, subclasses 56 through 96 for radiation sensitive compositions or products; subclass 139 for luminescent imaging process, composition or product; and subclass 900 for donor-acceptor complex photoconductors. (Class providing for materials used in active solid-state devices, Lines With Other Classes and Within This Class, C, above)

430, Radiation Imagery Chemistry: Process, Composition, or Product Thereof, subclasses 56 through 96 for radiation sensitive compositions or products; subclass 139 for luminescent imaging process, composition or product; and subclass 900 for donor-acceptor complex photoconductors. (Class providing for methods of making, cleaning, coating, etc., active solid-state devices, See Lines With Other Classes and Within This Class, D, above).

438, Semiconductor Device Manufacturing: Process, for (a) combined operations (steps) for producing a semiconductor substrate having a junction, usually between p-type and n-type material or (b) a unit operation involving semiconductor material, not elsewhere provided; see the search notes therein. (class providing for methods of making, cleaning, coating, etc., active solid-state devices, See Lines With Other Classes and Within This Class, D, above).

439, Electrical Connectors, appropriate subclasses for features related or analogous to electrical contact or housing features of active solid-state devices, e.g., subclasses 271+ for sealing elements, or subclasses 449+ for stress relief means for conductor to terminal joint. (class employing active solid-state devices in electronic circuits. See Lines With Other Classes and Within This Class, A, above).

455, Telecommunications, subclass 253.1 for semiconductor gain, level or volume control; subclass 291 for receivers having a wave collector with coupling to a stage of the receiver using an active device, and subclass 333 for transistorized or integrated circuit type frequency conversion structure or circuitry. (see B, Lines With Other Classes and Within This Class, above.)

455, Telecommunications, subclasses 261 and 262 for variable reactance, e.g., variable capacitance type automatic local oscillator control devices. (see G, Lines With Other Classes and Within This Class, above)

505, Superconductor Technology: Apparatus, Material, Process, subclasses 150+ for high temperature (T_c > 30 K) superconducting devices, and particularly subclasses 161 and 162 for bolometers or SQUIDs, subclasses 190+ for Josephson junctions, per se, and subclasses 191+ for other thin film solid-state devices; and pertinent cross-reference art collections, including subclasses 831+, for static information storage and retrieval system or device; subclasses 857+ for nonlinear solid-state device, system, or circuit; subclasses 873+ for active solid-state devices; subclass 883 for housing and mounting assemblies with plural diverse electrical components; subclasses 884+ for conductors; and subclasses 900+ for heat exchangers. (see B, Lines With Other Classes and Within This Class, above.)

505, Superconductor Technology: Apparatus, Material, Process, subclasses 150+ for high temperature (T_c > 30 K) superconducting devices, and particularly subclasses 161 and 162 for bolometers or SQUIDs, subclasses 190+ for Josephson junctions, per se, and subclasses 191+ for other thin film solid-state devices; and pertinent cross-reference art collections, including subclasses 831+, for static information storage and retrieval system or device; subclasses 857+ for nonlinear solid-state device, system, or circuit; subclasses 873+ for active solid-state devices; subclass 883 for housing and mounting assemblies with plural diverse electrical components; subclasses 884+ for conductors; and subclasses 900+ for heat exchangers. (Class providing for materials used in active solid-state devices, Lines With Other Classes and Within This Class, C, above)

600, Surgery, subclasses 486+ and 505 for active solid-state devices inserted inside a body and used for measuring and testing. (class employing active solid-state devices in electronic circuits. See Lines With Other Classes, A, above)

708, Electrical Computers: Arithmetic Processing and Calculating, subclass 190 for integrated circuit type digital computers.

716, Data Processing: Design and Analysis of Circuit or Semiconductor Mask, subclasses 1 through 18 for circuit design and subclasses 19-21 for design of a semiconductor mask.

902, Electronic Funds Transfer, subclass 26 for identification, means with a semiconductor chip, e.g., a smart card. (see B, Lines With Other Classes and Within This Class, above.)

D10, Measuring, Testing or Signalling Instruments, subclass 77 for transistor testers. (see B, Lines With Other Classes and Within This Class, above.)

D13, Equipment for Production, Distribution or Transformation of Energy, appropriate subclass for semiconductor, transistor or integrated circuit energy conversion or transformation. (see B, Lines With Other Classes and Within This Class, above.)

SECTION V - GLOSSARY

ACCEPTOR IMPURITY

An atom or ion different from or foreign to, but present in, a semiconductor material and which has insufficient valence electrons to complete the normal bonding arrangement in the semiconductor crystal structure. An acceptor impurity accepts an electron from an adjacent atom to create a hole. Acceptor impurities are also referred to as p-type impurities. Common acceptor impurities in silicon or germanium are boron, gallium, and indium.

ACTINIDES

Ac, Th, Pa, U, Np, Pu, Am, Cm, Bk, Cf, E, Fm, Mv, No, Lw.

ALKALI METALS

Li, Na, K, Rb, Cs, Fr.

ALKALINE-EARTH METALS

Ca, Sr, Ba, Ra.

ACTIVE SOLID-STATE ELECTRONIC DEVICE

An electronic device or component that is made up primarily of solid materials, usually semiconductors, which operates by the movement of charge carriers - electrons or holes - which undergo energy level changes within the material and can modify an input voltage to achieve rectification, amplification, or switching action. Active solid-state electronic devices include diodes, transistors, thyristors, etc., but exclude pure resistors, capacitors, inductors, or combinations solely thereof. The latter class of devices is characterized as passive.

ALLOY JUNCTION

A fused junction produced by combining one or more elemental impurity metals with a semiconductor. Typical alloyed junctions include indium- germanium and aluminum-silicon.

ALLOY TRANSISTOR

A transistor in which the emitter-base and collector-base junctions are alloy junctions.

AVALANCHE BREAKDOWN

A sudden change from high dynamic electrical resistance to very low dynamic resistance in a reverse biased semiconductor device, e.g., a reverse biased junction between p-type and n-type semiconductor materials, wherein current carriers are created by electrons or holes which have gained sufficient speed to dislodge valence electrons. Avalanche breakdown can cause structural damage to a semiconductor device.

AXIAL LEAD

A wire lead coming from the end of and along the axis of a resistor, capacitor, or other component.

BACK BONDED

The bonding of active chips to a substrate using the back of the chip opposite the side containing active solid-state devices.

BALL BOND

A bond formed by a round, ball-shaped lead on a semiconductor device.

BALLISTIC TRANSPORT DEVICE

An active solid-state electronic device in which an active layer is present through which carriers* pass, wherein the active layer is thinner than the mean free path of the carriers* in the material in that layer, so that carriers* can pass through the layer without scattering. Carriers* are typically injected into the ballistic transport layer as “hot” carriers*, having an energy, in the case of electrons, substantially greater than the minimum of the conduction band*, or in the case of holes, substantially lower than the maximum of the valence band. Ballistic electron injectors include heterojunctions, tunnel barriers, and punchthrough (e.g., planar doped or camel) barriers.

BAND GAP

The difference between the energy levels of electrons bound to their nuclei (valence electrons) and the energy levels that allow electrons to migrate freely (conduction electrons). The band gap depends on the particular semiconductor involved.

BARRIER REGION OR LAYER

A region which extends on both sides of a semiconductor junction in which all carriers are swept away from the junction region. The region is depleted of carriers. This is also referred to as a depletion region.

BARRITT DIODE

Barrier injection transit time diode. A bipolar or device in which a type of breakdown known as punchthrough occurs and wherein the punchthrough structure device is operable at microwave frequencies. In bipolar transistors a direct current path is formed from emitter to collector due to the formation of a depletion region throughout the base region and charge carriers from the emitter punch through to the collector. Carriers flowing from the emitter to the collector take a controlled time to pass through the depletion layer, leading to a controlled delay in current after a voltage is applied, and effective negative impedance.

BASE REGION

The region between the emitter and collector of a bipolar transistor into which minority carriers are injected by the emitter.

BASE CURRENT

The electrical current that flows in the base terminal of a bipolar transistor.

BEAM LEADS

Flat, metallic leads which extend beyond the edges of a chip component like wooden beams extend from a roof overhang. Beam leads are used to interconnect a component to film circuitry.

BIAS

A direct current or voltage applied to an active solid-state device that establishes certain operating characteristics of the device.

BI-FET

An active solid-state electronic device that contains both bipolar and field effect transistors.

BILATERAL

A characteristic of an active solid-state electronic device that permits it to support current flow in opposite directions.

BINARY COMPOUND

A substance that always contains the same two elements in a fixed atomic ratio.

BIPOLAR

An active solid-state electronic device in which both positive and negative current carriers are used to support current flow.

BIPOLAR TRANSISTOR

An active solid-state electronic device with a base electrode and two or more junction electrodes in which both positive and negative current carriers are used to support current flow.

BLOCH WAVELENGTH

The effective wavelength of electrons in a semiconductor crystal, sometimes referred to as a **wave packet** or **wave function**. It can be an order of magnitude larger than the de broglie wavelength of electrons having the same energy.

BONDING AREA

The area, defined by the extent of a metallization land or the top surface of a terminal, to which a lead is or is to be bonded.

BONDING PAD

A metallized area to which an electrical connection is to be made. It is also called a bonding island or a controlled collapse chip connection.

BONDING WIRE

Fine wire for making electrical connections in hybrid circuits between various bonding pads on the semiconductor device substrate and device terminals or substrate lands.

BREAKDOWN

A sudden change from high dynamic electrical resistance to a very low dynamic resistance in a reverse biased semiconductor device, e.g., a reverse biased junction between p-type and n-type semiconductor materials, wherein reverse current increases rapidly for a small increase in reverse applied voltage, and the device behaves as if it had negative electrical resistance.

BREAKDOWN POINT/VOLTAGE

The voltage value at which breakdown occurs.

BREAKOVER

The start of current flow in a silicon controlled rectifier.

BUCKET BRIGADE DEVICE

A charge transfer device in which only a portion of the charge carriers (electrons or holes) at each storage site are transferred to the next storage site.

BUMP CONTACT

A term used to describe, typically, solder bumps on a chip or substrate which are found on only one side of the chip or substrate as, for example, on a flip-chip.

BULK-CHANNEL CCD

A charge coupled device in which charge is stored and transferred below the surface of the device.

BULK-EFFECT DEVICE

An active solid-state device made up of a semiconductor material whose electrical characteristics and electronic properties are exhibited throughout the entire body of the material, rather than in just a localized region thereof, e.g., the surface.

BURIED CHANNEL CCD

See BULK-CHANNEL CCD.

CB JUNCTION

The collector-base junction of a bipolar transistor.

CAPACITOR

A component used in electrical and electronic circuits which stores a charge of electricity, usually for very brief periods of time, with the ability to rapidly charge and discharge. A capacitor is usually considered a passive component since it does not rectify, amplify, or switch and because charge carriers do not undergo energy level changes therein, although some active solid-state devices function as voltage variable capacitors.

CARRIER

A mobile free electron or hole.

CARRIER CONCENTRATION

The number of electrical charge carriers in a given volume, usually a cubic centimeter, of semiconductor material.

CELL

An individual integrated circuit element located on a large, or master chip of, semiconductor material.

CHANNEL

A path for conducting current between a source and drain of a field effect transistor.

CHANNEL LENGTH EFFECTS

Operating characteristics of FETs which depend on the length (distance between source and drain) of the channel regions. Such effects include switching speed change and threshold voltage change with channel length change.

CHANNEL WIDTH EFFECTS

Operating characteristics of FETs which depend on the width (horizontal distance perpendicular to channel length and parallel to upper surface of device) of the channel. Such effects include conductance and threshold voltage change with channel width change.

CHANNEL STOP

Means for limiting channel formation in a semiconductor device by surrounding the affected area with a ring of highly doped, low resistivity semiconductor material. In a field effect transistor, it is a region of highly doped material of the same type as the lightly doped substrate used to prevent leakage paths along the chip surface from developing. Also referred to as "chanstop."

CHANNEL PINCH-OFF REGION

The location in a current channel portion of a field effect transistor (FET) where the current is reduced to a minimum value due to its diameter being reduced to a minimum.

CHARACTERISTIC CURVE

A graph showing the relationship between two or more changing parameters, e.g., current and voltage of an electronic device.

CHARGE CARRIER

A mobile conduction electron or hole in a semiconductor.

CHARGE CONFINEMENT

Restriction of electrical charge carriers, e.g., electrons or holes, to specified locations, e.g., by quantum wells, gate electrode potentials, etc.

CHARGE-COUPLED DEVICE

A charge transfer device in which all carriers (electrons or holes) are transferred from one storage site to the next upon application of a shifting voltage.

CHARGE INJECTION DEVICE

A field effect device in which storage sites for packets

of electric charge are induced at or below the surface of an active solid-state device by an electric field applied to the device and wherein carrier potential energy per unit charge minima are established at a given storage site and such charge packets are injected into the device substrate or into a data bus. This type device differs from a charge transfer device in that, in the latter, charge is transferred to adjacent charge storage sites in a serial manner, whereas, in a charge injection device, the charge is injected in a non-serial manner to the device substrate or to a data bus.

CHARGE TRANSFER DEVICE

A semiconductor device in which discrete packets of electrical charge are transferred from one location to another. Examples of charge transfer devices include charge-coupled devices (CCDs) and bucket-brigade devices (BBDs).

CHIP

A single crystal substrate of semiconductor material on which one or more active or passive solid-state electronic devices are formed. A chip may contain an integrated circuit. A chip is not normally ready for use until packaged and provided with external connectors.

CHIP CARRIER

A package with terminals, for solid-state electronic devices, including chips which facilitates handling of the chip during assembly of the chip to other electronic elements.

CHIP COMPONENT

A circuit element (active or passive) for use in microelectronics. Besides integrated circuits, the term includes diodes, transistors, resistors, and capacitors.

CIRCUIT

A number of devices interconnected in a one or more closed paths to perform a desired electrical or electronic function.

CLADDING BARRIER

A higher band gap material which encases a lower band gap material that defines the walls of a quantum well.

CMOS

See COMPLEMENTARY METAL OXIDE SEMICONDUCTOR.

COHERENCE LENGTH

The typical distance an electron can travel before it is scattered (e.g., by a phonon, a defect, or an impurity).

COHERER

A term which encompasses both active and passive type devices, the passive type being a resistor whose resistance decreases when subjected to a high frequency signal, and the active type being a rectifier which is made up of active solid-state particles which conduct and rectify current when connected into a cohesive element but which loses that characteristic when the particles are separated (e.g., by shaking a container in which the particles are located).

COLLECTOR

That end region of a bipolar transistor which forms one of the main current regions and which is reverse biased in operation with respect to the base region.

COLLECTOR CURRENT

The current which flows through the terminal of the collector region of a bipolar transistor.

COLLECTOR DIFFUSION ISOLATION (CDI)

An electrical isolation technology used for bipolar devices which employs an epitaxial layer, which forms transistor base regions, laid on a substrate of the same conductivity type (p or n) as the epitaxial layer, with an opposite conductivity type region, more heavily doped than the epitaxial base layer and located between the layer and the substrate, forming the collector and isolating the transistor from the substrate.

COMMON-BASE CONFIGURATION

A bipolar transistor in which the base region is common to both the input and output circuit. This is also known as a grounded-base bipolar transistor circuit.

COMMON-COLLECTOR CONFIGURATION

A bipolar transistor in which the collector region is common to both the input and output circuit. It is also known as an emitter-follower bipolar transistor circuit.

COMMON-DRAIN CONFIGURATION

A unipolar transistor in which the drain region is common to both the input and output circuit.

COMMON-EMITTER CONFIGURATION

A bipolar transistor in which the emitter region is common to both the input and output circuit. It is also known as a grounded-emitter bipolar transistor circuit.

COMMON- OR GATE-CONFIGURATION

A unipolar transistor in which the gate region is common to both input and output circuits.

COMPLEMENTARY METAL OXIDE SEMICONDUCTOR (CMOS)

Both n-type and p-type metal oxide semiconductor devices, e.g., transistors, formed on the same substrate.

COMPONENT

An electronic device - active or passive - which has distinct electrical characteristics and has terminals for connection to other components to form a circuit.

COMPOUND

A homogeneous material which has definite proportions of chemically combined atoms or ions.

CONCENTRATION GRADIENT

A difference in dopant concentration (p- or n-type) from one position to another in a semiconductor.

CONDUCTION BAND

A partially filled energy band in which electrons can move freely, permitting a material to carry electric current where electrons are the current carriers.

CONDUCTION ELECTRONS

In a conductor or n-type semiconductor, outer shell electrons that are bound so loosely that they can move freely in the conduction band of a solid material under the influence of an electric field.

CONDUCTIVITY

The ability of a material to conduct electric current. Its converse is resistivity.

CONDUCTOR

A material which offers comparatively little resistance to the flow of current.

CONDUCTOR SPACING

The distance between adjacent edges (not centerline to centerline) of isolated conductive patterns in a conductor layer.

CONNECTOR AREA

That portion of metallized conductors used for providing external electrical connections from a component to a chip or other component.

CONTACT

The parts of a conductor designed to touch or be touched by other such parts of an electrical conductor to carry current to or from the conductor.

CONTACT WINDOW

An opening in an insulating layer to expose an underlying conductor to permit electrical contact thereto. It is also called a via hole.

COVALENT BONDING

The sharing of electrons by atoms in which each atom contributes one of a pair of electrons shared by another atom and forming a bond between those two atoms.

CRYOSAR

An active solid-state device which operates at cryogenic temperatures, i.e., at temperatures at or below 77 degrees Kelvin, by avalanche breakdown caused by impact ionization of device impurities.

CRYSTAL

A solid substance whose atoms are arranged with periodic geometric regularity, called a lattice.

CRYSTAL DEFECT

Any nonuniformity in a crystal lattice. There are four

categories of crystal defects: (1) point defects, (2) line defects, (3) area defects, and (4) volume defects. Point defects include any foreign atom at a regular lattice site (substitutional site) or between lattice sites (interstitial site), anti-site defects in compound semiconductors, e.g., Ga in As or As in Ga, missing lattice atoms, and host atoms located between lattice sites and adjacent to a vacant site (Frenkel defects). Line defects, also called edge dislocations, include extra planes of atoms in a lattice. Area defects include twins or twinning (a change in crystal orientation across a lattice) and grain boundaries (a transition between crystals having no particular positional orientation to one another. Volume defects include precipitates of impurity or dopant atoms caused by volume mismatch between a host lattice and precipitates.

CUTOFF

A minimum value of voltage or current applied to an active device which stops the device from operating in a particular manner.

DE BROGLIE WAVELENGTH

The wavelength of a particle, based on L.V. de Broglie's theory that particles exhibit wavelike characteristics.

DEEP DEPLETION

The condition in which a depletion layer formed in a MOS active device due to voltage applied to the gate electrode of the device, is deeper than the maximum depth at which inversion would normally be expected to occur at room temperature in a semiconductor device at the surface closest to the gate electrode, without formation of an inversion layer.

DEEP GROOVE ISOLATION

Electrical isolation of adjacent devices in a single monolithic semiconductor chip by grooves extending deeply into and below the surface of the chip between the devices.

DEEP-LEVEL CENTERS

Energy levels that can act as traps located in the forbidden band of a semiconductor material that are not near the conduction or valence band edges.

DEGENERATION

Doping of a semiconductor to such an extent that the Fermi level lies within the conduction band (N+ semiconductor) or within the valence band (P+ semiconductor). Also, in circuit applications, negative feedback between two or more active solid-state devices.

DEPLETION LAYER

See DEPLETION REGION.

DEPLETION MODE

The operation of a field-effect transistor having appreciable channel conductivity for zero gate- source voltage and whose channel conductivity may be increased or decreased according to the polarity of the applied gate-source voltage, by changing the gate-to-source voltage from zero to a finite value, resulting in a decrease in the magnitude of the drain current.

DEPLETION REGION

The region extending on both sides of a reverse biased semiconductor junction in which free carriers are removed from the vicinity of the junction. It is also called a space charge region, a barrier region, or an intrinsic semiconductor region.

DEVICE (ACTIVE)

The physical realization of an individual electrical element in a physically independent body which cannot be further divided without destroying its stated function. Examples are transistors, pnpn structures, and tunnel diodes.

DIE

A tiny piece of semiconductor material, separated from a semiconductor slice, on which one or more active electronic components are formed. Sometimes called a chip.

DIE BOND

Attachment of a semiconductor chip to a substrate or chip carrier or package, usually with an epoxy, eutectic, or solder alloy.

DIFFUSED JUNCTION

A junction between two different conductivity regions within a semiconductor and which is formed by diffusion of appropriate impurity atoms into the material.

DIFFUSED TRANSISTOR

A transistor in which the emitter and collector junctions are formed by diffusion of dopant atoms into the semiconductor material.

DIFFUSION

(1) The movement of carriers from a region of concentration to one of lower concentration; (2) a process of adding impurities to a semiconductor material to change its electrical characteristics.

DIFFUSION BARRIER

An obstacle to the diffusion of charge carriers in an active solid-state device.

DIFFUSION CURRENT

Current caused by charge carriers diffusing from a volume of high carrier concentration to a volume of lower carrier concentration in a solid-state material.

DIFFUSION LENGTH

In a homogeneous semiconductor material, the average distance minority carriers move during their lifetime (i.e., between generation and recombination).

DIODE

An electronic device which has two terminals and an asymmetrical or nonlinear voltage-current characteristic.

DIODE ISOLATION

A technique in which a high electrical resistance between an integrated circuit element and its substrate is achieved by surrounding the element with a reverse biased pn junction.

DIP (DUAL-IN-LINE PACKAGE)

A chip carrier or package consisting of a plastic or ceramic body with two rows of vertical leads in which a semiconductor integrated circuit is assembled and sealed. The leads are typically inserted into a circuit board and secured by soldering.

DIRECT BAND GAP SEMICONDUCTOR

A semiconductor material in which an electron transition from the conduction to the valence band, or vice versa, does not require a change in crystal momentum for the electron. Gallium arsenide is a direct band gap semiconductor material.

DISCRETE CIRCUIT

A circuit which has an individual identity and which is fabricated prior to installation, or is separately packaged and is not part of an integrated circuit.

DISLOCATION

A region in a crystal in which the atoms are not arranged in a perfect lattice-like structure. See CRYSTAL DEFECT for examples of crystal defects/dislocations.

DMOSFET

Depletion type metal oxide semiconductor field effect transistor. Such devices are normally in the on condition with no applied gate voltage.

DONOR IMPURITY

An element which when added to a semiconductor provides unbound or free electrons to the semiconductor which may serve as current carriers. Typically, donors are atoms which have more valence electrons than the atoms of the semiconductor material into which they are introduced in small quantities as an impurity or dopant. Since such donor impurities have more valence electrons than the semiconductor, a semiconductor doped with donor impurities is an n-type semiconductor.

DOPANT

An impurity added to a semiconductor material to change its electrical conductivity or other characteristics. N-type (negative) dopants, such as phosphorus, for a group IV semiconductor such as silicon typically come from group V of the periodic table. When added to silicon n-type dopants create a material that contains conduction electrons. P-type (positive) dopants, such as boron, for a group IV semiconductor such as silicon, typically come from group III and result in holes.

DOPING PROFILE

The point to point concentration throughout a semicon-

ductor of an impurity atom doped into the semiconductor.

DOUBLE-DIFFUSED MOS (DMOS)

A metal oxide semiconductor having diffused junctions in which successive diffusions of different impurity types are made in the same well-defined region of the semiconductor.

DRAIN

The electrode of a field effect transistor which receives charge carriers which pass through the transistor channel from the source electrode.

DRAIN CURRENT

The flow of charge carriers in the drain region of a field effect transistor.

DRAIN-SOURCE SATURATION CURRENT

The maximum amount of current carried by the drain of a field-effect transistor when the gate- source voltage equals zero volts.

DRIFT CURRENT

Current produced in a solid-state electronic device by charge carriers (e.g., holes or electrons) drifting in the direction of an applied electric field.

DUAL GUARD-BAND ISOLATION

A type of electrical isolation of functional elements of an integrated circuit comprised of two distinct unused areas of chip surface area adjacent to the elements desired to be electrically isolated.

DUAL-IN-LINE (DIP)

See DIP.

DYNAMIC RANDOM ACCESS MEMORY (DRAM)

solid-state memory in which the information decays over time and needs to be periodically refreshed.

EB JUNCTION

Emitter base junction in a bipolar transistor.

ELECTRON

The negatively charged particle in an atom that orbits the nucleus in specific energy levels.

ELECTRON FLOW

Movement of electrons from a source of negative potential to a positive potential.

ELECTRON-HOLE PAIR

A positive charge carrier (i.e., hole) and a negative charge carrier (i.e., electron) considered together as being created or destroyed as part of one and the same event.

EMITTER

The region of a bipolar junction transistor from which charge carriers flow through the emitter-base junction into the base region of the device.

EMITTER CURRENT

The amount of current flowing from the emitter across the emitter-base junction into the base region of the device.

E-MOSFET

Enhancement mode metal oxide semiconductor device. See ENHANCEMENT MODE and MOSFET.

ENERGY LEVELS

The possible energy values that an atom or molecule or subatomic particle (e.g., an electron) can have.

ENHANCEMENT MODE

The operation of a field effect transistor which has a channel formed therein between its source and drain regions and which normally does not conduct current through its channel with zero voltage applied to its gate electrode. Voltage of the correct polarity will accumulate minority carriers in the channel to permit conduction of current in the channel, thus turning on the transistor.

EPITAXY

The growth of a crystal of one substance on the surface of a crystal of the same or another substance so that the

crystal lattice of the base substance controls the orientation of the atoms in the grown crystal.

EPITAXIAL LAYER

An added layer of crystal that takes on the same crystalline orientation as the substrate crystal.

ESAKI DIODE

A heavily doped pn junction diode where conduction occurs through the junction potential barrier due to a quantum mechanical effect even though the carriers which tunnel through the potential barrier do not have enough energy to overcome the potential barrier. Esaki tunneling involves a tunneling barrier formed by a macroscopic depletion layer between n-type and p-type regions. It does not involve a resonant tunneling barrier using controlled quantum confinement, a layer located between junctions, nor a thin superlattice layer.

EXCESS CARRIERS

Charge carriers present in a semiconductor in excess of those present in thermal equilibrium.

EXTRINSIC SEMICONDUCTOR

A semiconductor whose charge carrier concentration and, therefore, electrical properties depend on impurity, atoms introduced therein.

FACE BONDED

A chip mounting technique wherein semiconductor chips are provided with small mounting pads, turned face down, and bonded directly to conductors on a substrate.

FANNED LEADS

Leads placed through a package wall at closer intervals than normal and radiated (fanned) out on the exterior of the package until a desired center-to-center lead spacing is achieved.

FET

Acronym for field effect transistor.

FIELD EFFECT TRANSISTOR

A unipolar transistor in which current carriers are injected at a source terminal and pass to a drain terminal through a channel of semiconductor material whose conductivity depends largely on an electric field applied to the semiconductor from a control electrode. There are two main types of FET, a junction FET and an insulated-gate FET. In the junction FET, the gate is isolated from the channel by a pn junction. In an insulated-gate FET, the gate is isolated from the channel by an insulating layer, so that the gate and channel form a capacitor with the insulating layer as the capacitor dielectric.

FIELD OXIDE

A thin (on a macroscopic scale) film made up of an oxide of a material which overlies a device substrate to reduce parasitic capacitive coupling between conductors overlying the oxide and the substrate or devices below the oxide layer (e.g., in the substrate).

FLAT PACK

An integrated circuit package with leads extending from it in the same plane as that of the package. It has a low profile.

FLIP-CHIP

A term which describes the situation wherein a semiconductor device which has all terminations on one side thereof in the form of bump contacts, has a passivated surface and has been flipped over and attached to a matching substrate.

FLOATING DIFFUSION

A region of a semiconductor device in which impurity atoms have been doped and which is electrically floating, that is, has no direct electrical connection.

FLOATING GATE

A gate electrode that is electrically floating, that is, has no direct electrical connection.

FOOTPRINT

Also called a land pattern. It is a combination of lands used to mount a surface mount component. Metal pads on a substrate surface are arranged in the same pattern as the leads or pads on the component itself.

FORBIDDEN ENERGY BAND/REGION/GAP

The energy band of a material which is located between a solid material's conduction and valence bands. It is

defined by the amount of energy that is needed to release an electron from its valence band to its conduction band. Electrons cannot exist in this gap. They are either below it, and bound to an atom, or above it, and able to move freely.

FORWARD BIAS

An external voltage applied in the conducting direction of a pn junction. A positive potential is connected to the p-type material and a negative potential to the n-type semiconductor material.

FORWARD BREAKOVER POTENTIAL

The value of positive terminal voltage at which a regenerative device (e.g., a silicon controlled rectifier), with its gate circuit open, becomes conductive.

FORWARD CURRENT

The current which flows across a semiconductor junction when a forward bias is applied across the junction.

FOUR-LAYER DIODE

A semiconductor diode with three junctions and only two terminals connected to the outer layers forming the junctions. This includes two terminal pnpn thyristors.

FOUR-PHASE CCD

A charge coupled device having four electrode sets and four gate voltages.

FOUR-SIDE LEAD LAYOUT

The situation wherein there are leads through all four sides of an integrated circuit package.

FRAME TRANSFER CCD

A charge coupled device area imager array with a separate image area, storage area, and read-out register area, the storage area being located between the image area and the readout area. This is distinguished from an interline-transfer CCD in which the sensing and storage/ readout function areas are located next to each other.

FREE ELECTRON

An electron not bound to a particular atom, but free to circulate among the atoms of a solid material.

GAIN

The ratio of the magnitude of the electrical output of a device to the magnitude of its electrical input.

GALLIUM ARSENIDE

A semiconducting chemical compound which is often used in active solid-state devices.

GATE

The control electrode or region of a field effect transistor, located between the source and drain electrodes, and regions thereof.

GATE ARRAY

A repeating geometric arrangement of groups of active solid-state devices, each group being connectable into a logic circuit, in one integrated, monolithic semiconductor chip.

GATE CHARGE

The electrical charge on a gate electrode.

GATE CONTROLLED DIODE

A three terminal semiconductor diode with the ability to be turned on or off by a pulse applied to its gate electrode.

GATE TRIGGER CURRENT

The amount of current needed to commence gate current flow in a four layer semiconductor device (e.g., a thyristor).

GATE TRIGGER VOLTAGE

The amount of voltage needed to begin gate current flow in a four layer semiconductor device (e.g., a silicon controlled rectifier).

GERMANIUM

A semiconductor material used in active solid-state devices.

GULL-WING

The name given to lead configurations of some surface

mounted devices. Gull wings extend from the side of a component package and have an L-shaped bend at component ends, which extend down to the substrate surface and away from the component.

GUNN DIODE

A diode in which electrons under the influence of sufficiently high electric fields are transferred between energy valleys of different momentum in the conduction band of the active semiconductor device material or holes under the influence of sufficiently high electric fields are transferred between energy valleys of different momentum in the valence band of the active semiconductor device material. A Gunn diode does not normally have a pn junction and cannot be used as a rectifier.

GUNN EFFECT

An inter valley transfer effect wherein electrons under the influence of sufficiently high electric fields are transferred between energy valleys of different momentum in the conduction band of the active semiconductor device material, or holes under the influence of sufficiently high electric fields are transferred between energy valleys of different momentum in the valence band of the active semiconductor device material.

HALL EFFECT DEVICE

An active solid-state device in which a current is flowing and is in a magnetic field perpendicular to the current, and in which a voltage is produced that is perpendicular to both the current flow direction and the magnetic field direction.

HALOGENS

F, Cl, Br, I, At.

HEADER

A slab-like or flat plug-in base for a package that is designed to be used with a cover or lid.

HEAT SINK

Devices used to absorb or transfer heat away from heat sensitive devices or device components.

HEAVY METALS

Metals other than light metals - see LIGHT METALS.

HETEROJUNCTION /HETEROINTERFACE

An interface between two dissimilar semiconductor materials. For example, one material may by InAs and the other may be InAlAs, or one material may be GaAs and the other material may be GaAlAs.

HETEROSTRUCTURE

See HETEROJUNCTION.

HIGH ELECTRON (HOLE) MOBILITY TRANSISTOR (HEMT)

A heterojunction field effect transistor with impurity ions located on the side of the hetero junction with lower affinity for the charge carriers (holes <u>or</u> electrons) injected at the source that pass to the drain via a channel adjacent the hetero junction.

HOLDING CURRENT

The minimum current needed to maintain a generative type active solid-state device (e.g., a thyristor) in an “on” or conducting condition.

HOLE

An empty energy level in the valence band of a semiconductor crystal which exhibits properties of a real particle and can act as a mobile positive charge carrier.

HOLE FLOW

The current in a semiconductor material due to the movement of holes therein.

HOMOJUNCTION

An interface between regions of opposite polarity in the same semiconductor material.

HOT CARRIER DIODE

A diode in which electrons (or holes) have energies greater than those that are in thermal equilibrium with the material of at least one of the regions forming the diode. Schottky barrier diodes typically have “hot carriers” (hot electrons) injected into the metal from the semiconductor.

HOT ELECTRONS

See HOT CARRIER DIODE.

HYBRID CIRCUIT

A small printed circuit having miniature components, which may include passive components (resistors, capacitors, and inductors, deposited on a printed circuit board. A "hybrid circuit" is NOT an integrated circuit, and is not classifiable in this class.

IMPURITY

A foreign material present in a semiconductor crystal, such as boron or arsenic in silicon, which is added to the semiconductor to produce either p-type or n-type semiconductor material, or to otherwise result in material whose electrical characteristics depend on the impurity dopant atoms.

INDIRECT BAND GAP SEMICONDUCTOR

A semiconductor material in which a change in semiconductor crystal momentum for an electron is required when it moves from the conduction band to the valence band and vice versa. Silicon is an indirect band gap semiconductor.

INSULATED-GATE FIELD EFFECT TRANSISTOR (IGFET)

A unipolar transistor with source, gate, and drain regions and electrodes, in which conduction takes place in a channel controlled by action of the voltage applied to the gate electrode of the device, in which the gate electrode is separated from the channel by an insulator layer.

INSULATOR

A material which has a high resistance to the flow of electric current. It has such low electrical conductivity that the flow of current therethrough can usually be neglected.

INTEGRATED CIRCUIT

See MONOLITHIC DEVICE (e.g., IC) as contrasted to HYBRID CIRCUIT.

INTRINSIC CONCENTRATION

The number of minority carriers in a semiconductor due to thermal generation of electron-hole pairs.

INTRINSIC SEMICONDUCTOR

A pure semiconductor, i.e., one with no impurity atoms introduced therein.

INVERSION

A condition in a semiconductor material in which the concentration of minority carriers exceeds the concentration of majority carriers.

INVERSION LAYER/CHANNEL

A region in a semiconductor material in which the concentration of minority carriers exceeds the concentration of majority carriers.

IRON GROUP METALS

Fe, Co, Ni.

ISOLATION

Prevention of the flow of electric current between electronic component parts of a solid-state electronic device.

ISOPLANAR CMOS

A semiconductor device in which relatively thick regions of silicon dioxide, recessed into the semiconductor surface, are used to electrically isolate device areas and prevent parasitic device formation. More commonly called LOCOS CMOS.

ISOPLANAR ISOLATION

A type of electric isolation in which relatively thick regions of silicon dioxide, recessed into the semiconductor surface, are used to electrically isolate device areas and prevent parasitic device formation. More commonly called LOCOS ISOLATION.

J-LEAD

A rolled-under, J-shaped configuration of some surface mounted component leads.

JUNCTION

A joining of two different semiconductors or of a semiconductor and a metal at an interface. Types of junctions include HETEROJUNCTIONS, SCHOTTKY BARRIER JUNCTIONS, and PN JUNCTIONS.

JUNCTION BARRIER

The opposition to the diffusion of majority carriers across a pn junction due to the charge of the fixed donor and acceptor ions.

JUNCTION CAPACITANCE

The capacitance across a pn junction. It depends on the width of the depletion layer, which increases with increased reverse bias voltage across the junction.

JUNCTION GATE FIELD EFFECT TRANSISTOR (JFET)

See FIELD EFFECT TRANSISTOR.

JUNCTION ISOLATION

Electrical isolation of devices on a monolithic integrated circuit chip using a reverse biased junction diode to establish a depletion layer that forms the electrical isolation between devices.

JUNCTION RESISTANCE

The electrical resistance across a semiconductor PN junction.

LAND

The conductive areas, normally metal patterns, on a semiconductor integrated circuit, which form part of the contacts and interconnections between components on the integrated circuit.

LAND PATTERN

A combination of lands on an integrated circuit.

LANTHANIDE ELEMENTS

La, Ce, Pr, Nd, Pm, Sm, Eu, Gd, Tb, Dy, Ho,Er, Tm, Yb, Lu.

LATCHING/LATCHED/LATCHUP

The state or condition of a regenerative feedback device, e.g., a thyristor, in which the device remains ON when the initializing signal is removed.

LCCC

An abbreviation for a leadless ceramic chip carrier which is a hermetically-sealable ceramic package in which an integrated chip can be placed to create a surface mounted component. It has pads around its perimeter for connection to a substrate.

LEAD

The conductor brought out from a component.

LEAD FRAME

A metal frame which provides support for an integrated circuit chip or die as well as electrical leads to interconnect the integrated circuit on the die or chip to other electrical components or contacts.

LEAKAGE CURRENT

Unwanted current flow.

LIFETIME

The average time interval between the introduction of and recombination of minority charge carriers in a semiconductor.

LIGHT EMITTING DIODE (LED)

Junction diodes which give off light when energized.

LIGHT METALS

Alkali metals, alkaline-earth metals, Be, Al, Mg.

LINE DEFECT

A planar crystal defect (e.g., an extra plane of atoms in a crystal). It is also called an edge dislocation.

LOCAL OXIDE CMOS (LOCMOS)

Local oxide complementary metal oxide semiconductor structure which features oxide isolation which is recessed into the semiconductor surface.

LOCOS

(Local Oxidation of Silicon) Patterns of oxide isolation which are recessed into the semiconductor surface. Sometimes also called isoplanar, ROX (Recessed Oxide Isolation), or planox.

LUMINESCENCE

Emission of light by directly converting some other type of energy. Types include thermoluminescence, photoluminescence, cathodoluminescence, and electroluminescence. It includes fluorescence and phosphorescence. Active solid-state luminescent devices are semiconductors which operate via injection luminescence. Active devices include pn junctions (including heterojunctions), Schottky barrier junctions, metal-insulator-semiconductor (MIS) structures, and high speed traveling domains, e.g., Gunn domain and acoustoelectric wave generated domains; whereas passive solid-state electroluminescent devices (phosphors) are insulators which operate in an intrinsic luminescence phenomena, i.e., where an applied electric field generates free carriers (there being no free carriers in an insulator to be accelerated by an applied field unless the field also generates them) to initiate the light emission mechanism.

MAJORITY CARRIER

The predominant charge carrier in a semiconductor. Electrons are majority carriers in n-type semiconductors. Holes are majority carriers in p-type semiconductors.

MAJORITY CURRENT

Current caused by the flow of majority carriers.

MASTERSLICE ARRAY/MASTERCHIP

A substrate that contains active and passive electronic components in a predetermined pattern which may be connected into different logic or analog circuits.

MBM JUNCTION

Active solid-state devices having metal-barrier-metal layer junctions.

METAL-OXIDE SEMICONDUCTOR FIELD EFFECT TRANSISTOR (MOSFET)

See INSULATED GATE FIELD EFFECT TRANSISTOR.

METAL-GATE FET

A field effect transistor having a gate conductor made of metal, rather than polycrystalline semiconductor material.

METALLIZATION

A single or multilayer film pattern of electrically conductive material deposited on a substrate to interconnect electronic components, or the metal film on the bonding area of a substrate which becomes part of the bond and performs both an electrical and a mechanical function.

METALS

Elements other than non-metals. See NON-METALS.

MIM DIODE

A junction diode with a thin insulating layer of material sandwiched between two metallic surface layers which operates as a tunneling (direct or Fowler-Nordheim type) diode.

MINORITY CARRIER

The less predominant charge carrier in a semiconductor. In a p-type semiconductor, minority carriers are electrons, whereas in n-type semiconductor material, minority carriers are holes.

MINORITY CURRENT

The current caused by flowing minority carriers.

MIS

Acronym for metal-insulator-semiconductor. Typically active solid-state devices with MIS technology have a silicon dioxide layer formed on a single crystal silicon substrate. A polysilicon conductor layer is formed on the oxide.

MOBILITY

The facility with which carriers move through a semiconductor when subjected to an applied electric field. Electrons and holes typically have different mobilities in the same semiconductor.

MODFET

Acronym for a modulation doped field effect transistor. A high speed semiconductor FET in which dopant atom containing semiconductor layers alternate with non-doped semiconductor layers, so that the carriers (electrons or holes) resulting from the dopant atoms can travel in the undoped material, so that there is little scat-

tering of carriers from dopant atoms. Typically, the dopant atoms are in semiconductor material having a lower carrier affinity than the undoped layers, to facilitate carrier spill over into the undoped layers. Such a structure may typically constitute a superlattice. See also HIGH ELECTRON MOBILITY TRANSISTOR (HEMT).

MODULATION DOPING

Spatial modulation of dopant atoms in a semiconductor crystal.

MONOLITHIC DEVICE (E.G., IC)

A device in which all components are fabricated on a single chip of silicon. Interconnections among components are provided by means of metallization patterns on the surface of the chip structure, and the individual parts are not separable from the complete circuit. External connecting wires are taken out to terminal pins or leads.

MSM

Acronym for metal-semiconductor-metal semiconductors. Active solid-state semiconductor devices having a semiconductor layer sandwiched between two layers of metal.

MULTILAYER METALLIZATION

Two or more layers of interconnecting metallization patterns in a monolithic integrated circuit separated by insulator material except in interconnection areas.

N-TYPE SEMICONDUCTOR

An extrinsic semiconductor in which electron density exceeds hole density.

NDM

Negative differential mobility (e.g., Gunn effect) intervalley active semiconductor devices wherein an applied electric field imparts energy to electrons or holes to permit them to jump to higher quantum electronic intervalley energy levels in which electrons have lowered electron mobility.

NEGATIVE RESISTANCE REGION

An operating region of an active solid-state electronic device in which an increase in applied voltage results in a decrease in output current.

NEGATIVE TEMPERATURE COEFFICIENT

The amount of reduction in a device parameter, such as capacitance or resistance, for each degree of device operating temperature.

NMOS

N-channel metal oxide semiconductor devices which use electrons as majority carriers.

NOBLE GASES

He, Ne, Ar, Kr, Xe, Rn.

NON-METALS

H, B, C, Si, N, P, O, S, Se, Te, noble gases, halogens.

NPN TRANSISTOR

A transistor in which the base is made of p-type material and both source and drain are made of n-type semiconductor material.

N-CHANNEL FET

A field effect transistor that has an n-type conduction channel.

N-TYPE SEMICONDUCTOR

An extrinsic semiconductor having n-type dopant atoms, e.g., atoms with one more valence electron than the host atoms.

ORGANIC SEMICONDUCTOR

A semiconductor compound in which the molecule is characterized by two or more carbon atoms bonded together, one atom of carbon bonded to at least one atom of hydrogen or halogen (i.e., chlorine, fluorine, bromine, iodine) or one atom of carbon bonded to at least one atom of nitrogen by a single or double bond.

(1) Note. Exceptions to this rule include HCN, CN-CN, HNCO, HNCS, cyanogen halides, cyanamide, fulminic acid, and metal carbides. These are not regarded as organic semiconductor materials. Also, note that graphite and diamond are not regarded as organic semiconductors since they are not

compounds; silicon carbide is not regarded as organic.

OXIDE ISOLATION

Electrical isolation of semiconductor electronic devices in a monolithic integrated circuit by an oxide (e.g., silicon oxide).

PACKAGE

A container, case, or enclosure for protecting a solid-state electronic device from the environment.

PAD

(1) The portion of a conductive pattern on a solid-state electronic device for making external connection thereto; (2) the portion of a conductive pattern on a chip or a printed circuit board designed for mounting or attaching a substrate or solid-state active electronic device.

PARASITIC CURRENT

Unintended current which flows between devices in an integrated circuit, or which flows between device regions and isolation regions.

PARASITIC DEVICES/CHANNELS

Junctions forming unintended active solid-state devices which interconnect intended active solid-state devices, which unintended devices are not designed to carry current flow.

PARASITIC THYRISTOR ACTION

Unwanted active solid-state device formation in which four adjacent complementary doped regions not designed to act as an active solid-state device, lack sufficient isolation therebetween and act as a thyristor. Parasitic thyristor action is typically a problem encountered in CMOS integrated circuits.

PARASITIC TRANSISTOR ACTION

Unwanted transistor formation in an integrated circuit structure.

PASSIVE DEVICE

A solid-state electronic device or component in which charge carriers do not change their energy levels and that does not provide rectification, amplification, or switching, but which does react to voltage and current. Examples are pure resistors, capacitors, and inductors.

P-CHANNEL

A conduction path, made of p-type semiconductor material, located between the source and drain of a field effect device.

PERISTALTIC CCD

See BULK CHANNEL CCD.

PERMISSIBLE ENERGY LEVEL

An energy level in a conduction or valence band which a charge carrier (electron or hole) may have.

PHOTODIODE

A diode in which charge carriers are created by light which illuminates the diode junction. It is a photovoltaic as well as a photoconductive device.

PHOTOTRANSISTOR

A transistor having no base terminal and in which charge carriers are created by light which illuminates its collector-base junction.

PHOTOVOLTAIC CELL

An active solid-state device with a pn junction that generates a voltage in response to light impinging on the junction.

PINCH-EFFECT RESISTOR

A monolithic integrated circuit resistor having a layer of one conductivity type, typically a P-layer formed at the same time as integrated circuit bipolar transistor base regions, which is thinned by an inset region of opposite conductivity type, typically an N-layer formed at the same time as integrated circuit bipolar transistor emitter regions.

PINCH-OFF

The condition in a depletion mode field effect transistor wherein the conducting channel is depleted of majority carriers and is thereby pinched off, no path remaining for the source-to-drain majority carrier (e.g., electron) flow.

PIN DIODE/DEVICE

A diode having an intrinsic semiconductor (i.e., one with no dopants) sandwiched between a p-type layer and an n-type layer. The depletion region (the intrinsic semiconductor layer) thickness can be tailored to optimize quantum efficiency for use as a photo diode or frequency response for use as a microwave diode.

PIN-GRID ARRAY

A semiconductor chip package having leads in the form of pins arranged in columns and rows.

PLANAR TRANSISTOR

A bipolar transistor in which the emitter base and collector regions terminate at the same plane surface without indentations in or protrusions from the surface. Hence, the emitter and base regions form dish shaped portions extending into the semiconductor from the common surface.

PLUG-IN PACKAGE

An electronic package for an active solid-state device in which the lead pins are perpendicular to the mounting area of the substrate, as contrasted with a flat package in which the leads are in the same plane as the substrate.

P-MOSFET

A metal oxide semiconductor field effect transistor having p-type source and drain regions and a p-type conduction channel which may be formed by a p type doped region (depletion mode) or induced by a voltage on the gate (enhancement mode).

PN-JUNCTION

The interface and region of transition between p-type and n-type semiconductors.

PN-JUNCTION DIODE

A semiconductor device having two terminals connected to opposite type semiconductor materials with a junction therebetween and exhibiting a non-linear voltage-current characteristic, usually used for switching or rectification.

PNP TRANSISTOR

A bipolar transistor with a p type emitter, an n-type base and a p-type collector.

POINT DEFECT

A crystal defect occurring at a point in a crystal. Examples include, (1) a foreign atom incorporated into the crystal lattice at either a substitutional (regular lattice) site or interstitial (between regular lattice sites) site, (2) a missing atom in the lattice, or (3) a host atom located between regular lattice sites and adjacent to a vacancy (called a Frenkel defect).

POLYCRYSTALLINE

A material composed of more than one crystal.

POLYSILICON

A polycrystalline form of silicon.

POSITIVE CARRIER

A charge carrier which has a net positive charge (e.g., a hole).

POSITIVE IONS

Atoms which are missing a valence shell electron.

POTENTIAL BARRIER

The difference in electrical potential across a pn junction in a semiconductor.

POTENTIAL HILL

See POTENTIAL BARRIER.

POTTING

An embedding process in which an electronic component is placed in a can, shell, or other container and buried in a liquid dielectric polymer which subsequently changes to a solid material. The container is not removed from the finished part, and a release agent is not used. This process differs from casting - which involves a removable mold.

PRINTED CIRCUIT BOARD

A structure formed on one or more layers of electrically insulating material having electrical terminals and con-

ductive material deposited thereon, in continuous paths, from terminal to terminal, to form circuits for electronic apparatus such as chips or substrates.

P-TYPE CONDUCTIVITY

Electrical conductivity associated with positive charge carriers (holes) in a semiconductor material.

P-TYPE SEMICONDUCTOR

An extrinsic semiconductor in which the hole density exceeds the conduction electron density.

PUNCHTHROUGH

Expansion of a depletion region* from one junction to another junction in an active solid-state device.

PURPLE PLAGUE

A brittle, inter metallic electrically conductive compound which has a purplish color and is formed when aluminum and gold, used as electrical contact materials in semiconductor electronic devices, contact each other and interact. It is usually considered undesirable because it breaks easily, reduces device reliability, and lowers product yield.

QUANTIZED STATES

Discrete energy levels due to the quantum mechanical properties of a material.

QUANTUM TRANSISTOR

Transistors whose operation is based on the properties of electrons confined in quantum wells - semiconductor films only a hundred or so angstroms thick sandwiched between high confining walls made of a second semiconductor material.

QUANTUM WELL

Semiconductor films only a hundred or so angstroms thick sandwiched between high confining walls made of a second material.

RARE EARTHS

Sc, Y, Lanthanides.

READ-OUT REGISTER

Gated semiconductor devices which receive and accumulate charges and make them available to an output device.

RECOMBINATION

The process by which excess holes and electrons in a semiconductor crystal recombine and and no longer function as charge carriers in the semiconductor. Basic recombination processes are band-to-band recombination which occurs when an electron in the conduction band recombines with a hole in the valence band, and trapping recombination which occurs when an electron or hole is captured by a deep energy level, such as produced by a deep level dopant, before recombining with an opposite conductivity type carrier.

REFRACTORY METALS

Ti, V, Cr, Zr, Nb, Mo, Hf, Ta, W.

RESISTIVITY

A measure of the resistance of a material to electric current. Resistivity is a bulk material property, measured in ohm-cm.

RESONANT TUNNELLING DEVICE

A device that works on the principle of resonant electron (or hole) tunneling through a pair of matched potential barriers. This occurs when the energy of the electrons (or holes) matches that of a quantum energy level in the quantum well formed between the barriers.

REVERSE BIAS

A voltage applied across a semiconductor junction in the reverse direction, i.e., wherein a positive potential is connected to the n-type semiconductor and a negative potential is applied to the p-type semiconductor.

REVERSE BREAKDOWN VOLTAGE

The reverse bias voltage value at which electrical resistance drops appreciably and operating current sharply increases.

REVERSE CURRENT

The current flowing through a rectifying junction with a reverse voltage thereacross.

SATURATION

The current between the base and collector of a bipolar transistor when an increase in emitter to base voltage causes no further increase in the collector current.

SCATTERING CENTERS

The impurities (dopants) in semiconductors that cause electrons or holes flowing through the semiconductor to scatter. These reduce carrier mobility and represent a problem in quantum devices because they affect electron coherence length.

SCHOTTKY BARRIER

A metal to semiconductor interface in which the carrier affinity and doping level of the semiconductor are such that a rectifying junction is formed. Usually, minority carriers in the semiconductor do not significantly contribute to the current flowing in a device with such a barrier.

SCHOTTKY DIODE

A diode with a Schottky barrier.

SEMICONDUCTOR

A material whose electrical resistivity is between that of insulators and conductors. The resistivity is commonly changed by light, heat, electric, or magnetic fields incident on the material. Current flow is achieved by transfer of positive holes as well as by movement of electrons.

SEMICONDUCTOR DEVICE

A device in which current conduction takes place within a semiconductor.

SEMICONDUCTOR LASER

A light emitting diode that uses stimulated emission of radiation to produce coherent light output.

SILICON BILATERAL SWITCH (SBS)

A silicon controlled switch that can conduct current in both directions.

SILICON CONTROLLED RECTIFIER (SCR)

A four layer pnpn device that, when in a normal state, blocks applied voltage in either direction. Application of a correct voltage to a gate terminal permits the device to conduct in a forward direction.

SILICON CONTROLLED SWITCH (SCS)

A four layer pnpn semiconductor switching device that can be triggered into conduction by applying either positive or negative pulses.

SILICON-GATE FET

A field effect transistor which has a gate electrode made of silicon.

SILICON ON INSULATOR (SOI)

A semiconductor structure using an insulating substrate, instead of silicon as a substrate material, with an overlying active layer of single crystal silicon containing active solid-state devices. The substrate may typically be of the form of an insulating layer which is itself formed on a single crystal substrate.

SILICON ON SAPPHIRE (S0S) CMOS

A complementary metal oxide semiconductor device (e.g., a transistor) wherein single crystal silicon is grown on a passive insulating base of sapphire (single crystal alpha phase aluminum oxide) with complementary MOS transistors formed in the silicon in one or more island portions.

SILICON TRANSISTOR

A transistor which uses silicon as the semiconductor material.

SINGLE-IN-LINE PACKAGE

A plug-in semiconductor device package with one row of pins with specified spacings therebetween.

SINGLE CRYSTAL

A body of material having atoms regularly located at periodic lattice sites throughout.

SINKER

A buried electrically conductive, low resistance path in an integrated circuit which connects an electrical con-

tact to a conductive region buried in the integrated circuit. It may be made up of a heavily doped impurity region.

SIS

An MIS structure (Metal-Insulator-Semiconductor) in which the "metal" layer is made of semiconductor material, typically polycrystalline silicon.

SOLAR CELL

A photovoltaic cell in the form of a semiconductor diode, usually made of silicon, that generates electricity directly from sunlight impingent on the cell.

SOLID-STATE DEVICE

An electronic device or component that uses current flow through solid (as opposed to liquid), gas, or vacuum materials. solid-state devices may be active or passive.

SOURCE

In a field effect transistor, the electrode to which the source of charge carriers is connected.

SPACE CHARGE REGION

The region around a pn junction in which holes and electrons recombine to leave no mobile charge carriers and a net charge density due to the residual dopant ions.

STEP RECOVERY DIODE

A pn junction active solid-state device in which a forward bias voltage injects charge carriers across the junction but prior to recombination of the carriers, a reverse voltage is applied to return the charge carriers to their source as a group.

SUBSTRATE

The supporting material on or in which the components of an integrated circuit are fabricated or attached.

SUBSTRATE BIAS

The electric potential applied to a substrate, which typically serves as the reference potential against which other voltages are measured. Also, in a MISFET, a voltage applied to the substrate with respect to the source region.

SUPERLATTICE

A periodic sequence of variations in carrier potential energy in a semiconductor, of such magnitude and spacing that the current carrier wave function is spread out over many periods, so that carrier energy and other properties are determined in part by the periodic variations. The variation may be in chemical composition of the material, as in a sequence of heterojunctions, or in impurity concentration, forming a doping superlattice, or both.

SURFACE-CHANNEL CCD

A charge coupled device in which charge resides at the semiconductor surface.

SURFACE MOUNT DEVICES

Active or passive solid-state devices which are structured and configured to be mounted directly to a printed circuit board surface. This type of mounting is distinguished from "through-hole" mounting which involves the electrical and physical connection of devices to a printed circuit board using drilled and plated holes through the conductive pattern of the board.

SURFACE RESISTIVITY

The resistance of a material between two opposite sides of a unit square of its surface. Also called Sheet Resistance. Measured in ohms, often written as "ohms per square" in this case.

TEST PROBES

Mechanical points of contact used for electrical measurement.

THERMISTOR

A semiconductor device whose electrical resistance varies with temperature. Its temperature coefficient of resistance is high, nonlinear, and usually negative.

THICK-FILM DEVICES

Printed thin-film circuits. Silk screen printing techniques are used to make the desired circuit patterns on a ceramic substrate. Active devices may be added thereto as separate devices (see HYBRID CIRCUIT).

THIN-FILM DEVICES

solid-state electronic devices which are constructed by depositing films of conducting material on the surface of electrically insulating bases.

THYRISTOR

A four layer p-n-p-n bistable switching device that changes from an off or blocking state to an on or conducting state which uses both electron and hole type carrier transport.

THRESHOLD VOLTAGE

The voltage at which a pn junction begins to conduct current.

THROUGH-HOLE MOUNTING

The electrical and physical connection of components to the surface of a conductive pattern using drilled and plated holes through the conductive and insulating layers of a printed circuit board.

TRANSFERRED ELECTRON DEVICE

See GUNN EFFECT. In such devices, advantage is taken of the negative differential mobility of electrons or holes in certain semiconducting compounds, particularly GaAs or InP.

TRANSISTOR

An active solid-state semiconductor device having three or more electrodes in which the current flowing between two specified electrodes is modulated by the voltage or current applied to one or more specified electrodes, and is capable of performing switching or amplification.

TRANSITION ELEMENTS

Sc, Ti, V, Cr, Mn, Fe, Co, Ni, Cu, Zn, Y, Zr, Nb, Mo, Te, Ru, Rh, Pd, Ag, Cd, La, Ce, Pr, Nd, Pm, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb, Lu, Hf, Ta, W, Re, Os, Ir, Pt, Au, Hg, Ac, Th, Pa, U, Np, Pu, Am, Cm, Bk, Cf, E, Fm, Mv, No, Lw.

TRAPATT DEVICE

An acronym for trapped plasma avalanche triggered transit diodes, which are biased into avalanche condition. As the diode breaks down, a highly conducting electron-hole plasma quickly fills the entire n-type region, and the voltage across the diode drops to a low value. The plasma is then extracted from the diode by the low residual electric field, thus causing a large current flow even though the voltage is low. Once extraction of the plasma is completed, the current drops and the voltage rises.

TRENCH ISOLATION

Electrical isolation of electronic components in a monolithic integrated circuit by the use of holes or other indentations in the surface of the device filled with dielectric material.

TUNNEL DIODE

A semiconductor diode in which the electrons penetrate a quantum barrier that is impenetrable in terms of classical physics, but which is penetrable in terms of quantum physics due to the quantum mechanical uncertainty in position of current carriers.

TUNNEL EFFECT/TUNNELLING

See TUNNEL DIODE and RESONANT TUNNELING DEVICE.

TWIN-TUB STRUCTURE

CMOS device structure in which both p-type and n-type deep wells are formed into a substrate for the n-channel and p-channel device (e.g., a transistor), respectively.

TWO-DIMENSIONAL ELECTRON GAS

A description of the motion of electrons which are confined in only one direction, such as electrons in the conducting channel of a MOSFET. In an electron gas, the electrons move around without apparent restriction. The behavior of electrons in conducting metals (e.g., copper) is an example of a three-dimensional electron gas. In a two dimensional electron gas, motion is restricted to a single plane (two dimensions).

UNIPOLAR

An active solid-state electronic device in which only one type of charge carrier, positive <u>or</u> negative, is used to support current flow.

UNIPOLAR TRANSISTOR

A transistor in which the source to drain current involves only one type of charge carrier.

VARACTOR

A semiconductor diode that changes capacitance with a change in applied voltage, comprising a two terminal active device using the voltage variable capacitance of a pn junction or a Schottky junction.

VARISTOR

A term applied to both passive and active solid-state devices. A varistor is a two-electrode semiconductor device with a voltage dependent nonlinear resistance which falls significantly as the voltage is increased. In an active device, the non-linear property is due to the presence of one or more potential barriers, whereas, in a passive type varistor, it is due to electrical heating of the material due to current flow therethrough. Varistors are to be contrasted with passive variable resistors such as rheostats or potentiometers.

VERTICAL JUNCTION

A junction of finite width which has a vertical axis. The materials which form it lie on either horizontal side thereof.

VIA

A metallized or plated-through hole, in an insulating layer, e.g., a substrate, chip or a printed circuit board which forms a conduction path itself and is not designed to have a wire or lead inserted therethrough.

WAFER

A thin slice of semiconductor material with parallel faces used as the substrate for active solid-state devices in discrete or monolithic integrated circuit form.

WIRE BOND

Attachment of a tiny wire, as by thermocompression bonding, to a bonding pad on a semiconductor chip.

WIRING CHANNEL

An area on an integrated circuit, such as a gate array, which is left free of active devices and in which interconnection metallization patterns are formed.

WORK FUNCTION

The minimum energy required to remove an electron from the Fermi level of a material and liberate it to free space outside the solid.

ZENER CURRENT

The current generated by a Zener diode when its reverse voltage is increased above the Zener breakdown value.

ZENER DIODE

A single pn junction, two terminal semiconductor diode reversed biased into breakdown caused by the Zener effect, i.e., by field emission of charge carriers in the device's depletion layer. NOTE: True Zener breakdown occurs in silicon at values below 6 volts. It is to be distinguished from the avalanche breakdown mechanism that occurs in reverse biased diodes at higher (about 6 volts) voltages.

SUBCLASSES

1 BULK EFFECT DEVICE:

This subclass is indented under the class definition. Subject matter in which the active device is made up of a semiconductor material whose electrical characteristics are due to the electronic properties of the semiconductor material, which are exhibited throughout the entire body of material rather than in just a localized region thereof (e.g., the surface).

(1) Note. Excluded from this subclass are semiconductive devices whose nonlinear characteristic is due to a junction rather than to the bulk properties of the semiconductor, whether they are homojunctions (i.e., made up of the same semiconductor material with different dopant ions on opposite sides of a junction) or heterojunctions (i.e., made up of different materials on either side of a junction).

SEE OR SEARCH THIS CLASS, SUBCLASS:

289, for insulated electrode devices having significant semiconductor compound in bulk crystal.

SEE OR SEARCH CLASS:

438, Semiconductor Device Manufacturing: Process, subclass 900 for methods of making a bulk effect semiconductor device.

2 Bulk effect switching in amorphous material:

This subclass is indented under subclass 1. Subject matter wherein the bulk material is an amorphous material, i.e., one in which active solid material is non-crystalline in the sense that (1) there is either complete disorder in the arrangement of atoms/mole or molecules of the material or (2) there is an absence of any long range structural order that is detectable by electron or X-ray diffraction patterns of the material and the device is used as an electronic switch.

3 With means to localize region of conduction (e.g., "pore" structure):

This subclass is indented under subclass 2. Subject matter wherein means (e.g., a porous structure) is provided to confine the operating current to a particular region of the bulk effect amorphous material.

4 With specified electrode composition or configuration:

This subclass is indented under subclass 2. Subject matter wherein the amorphous material bulk effect switching device has electrodes which have a particular chemical constituency or shape.

5 In array:

This subclass is indented under subclass 2. Subject matter in which the amorphous bulk effect switch has a group of individual switch elements with a predetermined (often regular) spacing extended in one or more directions.

(1) Note. The elements often extend in two dimensions to form two-dimensional arrays.

6 Intervalley transfer (e.g., Gunn effect):

This subclass is indented under subclass 1. Subject matter wherein electrons under the influence of sufficiently high electric fields are transferred between energy minima having different momentum in the conduction band of the active semiconductor material, or holes under the influence of sufficiently high electric fields are transferred between energy minima having different momentum in the valence band of the active semiconductor material.

SEE OR SEARCH CLASS:

331, Oscillators, subclass 107 for Gunn-type bulk effect device oscillators.

341, Coded Data Generation or Conversion, subclass 133 for analog to or from digital conversion with particular solid-state devices (e.g., Gunn effect devices).

365, Static Information Storage and Retrieval, subclass 169 for systems using a Gunn effect device.

7 In monolithic integrated circuit:

This subclass is indented under subclass 6. Subject matter wherein the intervalley transfer devices are integrally combined with one or more other active (e.g., diode or transistor) or passive (e.g., resistor or capacitor) devices in a single solid-state electronic device.

8 Three or more terminal device:

This subclass is indented under subclass 6. Subject matter wherein an intervalley transfer device contains three or more electrical terminals.

9 THIN ACTIVE PHYSICAL LAYER WHICH IS (1) AN ACTIVE POTENTIAL WELL LAYER THIN ENOUGH TO ESTABLISH DISCRETE QUANTUM ENERGY LEVELS OR (2) AN ACTIVE BARRIER LAYER THIN ENOUGH TO PERMIT QUANTUM MECHANICAL TUNNELING OR (3) AN ACTIVE LAYER THIN ENOUGH TO PERMIT CARRIER TRANSMISSION WITH SUBSTANTIALLY NO SCATTERING (E.G., SUPERLATTICE QUANTUM WELL, OR BALLISTIC TRANSPORT DEVICE):

This subclass is indented under the class definition. Subject matter wherein the active material is a thin physical layer of material located between materials which have different electrical properties than the thin layer and wherein the thin active physical layer is (1) a potential well layer thin enough to establish discrete quantum energy levels or (2) a potential barrier layer thin enough to permit quantum mechani-

cal tunneling or (3) a layer thin enough to permit carrier transmission therethrough with substantially no scattering of the carriers.

(1) Note. Examples of such devices are superlattice, quantum well, and ballistic transport devices.

(2) Note. Esaki tunneling is not the type of tunneling which this subclass and those indented thereunder contemplate. Esaki tunneling, while being quantum mechanical in nature, merely involves a tunneling barrier formed by a macroscopic depletion layer between n-type and p-type regions, but which neither a resonant tunneling barrier using controlled quantum mechanical charge confinement, a layer located between junctions, a thin layer as defined above. Esaki tunneling devices are found classified below, in subclasses 104+.

(3) Note. Active junction devices may employ a plurality of barrier junctions forming layers of material therebetween, but those layers are only classified in this subclass if they are thin enough to have the properties set forth in the definition. If those layers do not meet the definition, then the devices are classified below.

SEE OR SEARCH CLASS:

372, Coherent Light Generators, subclasses 43.01+ for semiconductor lasers which may contain thin layer devices of this type for producing coherent light.

10 Low workfunction layer for electron emission (e.g., photocathode electron emissive layer):

This subclass is indented under subclass 9. Subject matter wherein a layer of material from which electrons are emitted with less input energy than that necessary to emit them from adjacent material is provided.

(1) Note. The adjacent material and the low workfunction layer form either a heterojunction or a Schottky barrier, depending on whether both materials are semiconductors or one of the materials is a metal.

(2) Note. Typical low workfunction layer devices include cold cathode emitters in electron tubes.

SEE OR SEARCH CLASS:

313, Electric Lamp and Discharge Devices, subclasses 346+ and 373+ for photoemissive cathodes and subclasses 527, 530, 541, and 542+ for photocathodes in general.

438, Semiconductor Device Manufacturing: Process, subclass 20 for processes of making an electron emissive device utilizing a semiconductor substrate.

11 Combined with a heterojunction involving a III-V compound:

This subclass is indented under subclass 10. Subject matter in which the thin active layer and low workfunction layer for electron emission are combined with a heterojunction, i.e., a transition region between two materials with different energy band gaps, one material of which is a III-V compound, i.e., a compound wherein one material is found in group III of the periodic table and another material is found in group V of the periodic table.

12 Heterojunction:

This subclass is indented under subclass 9. Subject matter wherein the device includes at least two adjacent active layers, one of which is made of a substance that differs from that of the other.

(1) Note. See the illustration of a heterojunction device, in subclass 183.

SEE OR SEARCH THIS CLASS, SUBCLASS:

194, for heterojunction FETs having doping on the side of the heterojunction with lower carrier affinity.

13 Incoherent light emitter:

This subclass is indented under subclass 12. Subject matter wherein the device emits incoherent light.

(1) Note. Coherent light generators are explicitly excluded from this subclass. This means that cross-references from

Class 372, Coherent Light Generators, are not to be placed in this subclass. It is not desired to create a duplicate set of heterostructure lasers in this subclass.

SEE OR SEARCH CLASS:

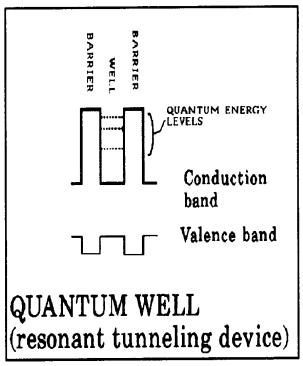
372, Coherent Light Generators, subclasses 43.01+ for coherent semiconductor light generators.

14 Quantum well:

This subclass is indented under subclass 12. Subject matter wherein at least two heterojunctions are formed with a thin active layer of material having a relatively large carrier affinity between two materials with smaller carrier affinities, resulting in a quantum mechanical energy well located in the thin active layer with the relatively large carrier affinity.

(1) Note. Quantum well devices appear in many forms, including (a) heterostructures; (b) only those high electron mobility transistors (HEMTs) which use a quantum well or a plurality of quantum wells; (c) superlattices which comprise many quantum wells so tightly coupled that the individual wells are not distinguishable, but rather the wells become analogous to atoms in a lattice and superlattice devices may behave more like new types of materials rather than as groups of coupled quantum wells; and (d) resonant tunneling devices - which exhibit quantum coupling, charge confinement and resonant tunneling.

(2) Note. See the illustration, below, for a graphic example of a quantum well device.

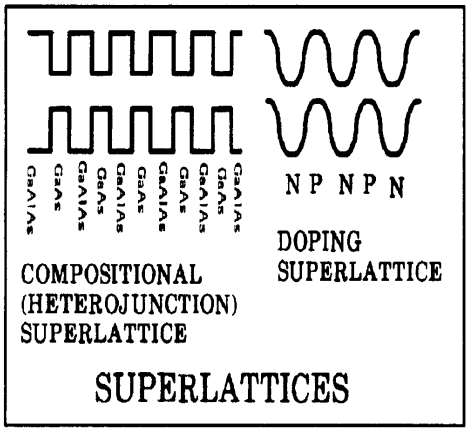


15 Superlattice:

This subclass is indented under subclass 14. Subject matter wherein a large number of quantum wells are present, the quantum wells being sufficiently close to each other that carrier quantum wave functions are spread out over plural quantum wells and the intervening barriers formed by the boundaries between adjacent layers having different carrier affinities.

(1) Note. Thicknesses of both the quantum well layers and the barrier layers are typically a few angstroms to a few hundred angstroms (10^{-10} meter) thick.

(2) Note. See the illustration, below, for energy level diagrams showing band edge energy discontinuities at four types of superlattice heterointerfaces.



SEE OR SEARCH CLASS:
148, Metal Treatment, digest 160 for superlattice treatment.

16 Of amorphous semiconductor material:
This subclass is indented under subclass 15. Subject matter wherein a superlattice active layer is made of a semiconductor crystal with no regular crystalline structure.

17 With particular barrier dimension:
This subclass is indented under subclass 15. Subject matter wherein the superlattice has a specific quantum electronic potential barrier dimension (e.g., height or width).

18 Strained layer superlattice:
This subclass is indented under subclass 15. Subject matter wherein the crystalline lattice characteristics of adjacent thin active superlattice layers are mismatched so that alternate layers are in elastic tension or compression.

19 Si_xGe_{1-x}:
This subclass is indented under subclass 18. Subject matter wherein at least one of the strained superlattice materials is a silicon-germanium alloy.

20 Field effect device:
This subclass is indented under subclass 15. Subject matter wherein the superlattice active layer forms the conduction channel of a field effect device (i.e., one which has two or more terminals denoted as source and gate with a conduction channel therebetween, and in which the current through the conducting channel is controlled by an electric field coming from a voltage which is applied between the gate and source terminals thereof).

21 Light responsive structure:
This subclass is indented under subclass 15. Subject matter wherein absorption of light (ultraviolet, visible, or infrared) by a superlattice active layer or junction causes a change in the current-voltage characteristic of the device.

22 With specified semiconductor materials:
This subclass is indented under subclass 15. Subject matter wherein the superlattice is formed of specified materials.

23 Current flow across well:
This subclass is indented under subclass 14. Subject matter wherein the device operation involves flow of carriers (electrons or holes) across the quantum well (as contrasted with tunneling through the well).

(1) Note. Current flow is considered to be "across" the well if the carriers have sufficient energy to pass over the barrier layers confining the quantum well, as contrasted to passing through the barriers by quantum mechanical tunneling.

SEE OR SEARCH THIS CLASS, SUBCLASS:
25, for devices which operate by resonant tunneling through the barriers, rather than over them.

24 Field effect device:
This subclass is indented under subclass 14. Subject matter wherein the quantum well device is a field effect device, i.e., one which has two or more terminals denoted as source and gate, with a conduction channel therebetween, and in which the current through the conducting channel is controlled by an electric field coming from a voltage which is applied between the gate and source terminals thereof.

(1) Note. See illustration under subclass 213 for various field effect devices.

25 Employing resonant tunneling:
This subclass is indented under subclass 14. Subject matter wherein the operation of the device depends not only on carrier charge confinement by the quantum well, but the quantum well layer also acts as an intermediate layer through which carriers pass by resonantly tunneling through both confining barriers and the well.

26 Ballistic transport device:
This subclass is indented under subclass 12. Subject matter in which an active layer is present through which carriers pass, wherein the active layer is thinner than the mean free path of the carriers in the material in that layer, so that carriers can pass through the layer without scattering.

(1) Note. Carriers are typically injected into the ballistic transport layer as "hot" carriers, having an energy, in the case of electrons, substantially greater than the minimum of the conduction band, or in the case of holes, substantially lower than the maximum of the valence band.

27 Field effect transistor:
This subclass is indented under subclass 26. Subject matter wherein the ballistic transport device is a field effect transistor, i.e., one which has two or more terminals denoted as source and gate with a conduction channel therebetween, and in which the current through the conducting channel is controlled by an electric field coming from a voltage which is applied between the gate and source terminals thereof.

(1) Note. See illustration, below, of various field effect devices under subclass 213.

28 Non-heterojunction superlattice (e.g., doping superlattice or alternating metal and insulator layers):
This subclass is indented under subclass 9. Subject matter wherein there are a plurality of active layers and barrier regions, the active layers being sufficiently close to each other that carrier quantum wave functions are spread out over plural active layers and the intervening barriers, and wherein the active layers and barrier regions do not form heterojunctions between different semiconductor materials.

(1) Note. Typically the active layers and barrier layers may be doped with opposite conductivity type dopants. Thicknesses of both the active layers and the barrier layers are typically a few angstroms to a few hundred angstroms (10^{-10} meter) thick.

29 Ballistic transport device (e.g., hot electron transistor):
This subclass is indented under subclass 9. Subject matter in which an active layer is present through which carriers pass, which active layer is thinner than the mean free path of the carriers in the material in that layer, so that carriers can pass through the layer without scattering.

(1) Note. Carriers are typically injected into the ballistic transport layer as "hot" carriers, having an energy, in the case of electrons, substantially greater than the minimum of the conduction band, or in the case of holes, substantially lower than the maximum of the valence band.

30 Tunneling through region of reduced conductivity:
This subclass is indented under subclass 9. Subject matter wherein the active layer through which carrier tunnelling occurs has lower electrical conductivity than the material adjacent thereto.

SEE OR SEARCH CLASS:
29, Metal Working, subclass 25.01 for methods of making barrier layer devices of the metal-insulator-metal type.
331, Oscillators, subclass 107 for superconductive element and tunneling element oscillators.

31 Josephson:
This subclass is indented under subclass 30. Subject matter wherein the device is of the form of a pair of superconductive electrodes separated by a thin, less conductive, portion, through which superconductive tunneling may occur.

SEE OR SEARCH CLASS:
29, Metal Working, subclass 25.01 for methods of making barrier layer devices possessing a Josephson junction.
216, Etching a Substrate: Processes, subclass 3 for Josephson Junction device manufacture involving etching.
505, Superconductor Technology: Apparatus, Material, Process, subclass 1 for high temperature superconductor Josephson devices with particular electrode materials and pertinent cross-reference art collections, including subclasses 857+ for nonlinear solid-state device, system, or circuit; and subclasses 873+ active solid-state devices.

32 Particular electrode material:
This subclass is indented under subclass 31. Subject matter wherein the electrode material is specified.

33 High temperature (i.e., >30° Kelvin):
This subclass is indented under subclass 32. Subject matter wherein the device can operate at temperatures above 30 degrees on the Kelvin temperature scale.

SEE OR SEARCH CLASS:
505, Superconductor Technology: Apparatus, Material, Process, subclass 1 for high temperature superconductor materials and devices.

34 Weak link (e.g., narrowed portion of superconductive line):
This subclass is indented under subclass 31. Subject matter wherein the active layer is a superconductive material of lower current capacity than the pair of superconductive electrodes.

35 Particular barrier material:
This subclass is indented under subclass 31. Subject matter wherein the active layer material is specified.

36 With additional electrode to control conductive state of Josephson junction:
This subclass is indented under subclass 31. Subject matter wherein a specific electrode in addition to the pair of superconductive electrodes forming the Josephson junction is used to control the conductive state of the junction.

37 At least one electrode layer of semiconductor material:
This subclass is indented under subclass 30. Subject matter wherein the tunneling device has at least one electrode layer comprised of a semiconductive material.

38 Three or more electrode device:
This subclass is indented under subclass 37. Subject matter wherein the tunneling device has three or more electrodes, at least one of which is made of a semiconductive material.

39 Three or more electrode device:
This subclass is indented under subclass 30. Subject matter wherein the tunneling device has three or more electrodes.

40 ORGANIC SEMICONDUCTOR MATERIAL:
This subclass is indented under the class definition. Subject matter comprising a semiconductor compound that includes an organic material characterized by two or more carbon atoms bonded together, one atom of carbon bonded to at least one atom of hydrogen or halogen (i.e., chlorine, fluorine, bromine, iodine), or one atom of carbon bonded to at least one atom of nitrogen by a single or double bond.

(1) Note. Certain compounds are exceptions to this rule, i.e., HCN, CN-CN, HNCO, HNCS, cyanogen halides, cyanamide, fulminic acid, and metal carbides. These are not regarded as organic materials.

(2) Note. Graphite and diamond are not regarded as organic, since they are not compounds; silicon carbide is not regarded as organic. Active solid-state devices using silicon carbide or diamond as the semiconductor are in subclass 77 of this class.

(3) Note. Organic insulating materials, as opposed to semiconducting materials, do not go in this subclass.

SEE OR SEARCH CLASS:
136, Batteries: Thermoelectric and Photoelectric, subclass 263 for photoelectric cells containing organic active material.
260, Chemistry of Carbon Compounds, and other classes which form integral parts of Class 260, appropriate subclasses for organic materials
313, Electric Lamp and Discharge Devices, subclass 504 for solid-state organic phosphor material luminescent devices.
361, Electricity: Electrical Systems and Devices, subclass 527 for solid electrolytic capacitors containing an organic salt.

438, Semiconductor Device Manufacturing: Process, subclass 82 for processes of making a light responsive device utilizing an organic semiconductor, and subclass 99 for methods of making an electrical device utilizing as a semiconductor component an organic semiconductor.

41 POINT CONTACT DEVICE:
This subclass is indented under the class definition. Subject matter including a junction between a semiconductor and a metallic element (e.g., wire) at a single point of contact therebetween.

42 SEMICONDUCTOR IS SELENIUM OR TELLURIUM IN ELEMENTAL FORM:
This subclass is indented under the class definition. Subject matter including a semiconductor material comprised of selenium or tellurium in elemental form (i.e., not in a compound).

SEE OR SEARCH CLASS:
430, Radiation Imagery Chemistry: Process, Composition or Product, subclass 57.8 for electrophotographic plates containing selenium or a selenium alloy.

43 SEMICONDUCTOR IS AN OXIDE OF A METAL (E.G., CuO, ZnO) OR COPPER SULFIDE:
This subclass is indented under the class definition. Subject matter wherein a semiconductor material includes a metal oxide or copper sulfide.

(1) Note. Those variable resistors known as "coherers" which are active solid-state devices, and are made of a metal oxide, are found in this subclass.

SEE OR SEARCH THIS CLASS, SUBCLASS:
798, for other active solid-state device type coherers.

SEE OR SEARCH CLASS:
338, Electrical Resistors, subclasses 1 and 223+ for passive solid-state coherers.
438, Semiconductor Device Manufacturing: Process, subclass 85 for processes of making a light responsive device utilizing as the semiconductive component a metal oxide or copper sulfide and subclasses 104 for methods of forming an electrical device utilizing as a semiconductive component a metal oxide or copper sulfide.

44 WITH METAL CONTACT ALLOYED TO ELEMENTAL SEMICONDUCTOR TYPE PN JUNCTION IN NONREGENERATIVE STRUCTURE:
This subclass is indented under subclass 107. Subject matter under the class definition wherein the active solid-state device has a pn junction formed by alloying one or more impurity metal contacts to an elemental semiconductor, and wherein the active solid-state device is not a regenerative device of this class.

(1) Note. The impurity metal contact alloys with a semiconductor material to form a p-region or n-region, depending on the impurity used.

45 Elongated alloyed region (e.g., thermal gradient zone melting, TGZM):
This subclass is indented under subclass 44. Subject matter wherein the alloyed region has at least one dimension substantially larger than another.

46 In pn junction tunnel diode (Esaki diode):
This subclass is indented under subclass 44. Subject matter wherein the alloyed pn junction device is a tunnel diode, i.e., wherein the active solid-state device includes a heavily doped pn junction wherein conduction occurs through the junction potential barrier due to a quantum mechanical effect even though the carriers which tunnel through the potential barrier do not have enough energy to overcome the barrier potential.

47 In bipolar transistor structure:
This subclass is indented under subclass 44. Subject matter wherein the alloyed pn junction device is a bipolar transistor, i.e., a transistor structure whose working current passes through semiconductor material of both polarities (p and n).

48 TEST OR CALIBRATION STRUCTURE:
This subclass is indented under the class definition. Subject matter in which structures are provided on active solid-state devices to permit or facilitate the measurement, test, or calibration of the characteristics of the devices.

(1) Note. Active solid-state device standards are also included herein.

SEE OR SEARCH CLASS:
324, Electricity: Measuring and Testing, subclass 158 for semiconductor device test apparatus and methods.
438, Semiconductor Device Manufacturing: Process, particularly subclass 18 for methods under the class definition having combined therewith a step of measuring an electrical condition utilizing a test element.

49 NON-SINGLE CRYSTAL, OR RECRYSTALLIZED, SEMICONDUCTOR MATERIAL FORMS PART OF ACTIVE JUNCTION (INCLUDING FIELD-INDUCED ACTIVE JUNCTION):
This subclass is indented under the class definition. Subject matter wherein there is an active junction (e.g., a junction between dissimilar materials, or a junction induced by an applied electric field, which exhibits non-linear current-voltage characteristics) and at least part of the active junction is formed by a semiconductor material in polycrystalline or amorphous form.

SEE OR SEARCH CLASS:
136, Batteries: Thermoelectric and Photoelectric, subclass 258 for photoelectric cells with polycrystalline or amorphous semiconductor material.
438, Semiconductor Device Manufacturing: Process, particularly subclass 96 and 482+ for methods of depositing amorphous semiconductive material functioning as an active region for an electrical device and subclasses 97 and 488+ for methods of depositing polycrystalline semiconductive material functioning as an active region for an electrical device.

50 Non-single crystal, or recrystallized, active junction adapted to be electrically shorted (e.g., "anti-fuse" element):
This subclass is indented under subclass 49. Subject matter wherein the active junction is structured or arranged to form an electrical short circuit between the electrical terminals of the active device.

51 Non-single crystal, or recrystallized, material forms active junction with single crystal material (e.g., monocrystal to polycrystal pn junction or heterojunction):
This subclass is indented under subclass 49. Subject matter wherein the active junction is formed by both non-single crystal material and single crystal material.

52 Amorphous semiconductor material:
This subclass is indented under subclass 49. Subject matter wherein the non-single crystal semiconductor material is amorphous, i.e., non-crystalline in the sense that (1) there is either complete disorder in the arrangement of atoms or molecules of the material or (2) there is an absence of any long range structural order that is detectable by electron or X-ray diffraction patterns of the material.

SEE OR SEARCH THIS CLASS, SUBCLASS:
2, through 5, for bulk effect switching in amorphous material.
16, for superlattice quantum well heterojunction devices of amorphous semiconductor material.
646, for amorphous semiconductor material coating to control surface effects.

SEE OR SEARCH CLASS:
136, Batteries: Thermoelectric and Photoelectric, subclass 258 for photoelectric cells with polycrystalline or amorphous semiconductor material.
438, Semiconductor Device Manufacturing: Process, particularly subclasses 482+ for methods for depositing amorphous semiconductor.

53 Responsive to nonelectrical external signals (e.g., light):
This subclass is indented under subclass 52. Subject matter wherein the amorphous semiconductor active junction generates an electrical signal when subjected to non-electrical (e.g., optical, thermal, or vibratory) signals.

SEE OR SEARCH CLASS:
430, Radiation Imagery Chemistry: Process, Composition or Product, subclass 57.4 for electrophotographic plates containing amorphous silicon.

54 With Schottky barrier to amorphous material:
This subclass is indented under subclass 53. Subject matter wherein the amorphous semiconductor active junction is formed with a metal, thereby forming a Schottky barrier.

55 Amorphous semiconductor is alloy or contains material to change band gap (e.g., Si_xGe_{1-x}, SiN_y):
This subclass is indented under subclass 53. Subject matter wherein the amorphous semiconductor is an alloy or contains material to change the band gap of the amorphous semiconductor material (e.g., Si_xGe_{1-x} see below, SiN_y).

SEE OR SEARCH THIS CLASS, SUBCLASS:
63, for this subject matter except in a device which is not responsive to nonelectrical external signals.

56 With impurity other than hydrogen to passivate dangling bonds (e.g., halide):
This subclass is indented under subclass 53. Subject matter wherein the amorphous semiconductor material is doped with an impurity other than hydrogen (e.g., a halide) for providing electrical stability by completing chemical bonds between semiconductor atoms which were not completed due to the amorphous nature of the semiconductor active layer material.

57 Field effect device in amorphous semiconductor material:
This subclass is indented under subclass 52. Subject matter wherein the amorphous semiconductor active junction is a field effect device, i.e., one which has a conducting channel and two or more electrodes, one of which is denoted a source and the other a drain electrode, and in which the current through the conducting channel is controlled by an electric field coming from a voltage which is applied between the gate and source terminals thereof.

(1) Note. See illustration under subclass 213 for various field effect devices.

SEE OR SEARCH CLASS:
438, Semiconductor Device Manufacturing: Process, particularly subclasses 149+ for methods of forming a field effect transistor on an insulating substrate or layer (e.g., SOS, SOI, etc.).

58 With impurity other than hydrogen to passivate dangling bonds (e.g., halide):
This subclass is indented under subclass 57. Subject matter wherein the semiconductor active junction amorphous field effect device is doped with an impurity other than hydrogen (e.g., a halide) for providing electrical stability by completing chemical bonds between semiconductor atoms which were not completed due to the amorphous nature of the semiconductor active layer material.

59 In array having structure for use as imager or display, or with transparent electrode:
This subclass is indented under subclass 57. Subject matter wherein a plurality of semiconductor active junction amorphous field effect devices are interconnected in a monolithic chip device for generating an image of an object, light from which is incident on the device, or for displaying signals applied to the device, or having an electrode that transmits optical radiation in the infrared, visible, or ultraviolet wavelength bands.

60 With field electrode under or on a side edge of amorphous semiconductor material (e.g., vertical current path):
This subclass is indented under subclass 57. Subject matter wherein the semiconductor active junction amorphous field effect device has an electrode located under or on a side edge of the device to affect the current path through the device (e.g., providing a vertical current path).

61 With heavily doped regions contacting amorphous semiconductor material (e.g., heavily doped source and drain):
This subclass is indented under subclass 57. Subject matter wherein the semiconductor active junction amorphous field effect device has regions in contact with the amorphous material which contain dopant ions with relatively heavy concentrations (e.g., 10^{18} to 10^{21} dopant atoms per cubic centimeter).

62 With impurity other than hydrogen to passivate dangling bonds (e.g., halide):
This subclass is indented under subclass 52. Subject matter wherein the semiconductor active junction amorphous field effect device is doped with an impurity other than hydrogen (e.g., a halide) for providing electrical stability by completing chemical bonds between semiconductor atoms which were not completed due to the amorphous nature of the semiconductor active layer material.

63 Amorphous semiconductor is alloy or contains material to change band gap (e.g., Si_xGe_{1-x}, SiN_y):
This subclass is indented under subclass 52. Subject matter wherein the amorphous semiconductor material is an alloy or contains material to change the energy gap between the valence and conduction bands.

SEE OR SEARCH THIS CLASS, SUBCLASS:
55, for this subject matter in a device which is responsive to nonelectrical external signals.

64 Non-single crystal, or recrystallized, material with specified crystal structure (e.g., specified crystal size or orientation):
This subclass is indented under subclass 49. Subject matter wherein the non-single crystal semiconductor material has a specified crystal structure, such as a specified grain size, a preferred crystallos:graphic axis, or orientation; polycrystalline material in the form of elongated crystallites; or particular configuration of grain boundaries.

65 Non-single crystal, or recrystallized, material containing non-dopant additive, or alloy of semiconductor materials (e.g., Ge_xSi_{1-x}, polycrystalline silicon with dangling bond modifier):
This subclass is indented under subclass 49. Subject matter wherein the non-single crystal semiconductor is an alloy or contains an additive other than an electrically active dopant, such as a dangling bond passivator or an additive to change the band gap of the amorphous semiconductor material (e.g., Si_xGe_{1-x}, SiN_y).

66 Field effect device in non-single crystal, or recrystallized, Semiconductor material:
This subclass is indented under subclass 49. Subject matter wherein the active solid-state device is a field effect device, i.e., one which operates with the application of a voltage across electrical terminals thereof.

SEE OR SEARCH CLASS:
438, Semiconductor Device Manufacturing: Process, particularly subclasses 149+ for methods of forming a field effect transistor on an insulating substrate or layer (e.g., SOS, SOI, etc.).

67 In combination with device formed in single crystal semiconductor material (e.g., stacked FETs):
This subclass is indented under subclass 66. Subject matter wherein the field effect device is combined with an active or passive solid-state device located in a single crystal semiconductor material (i.e., one in which atoms are arranged in a regular three dimensional array).

68 Capacitor element in single crystal semiconductor (e.g., DRAM):
This subclass is indented under subclass 67. Subject matter wherein the device is a capacitor element in single crystal material.

69 Field effect transistor in single crystal material, complementary to that in non-single crystal, or recrystallized, material (e.g., CMOS):
This subclass is indented under subclass 67. Subject matter wherein there is a field effect transistor in single crystal material complementary in polarity to the field effect device in the non-single crystal, or recrystallized, material (e.g., a CMOS device).

70 Recrystallized semiconductor material:
This subclass is indented under subclass 67. Subject matter wherein the combined device contains a non-single semiconductor region of recrystallized material.

(1) Note. Recrystallized semiconductor material has been processed, typically by heat or laser irradiation to cause growth of large regions of substantially single crystal material to obtain properties approximating those of completely single crystal material.

71 In combination with capacitor element (e.g., DRAM):
This subclass is indented under subclass 66. Subject matter wherein the field effect device in the non-single crystal, or recrystallized, semiconductor material is combined with a capacitor element.

72 In array having structure for use as imager or display, or with transparent electrode:
This subclass is indented under subclass 66. Subject matter wherein a plurality of field effect devices in non-single crystal, or recrystallized, semiconductor material are interconnected in a monolithic chip device for generating an image of an object, light from which is incident on the device, or for displaying signals applied to the device, or having an electrode that transmits optical radiation in the infrared, visible, or ultraviolet wavelength bands.

73 Schottky barrier to polycrystalline semiconductor material:
This subclass is indented under subclass 49. Subject matter wherein the device contains a non-ohmic, rectifying metal-to-polycrystalline bulk material electrical contact.

74 Plural recrystallized semiconductor layers (e.g., "3-dimensional integrated circuit"):
This subclass is indented under subclass 49. Subject matter wherein the recrystallized material comprises more than one layer of recrystallized semiconductor material.

75 Recrystallized semiconductor material:
This subclass is indented under subclass 49. Subject matter wherein the device contains a non-single crystal semiconductor material whose amorphous nature is due to recrystallization.

76 SPECIFIED WIDE BAND GAP (1.5eV) SEMICONDUCTOR MATERIAL OTHER THAN GaAsP or GaAlAs:
This subclass is indented under the class definition. Subject matter including a semiconductor material with a band gap (between its valance and conduction bands) greater that 1.5 electron volts which is not gallium arsenide phosphide or gallium aluminum arsenide.

77 Diamond or silicon carbide:
This subclass is indented under subclass 76. Subject matter wherein the specified wide band gap material is diamond or silicon carbide.

78 II-VI compound:
This subclass is indented under subclass 76. Subject matter wherein the specified wide band gap material is a compound, one element of which comes from group II, and the other element of which comes from group VI of the periodic table of elements.

79 INCOHERENT LIGHT EMITTER STRUCTURE:
This subclass is indented under the class definition. Subject matter wherein the active solid-state device generates incoherent light when subjected to an appropriate input signal.

(1) Note. Lasers (coherent light generators) are classified in Class 372, and patents

directed to lasers are not to be cross-referenced in this or indented subclasses unless such patent contains disclosure of a light emitting semiconductor device which is NOT a laser or coherent light generator.

SEE OR SEARCH THIS CLASS, SUBCLASS:

13, for incoherent thin physical layer light emitter devices with operating principles as specified therein.

SEE OR SEARCH CLASS:

250, Radiant Energy, subclasses 552+ for solid-state light source circuits.

313, Electric Lamp and Discharge Devices, subclasses 498+ for electric lamp and discharge devices having solid-state luminescent materials, including nominally recited luminescent semiconductor type materials; and subclass 504 for solid-state organic phosphor material luminescent devices.

340, Communications: Electrical, subclasses 760+ and 766+ for solid-state light emitting arrays and array elements.

362, Illumination, subclass 84 for light source or light source support and luminescent material and subclass 800 (cross-reference art collection) for light emitting diode light sources.

438, Semiconductor Device Manufacturing: Process, particularly subclasses 22+ for methods of forming a semiconductor device which may be emissive of either coherent or incoherent radiation.

80 In combination with or also constituting light responsive device:

This subclass is indented under subclass 79. Subject matter wherein the light emitting active semiconductor device is combined with a separate device which generates an electrical signal when light impinges upon it or the active device both emits light when stimulated and generates an electrical signal in response to light impingent thereupon.

SEE OR SEARCH CLASS:

250, Radiant Energy, subclass 551 for signal isolators involving a light source and photodetector.

81 With specific housing or contact structure:

This subclass is indented under subclass 80. Subject matter wherein the combined light emitting and light responsive device is provided with a particular housing or electrical contact structure.

82 Discrete light emitting and light responsive devices:

This subclass is indented under subclass 81. Subject matter wherein the device with a specific housing or contact structure contains separate light emitting and light responsive elements.

83 Light coupled transistor structure:

This subclass is indented under subclass 80. Subject matter wherein the active solid-state device has a pair of rectifying junctions, a first of which when forward biased produces light which, when absorbed in the depletion region of the second junction when reverse biased, produces a current through the second junction, with the first junction functioning similarly to the emitter-base junction, and the second junction functioning similarly to the base-collector junction, of an ordinary bipolar transistor.

SEE OR SEARCH CLASS:

250, Radiant Energy, subclass 551 for signal isolator for optically coupled light emitter and light detector combinations wherein the devices are used to isolate electrical signals.

84 Combined in integrated structure:

This subclass is indented under subclass 80. Subject matter wherein the light emitting and light responsive devices are combined in a single crystal monolithic structure.

85 With heterojunction:

This subclass is indented under subclass 84. Subject matter wherein the device contains a heterojunction, i.e., wherein the junction separates semiconductor materials of different chemical composition.

86 Active layer of indirect band gap semiconductor:
This subclass is indented under subclass 79. Subject matter wherein the light emitting active region is in or between semiconductor materials in which direct transitions of electrons from conduction to valance bands do not take place.

(1) Note. Transitions may take place in steps due to trapping levels located in the forbidden band between the conduction and valance bands.

87 With means to facilitate electron-hole recombination (e.g., isoelectronic traps such as nitrogen in GaP):
This subclass is indented under subclass 86. Subject matter wherein the light emitting active region with an indirect band gap layer has means to facilitate electron-hole recombination (e.g., isoelectronic traps such as nitrogen in gallium phosphide).

88 Plural light emitting devices (e.g., matrix, 7-segment array):
This subclass is indented under subclass 79. Subject matter wherein the light emitting active semiconductor device contains more than one light emitting active junction.

SEE OR SEARCH CLASS:
340, Communications: Electrical, subclasses 760+ and 766+ for solid-state light emitting arrays and array elements.

89 Multi-color emission:
This subclass is indented under subclass 88. Subject matter wherein different light emitting devices emit light of different hues.

90 With heterojunction:
This subclass is indented under subclass 89. Subject matter wherein there is at least one heterojunction, i.e., wherein the junction separates semiconductor materials of different chemical composition.

91 With shaped contacts or opaque masking:
This subclass is indented under subclass 88. Subject matter wherein the plural light emitting devices have electrical contacts with specific shapes or are combined with optical elements which are impervious to light emitted by the devices and are placed in the path of light emitted by the devices.

92 Alphanumeric segmented array:
This subclass is indented under subclass 88. Subject matter wherein the plural light emitting devices are structured and arranged in segments of Arabic numerals or alphabet letters.

SEE OR SEARCH CLASS:
340, Communications: Electrical, subclasses 760+ and 766+ for solid-state light emitting arrays and array elements.

93 With electrical isolation means in integrated circuit structure:
This subclass is indented under subclass 88. Subject matter wherein means to provide electrical isolation, i.e., to prevent electrical short circuits, with respect to each light emitting device, are provided in a single, monolithic chip structure.

94 With heterojunction:
This subclass is indented under subclass 79. Subject matter wherein there is at least one junction between semiconductor materials of different chemical compositions.

(1) Note. See the illustration of a heterojunction device in subclass 183.

95 With contoured external surface (e.g., dome shape to facilitate light emission):
This subclass is indented under subclass 94. Subject matter wherein the light emitting device has an external surface with a particular geometric shape, for example, a dome shape to facilitate emission of light from the light emitting device, in spite of it being made of semiconductor material of relatively high index of refraction.

96 Plural heterojunctions in same device:
This subclass is indented under subclass 94. Subject matter wherein the heterojunction light emitting device has more than one heterojunction.

97 More than two heterojunctions in same device:
This subclass is indented under subclass 96. Subject matter wherein the light emitting device has more than two heterojunctions.

98 With reflector, opaque mask, or optical element (e.g., lens, optical fiber, index of refraction matching layer, luminescent material layer, filter) integral with device or device enclosure or package:
This subclass is indented under subclass 79. Subject matter wherein the light emitting active junction device is combined with one or more optical elements (e.g., to transmit or shape or otherwise affect light emitted by the device); and the optical element is an integral part of the device or of the housing, encapsulant, or other device enclosure or package.

99 With housing or contact structure:
This subclass is indented under subclass 79. Subject matter wherein the light emitting active junction device is combined with a housing or electrical contact structure.

100 Encapsulated:
This subclass is indented under subclass 79. Subject matter wherein the light emitting active junction device is embedded in a protective coating.

SEE OR SEARCH CLASS:
174, Electricity: Conductors and Insulators, subclass 521 for potted or encapsulated electrical devices.
439, Electrical Connectors, subclass 936 for potting material or coating for electrical conductors.

101 With particular dopant concentration or concentration profile (e.g., graded junction):
This subclass is indented under subclass 79. Subject matter wherein the light emitting active junction has a particular concentration of dopant ions or profile in a given direction or cross sectional area or volume.

102 With particular dopant material (e.g., zinc as dopant in GaAs):
This subclass is indented under subclass 79. Subject matter wherein the dopant material of the active junction is specified.

103 With particular semiconductor material:
This subclass is indented under subclass 79. Subject matter wherein the active junction is in or between semiconductor material whose composition is specified.

104 TUNNELING PN JUNCTION (E.G., ESAKI DIODE) DEVICE:
This subclass is indented under the class definition. Subject matter wherein the active solid-state device includes a heavily doped pn junction where conduction occurs through the junction potential barrier due to a quantum mechanical effect even though the carriers which tunnel through the potential barrier do not have enough energy to overcome the barrier potential.

(1) Note. PN Junction tunnel diodes operated under forward bias are often referred to as Esaki diodes.

SEE OR SEARCH THIS CLASS, SUBCLASS:
46, for an Esaki diode having a metal contact alloyed to elemental semiconductor type pn junction in a non-regenerative structure.

SEE OR SEARCH CLASS:
326, Electronic Digital Logic Circuitry, subclass 134 for a digital logic device which includes a tunnel diode.
327, Miscellaneous Active Electrical Nonlinear Devices, Circuits, and Systems, subclass 195 for stable state circuits utilizing a tunnel diode; subclass 326 for limiting, clipping, or clamping using a tunnel diode; subclass 402 for a delay controlled switch with tunnel diode; subclasses 420 and 499 for gating circuits utilizing transistors or diodes respectively which use tunnel diodes; and subclass 570 for miscellaneous tunnel diode circuits.
331, Oscillators, subclass 107 for tunnel diode oscillators.
361, Electricity: Electrical Systems and Devices, subclass 100 for tunnel diode current responsive fault sensors.

105 In three or more terminal device:
This subclass is indented under subclass 104. Subject matter wherein the tunnel junction is part of an active solid-state electronic device which has three or more electrical terminals (e.g., transistors or thyristors).

106 Reverse bias tunneling structure (e.g., "backward" diode, true Zener diode):
This subclass is indented under subclass 104. Subject matter wherein the tunnel junction is structured to permit quantum mechanical tunneling of carriers in a reverse bias mode, i.e., when the p-side of the junction is connected to a negative voltage source and the n-side of the junction is connected to a positive voltage source.

(1) Note. In silicon, such conduction occurs when the junction breakdown voltage is less than approximately 5.6 volts.

SEE OR SEARCH CLASS:
148, Metal Treatment, digest 174 for treatment of Zener diodes.
323, Electricity: Power Supply or Regulation Systems, subclass 231 for systems using a Zener diode and being in shunt with a load.
327, Miscellaneous Active Electrical Nonlinear Devices, Circuits, and Systems, subclasses 194 and 195 for stable state circuits with a zener or back diode respectively; subclass 326 for limiting, clipping, or clamping utilizing a zener diode; subclass 421 for gating circuits having a transistor which utilizes a zener effect; subclass 502 for a gating circuit with zener diode; and subclass 584 for a miscellaneous circuit utilizing a zener diode.
361, Electricity: Electrical Systems and Devices, subclass 197, for relay time delay safety or protection devices including, for example, a Zener diode.
377, Electrical Pulse Counters, Pulse Dividers, or Shift Registers: Circuits and Systems, subclass 128 for pulse counting or dividing chains which include bi-stable semiconductor devices with only two electrodes, e.g., tunnel diodes.

107 REGENERATIVE TYPE SWITCHING DEVICE (E.G., SCR, COMFET, THYRISTOR):
This subclass is indented under the class definition. Subject matter wherein the active solid-state device acts as if it has two or more active emitter junctions each of which is associated with a separate, equivalent transistor having an individual gain and, when initiated by a base region current, the equivalent transistors mutually drive each other in a regenerative manner to lower the voltage drop between the emitters.

(1) Note. If the current is above a level I_H, called the "holding current", then the device will remain ON when the triggering signal is removed by the regenerative feedback therebetween, and is then said to be "latched".

SEE OR SEARCH CLASS:
123, Internal-Combustion Engines, subclass 648 for circuits employing silicon controlled rectifiers (SCRs).
327, Miscellaneous Active Electrical Nonlinear Devices, Circuits, and Systems, subclasses 199+ for a bistable circuit which includes diverse solid-state devices such as an SCR, subclasses 392+ for a delay controlled switch which may include an SCR, and subclasses 438+ for gating circuits which may use a thyristor or SCR.
361, Electricity: Electrical Systems and Devices, subclasses 100+ and 205 for circuits employing thyristors (e.g., silicon controlled rectifiers (SCRs)).
363, Electric Power Conversion Systems, subclasses 27+, 54, 57+, 68, 85+, 96+, 128+, 135+, and 160+ for circuits employing thyristors (e.g., silicon controlled rectifiers (SCRs)).
388, Electricity: Motor Control Systems, subclasses 917+ for circuits employing thyristors (e.g., silicon controlled rectifiers (SCRs)).
438, Semiconductor Device Manufacturing: Process, particularly subclasses 133+ for methods of forming a regenerative type switching device.

108 Controlled by nonelectrical, nonoptical external signal (e.g., magnetic field, pressure, thermal):
This subclass is indented under subclass 107. Subject matter wherein the regenerative switching device is controlled by an input signal other than an optical or electrical signal (e.g., by a magnetic field) or by mechanical stress.

109 Having only two terminals and no control electrode (gate), e.g., Shockley diode:
This subclass is indented under subclass 107. Subject matter wherein the regenerative switching device has only two electrical terminals, neither one of which is a control electrode (e.g., gate or base electrode).

110 More than four semiconductor layers of alternating conductivity types (e.g., pnpnpn structure, 5 layer bidirectional diacs, etc.):
This subclass is indented under subclass 109. Subject matter wherein the two terminal device with no control electrode has more than four layers of semiconductor material, each layer having an electrical conductivity type (e.g., p-type or n-type) which differs from that of each adjacent layer.

111 Triggered by V_{BO} overvoltage means:
This subclass is indented under subclass 109. Subject matter wherein the two terminal device with no control electrode includes means to apply a voltage larger than the breakover voltage V_{BO} to initiate operation of the device.

112 With highly-doped breakdown diode trigger:
This subclass is indented under subclass 109. Subject matter wherein the two terminal device with no control electrode includes a diode portion which is heavily doped to decrease its breakdown voltage to trigger the device into operation.

113 With light activation:
This subclass is indented under subclass 107. Subject matter wherein the regenerative switching device is activated (e.g., turned on and/or off) by light impinging on a light sensitive portion of the device.

114 With separate light detector integrated on chip with regenerative switching device:
This subclass is indented under subclass 113. Subject matter wherein the light sensitive portion is separate from the regenerative switching device, and is contained in a physically separated area of a single, monolithic chip with the regenerative switching device.

115 With electrical trigger signal amplification means (e.g., amplified gate, "pilot thyristor", etc.):
This subclass is indented under subclass 113. Subject matter wherein means are provided to amplify the electrical signal generated by the light sensitive portion, in order to trigger the regenerative switching device.

116 With light conductor means (e.g., light fiber or light pipe) integral with device or device enclosure or package:
This subclass is indented under subclass 113. Subject matter wherein the active semiconductor device is provided with means to conduct light (e.g., as light fiber or light pipe) to the light sensitive portion, and the light conductor means is an integral part of the device or of the housing, encapsulant or other device enclosure, or package.

117 In groove or with thinned semiconductor portion:
This subclass is indented under subclass 116. Subject matter wherein the light sensitive portion is located in a groove in the device or wherein it is covered by a relatively thin portion of semiconductor material.

118 With groove or thinned light sensitive portion:
This subclass is indented under subclass 113. Subject matter wherein the light sensitive portion is located in a groove in the surface of the device or is located close to the surface of the device in a thinned region of the device so that only a relatively thin portion of the device has to be traversed by light.

119 Bidirectional rectifier with control electrode (gate) (e.g., Triac):
This subclass is indented under subclass 107. Subject matter wherein the regenerative switching device has a control electrode, can

conduct in both forward and reverse directions, and can be triggered into conduction by a pulse applied to its control electrode.

SEE OR SEARCH THIS CLASS, SUBCLASS:
110, for bidirectional rectifiers with no control electrode.

SEE OR SEARCH CLASS:
323, Electricity: Power Supply or Regulation Systems, subclasses 240 and 325 for circuit having unidirectional elements with bidirectional pass.

120 Six or more semiconductor layers of alternating conductivity types (e.g., npnpnpn structure):
This subclass is indented under subclass 119. Subject matter wherein the bidirectional rectifier with control electrode contains six or more layers of semiconductor material, each of which has a different conductivity type, (e.g., n-type or p-type) which differs from that of each adjacent layer.

121 With diode or transistor in reverse path:
This subclass is indented under subclass 119. Subject matter wherein a diode (i.e., a device which passes current in only one direction) is connected to conduct current in one direction, with a regenerative switching device with a control electrode connected to conduct current in the other direction to produce a bi-directionally conducting regenerative switching device.

122 Lateral:
This subclass is indented under subclass 119. Subject matter wherein the bidirectional rectifier with control electrode is of the lateral type, i.e., when viewed in cross section, the two main electrodes (e.g., anode and cathode) are arranged horizontally, side-by-side in the same surface of the semiconductor body.

123 With trigger signal amplification (e.g., amplified gate):
This subclass is indented under subclass 119. Subject matter wherein the bidirectional rectifier with control electrode is combined with means to amplify the electrical signal applied to the control electrode to trigger the device.

124 Combined with field effect transistor structure:
This subclass is indented under subclass 119. Subject matter wherein the bidirectional rectifier with control electrode includes or is combined with a field effect transistor structure, i.e., a transistor in which the current through a conducting channel is controlled by an electric field coming from a voltage which is applied between the gate and source terminals thereof.

(1) Note. See illustration under subclass 213 for various field effect devices.

125 Controllable emitter shunting:
This subclass is indented under subclass 124. Subject matter wherein the field effect transistor structure is connected to shunt one of the emitter-base junctions of the regenerative structure under control of the voltage applied to the gate of the field effect transistor.

126 With means to separate a device into sections having different conductive polarity:
This subclass is indented under subclass 119. Subject matter wherein the bidirectional rectifier with control electrode has means separating portions thereof which have different conductive polarity.

127 Guard ring or groove:
This subclass is indented under subclass 126. Subject matter wherein the means to separate portions of the device having different conductive polarity is or includes a groove, or a guard ring, i.e., a pn junction region in the body of the device located and/or configured to reduce electric field strength at a given applied voltage.

128 Having overlapping sections of different conductive polarity:
This subclass is indented under subclass 119. Subject matter wherein the bidirectional rectifier with control electrode has outer emitter regions which overlap one another in at least one portion.

129 With means to increase reverse breakdown voltage:
This subclass is indented under subclass 119. Subject matter wherein the bidirectional rectifier with control electrode has means associ-

ated therewith to increase the reverse voltage which may be applied without causing electrical breakdown.

130 Switching speed enhancement means:
This subclass is indented under subclass 119. Subject matter wherein the bidirectional rectifier with control electrode includes or is combined with means to increase the speed at which the device switches.

131 Recombination centers or deep level dopants:
This subclass is indented under subclass 130. Subject matter wherein the switching speed enhancement means include (1) centers wherein excess holes and electrons recombine and are removed as charge carriers in the device or (2) dopant ions with energy levels that are located in the forbidden band of the active semiconductor material of the device.

132 Five or more layer unidirectional structure:
This subclass is indented under subclass 107. Subject matter wherein the regenerative active solid-state device has five or more layers of semiconductor material producing at least four active junctions, and is operable in a single electrical direction.

133 Combined with field effect transistor:
This subclass is indented under subclass 107. Subject matter wherein the regenerative device includes or is combined with a field effect transistor, i.e., a transistor in which the current through a conducting channel is controlled by an electric field coming from a voltage which is applied between the gate and source terminals thereof.

134 J-FET (junction field effect transistor):
This subclass is indented under subclass 133. Subject matter wherein the field effect transistor combined with the regenerative action junction type switching device is a junction field effect transistor, i.e., a field effect transistor wherein the gate region is isolated from the conducting channel by a rectifying pn junction or Schottky barrier junction.

SEE OR SEARCH THIS CLASS, SUBCLASS:
287, for power JFET devices.
504, for JFET type isolation.

135 Vertical (i.e., where the source is located above the drain or vice versa):
This subclass is indented under subclass 134. Subject matter wherein the operating current path of the JFET is perpendicular to the plane of its main surface.

136 Enhancement mode (e.g., so-called SITs):
This subclass is indented under subclass 135. Subject matter in which no current flows except for leakage current, when the gate to source voltage is zero.

(1) Note. Conduction does not begin until the gate voltage reaches a finite threshold value.

(2) Note. Compare this with depletion mode J-FETS in which maximum current is passed by the transistor at a zero gate potential and current decreases as the gate voltage increases.

137 Having controllable emitter shunt:
This subclass is indented under subclass 133. Subject matter wherein the regenerative switching device is combined with a junction field effect transistor that is connected across an emitter-base junction of the regenerative device to controllably divert current from the emitter-base junction.

138 Having gate turn off (GTO) feature:
This subclass is indented under subclass 137. Subject matter wherein the regenerative switch is configured to permit application of sufficient gate current to switch the regenerative switch to the OFF state.

139 With extended latchup current level (e.g., COMFET device):
This subclass is indented under subclass 133. Subject matter wherein the regenerative active junction type switching device (e.g., a conductivity modulated FET) includes means to provide regenerative action without latchup over an extended current range of the device (i.e., by increasing I_H).

140 Combined with other solid-state active device in integrated structure:
This subclass is indented under subclass 139. Subject matter wherein the extended latchup current level device is combined with another solid-state active device in a monolithic single crystal chip structure.

141 Lateral structure, i.e., current flow parallel to main device surface:
This subclass is indented under subclass 139. Subject matter wherein the extended latchup current level device is structured so that operating current flows parallel to the main device surface (i.e., horizontally or laterally).

142 Having impurity doping for gain reduction:
This subclass is indented under subclass 139. Subject matter wherein the extended latchup current level device has impurity dopant to reduce device regenerative gain, i.e., the gain or amplification of one or more of the active junction portions connected in regenerative fashion.

143 Having anode shunt means:
This subclass is indented under subclass 139. Subject matter wherein the extended latchup current level device has means connected across the emitter-base junction of the PNP transistor portion of the regenerative device to controllably divert current from the emitter-base junction.

144 Cathode emitter or cathode electrode feature:
This subclass is indented under subclass 139. Subject matter wherein the extended latchup current level device has a particular cathode emitter or cathode electrode feature.

145 Low impedance channel contact extends below surface:
This subclass is indented under subclass 139. Subject matter wherein the extended latchup current level device has an electrical contact extending from the device surface into the body of the device which is connected to the channel of the field effect transistor portion and wherein the contact has a relatively low electrical impedance.

146 Combined with other solid-state active device in integrated structure:
This subclass is indented under subclass 107. Subject matter wherein the regenerative active junction type switching device is combined with one or more active or passive electronic solid-state devices in a unitary, monolithic, integrated structure.

147 With extended latchup current level (e.g., gate turn off "GTO" device):
This subclass is indented under subclass 107. Subject matter wherein the regenerative switching device includes means to provide regenerative action without latchup over an extended current range of the device, i.e., extends I_H as defined in subclass 107.

(1) Note. Another name for this device is a gate controlled switch.

148 Having impurity doping for gain reduction:
This subclass is indented under subclass 147. Subject matter wherein the regenerative switching device has impurity dopant to reduce device gain of one of the equivalent transistors.

SEE OR SEARCH THIS CLASS, SUBCLASS:
142, for this subject matter in a COMFET device.

149 Having anode shunt means:
This subclass is indented under subclass 147. Subject matter wherein the regenerative switching device has means connected across the emitter-base junction of the PNP transistor section of the regenerative device to divert current from the emitter-base junction.

150 With specified housing or external terminal:
This subclass is indented under subclass 147. Subject matter wherein the regenerative switching device is provided with means to enclose it or a terminal means located external to an enclosure for the device.

151 External gate terminal structure or composition:
This subclass is indented under subclass 150. Subject matter wherein the external electrical terminal structural features or material composition is specified.

152 Cathode emitter or cathode electrode feature:
This subclass is indented under subclass 147. Subject matter wherein the extended latchup current level device has a particular cathode emitter or cathode electrode feature.

153 Gate region or electrode feature:
This subclass is indented under subclass 147. Subject matter wherein the extended latchup current level device has a particular gate (control) electrode feature.

154 With resistive region connecting separate sections of device:
This subclass is indented under subclass 107. Subject matter wherein the regenerative active junction type switching device has a resistive region or portion connecting discrete regions of the device.

155 With switching speed enhancement means (e.g., Schottky contact):
This subclass is indented under subclass 107. Subject matter wherein the regenerative active junction type switching device is provided with means to increase its switching speed.

156 Having deep level dopants or recombination centers:
This subclass is indented under subclass 155. Subject matter wherein the regenerative device has deep level dopants or electron-hole recombination centers with energy levels that are within the forbidden energy band and widely spaced from the conduction and valence bands of the semiconductor device.

157 With integrated trigger signal amplification means (e.g., amplified gate, "pilot thyristor", etc.):
This subclass is indented under subclass 107. Subject matter wherein the regenerative switching device has means to amplify the control current of the device, which is physically integrated with the regenerative switching device.

SEE OR SEARCH THIS CLASS, SUBCLASS:
115, for light activated regenerative devices with trigger signal amplification.
123, for bidirectional regenerative devices with trigger signal amplification.

SEE OR SEARCH CLASS:
330, Amplifiers, subclasses 250+ for semiconductor amplifying devices (e.g., transistors

158 Three or more amplification stages:
This subclass is indented under subclass 157. Subject matter wherein the amplification means has three or more stages of amplification.

159 Transistor as amplifier:
This subclass is indented under subclass 157. Subject matter wherein the amplification means is a transistor (i.e., an active semiconductor device having three or more electrodes).

160 With distributed amplified current:
This subclass is indented under subclass 157. Subject matter wherein the regenerative device with amplification means produces amplified current which is distributed by electrodes to other portions of the device.

161 With a turn-off diode:
This subclass is indented under subclass 157. Subject matter wherein the regenerative device with amplification means is integrally provided with a diode, i.e., a solid-state active rectifying two terminal device, to bypass the amplifying stage(s), in order to switch OFF the regenerative device.

162 Lateral structure:
This subclass is indented under subclass 107. Subject matter wherein the regenerative active junction type switching device has a lateral structure, i.e., one in which the active junctions are arranged so that electric current flows from side to side, rather than from top to bottom of the device.

163 Emitter region feature:
This subclass is indented under subclass 107. Subject matter wherein the active emitter junction region of the regenerative device has a particular characteristic.

164 Multi-emitter region (e.g., emitter geometry or emitter ballast resistor):
This subclass is indented under subclass 163. Subject matter wherein the regenerative switching device has more than one emitter region.

SEE OR SEARCH THIS CLASS, SUBCLASS:
580+, for bipolar transistors with emitter ballast resistors.

165 Laterally symmetric regions:
This subclass is indented under subclass 164. Subject matter wherein the plural emitters are located in regions of the device which are symmetrical in a horizontal direction.

166 Radially symmetric regions:
This subclass is indented under subclass 164. Subject matter wherein the plural emitters are located in regions of the device which are symmetrical extending radially in a horizontal direction from a predetermined emitter location.

167 Having at least four external electrodes:
This subclass is indented under subclass 107. Subject matter wherein the regenerative active junction switching device has at least four electrodes connected to the outside of the device.

168 With means to increase breakdown voltage:
This subclass is indented under subclass 107. Subject matter wherein the regenerative active junction type switching device includes means to increase the reverse voltage which the device can sustain without breaking down.

169 High resistivity base layer:
This subclass is indented under subclass 168. Subject matter wherein the means for increasing breakdown voltage includes a base (as contrasted with emitter or collector) layer which has a relatively high electrical resistivity.

170 Surface feature (e.g., guard ring, groove, mesa, etc.):
This subclass is indented under subclass 168. Subject matter wherein the means for increasing breakdown voltage includes a surface feature (e.g., a guard ring or groove or mesa).

171 Edge feature (e.g., beveled edge):
This subclass is indented under subclass 170. Subject matter wherein the surface feature for increasing breakdown voltage is an edge feature (e.g., a beveled) as contrasted with a right angled edge.

172 With means to lower "ON" voltage drop:
This subclass is indented under subclass 107. Subject matter wherein the regenerative active junction type switching device comprises means to lower the voltage drop across the main terminals when the switch is operated in the ON mode.

173 Device protection (e.g., from overvoltage):
This subclass is indented under subclass 107. Subject matter wherein the regenerative active junction type switching device includes means for protecting the device from destructive overloads (e.g., from operating voltage above a particular threshold level).

SEE OR SEARCH CLASS:
361, Electricity: Electrical Systems and Devices, subclasses 91.1+ for overvoltage protection in safety and protection of systems and devices.

174 Rate of rise of current (e.g., dI/dt):
This subclass is indented under subclass 173. Subject matter wherein the parameter for which protection means is provided is the rate of rise of operating current in the device.

175 With means to control triggering (e.g., gate electrode configuration, Zener diode firing, dV/Dt control, transient control by ferrite bead, etc.):
This subclass is indented under subclass 107. Subject matter wherein the regenerative active junction type switching device includes means for controlling device turn-on.

(1) Note. Transient electrical phenomena, e.g., damped oscillations or surges in operation current or voltage following a sudden change in the applied voltage or current to the device, may be controlled, for example, by use of ferrite bead or capacitive input means.

176 Located in an emitter-gate region:
This subclass is indented under subclass 175. Subject matter wherein the signal control mechanism is a transistor emitter junction with the gate region, and is used as the gate input.

177 With housing or external electrode:
This subclass is indented under subclass 107. Subject matter wherein the regenerative active junction type switching device includes a structure in which to place the device.

SEE OR SEARCH THIS CLASS, SUBCLASS:
81, and 82, for a light emitting device in combination with or constituting a light responsive device, with specific housing structure.
99, for light emitting device with specific housing structure.
433, and 434, for light responsive device with housing or encapsulation means.
573, for Darlington configuration bipolar transistor structure with housing or contact structure.
584, for enlarged emitter device bipolar transistor means having housing or contact.
602, for a voltage variable capacitance device with specified housing or contact.
660, for means to shield a device contained in a housing.

178 With means to avoid stress between electrode and active device (e.g., thermal expansion matching of electrode to semiconductor):
This subclass is indented under subclass 177. Subject matter wherein the device has electrode means connected to its terminals and is further provided with means to avoid creation of stress between the active device and the electrode means.

(1) Note. The means to avoid such stress may include means to thermally match the electrode to the semiconductor.

SEE OR SEARCH CLASS:
439, Electrical Connectors, subclasses 449+ for stress relief means for a conductor-to-terminal joint.

179 With malleable electrode (e.g., silver electrode layer):
This subclass is indented under subclass 178. Subject matter wherein the electrode means is soft and pliable.

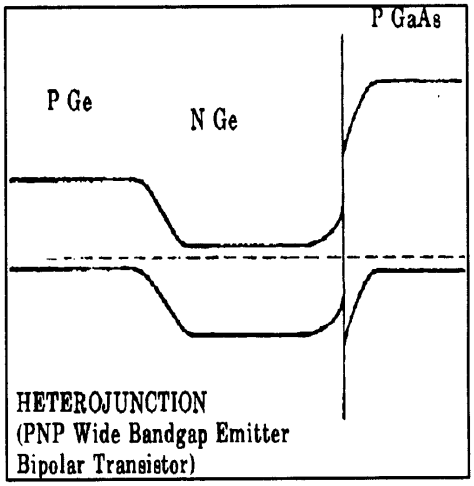
180 Stud mount:
This subclass is indented under subclass 177. Subject matter wherein the housing is provided with a threaded or serrated insert or post used for connecting heat sinks or terminals to the device.

181 With large area flexible electrodes in press contact with opposite sides of active semiconductor chip and surrounded by an insulating element, (e.g., ring):
This subclass is indented under subclass 177. Subject matter wherein the housing is provided with large area flexible electrodes in press contact with opposite sides of active semiconductor chip and surrounded by an insulating element (e.g., ring).

182 With lead feedthrough means on side of housing:
This subclass is indented under subclass 181. Subject matter wherein means are provided on a side of the housing through which electrical leads extending to or from the device can be located.

183 HETEROJUNCTION DEVICE:
This subclass is indented under the class definition. Subject matter wherein the active solid-state device contains a heterojunction, i.e., a boundary between different regions, one of which is made of a material that differs from that of the other region.

(1) Note. See illustration, below, for an example of a heterojunction bipolar transistor.



SEE OR SEARCH THIS CLASS, SUBCLASS:

10, and 11, for a heterojunction involving a low workfunction layer for electron emission.

12, through 27, for heterojunction devices which involve quantum well, superlattice or ballistic (hot carrier) transport devices.

51, for a non-single crystal material/monocrystal heterojunction device.

85, for a light emitting structure device combined with a light responsive device in an integrated structure wherein the light responsive device has a heterojunction.

90, for plural light emitting heterojunction devices.

94, through 97, for heterojunction light emitter structures.

183.1, for a heterojunction charge transfer device.

SEE OR SEARCH CLASS:

372, Coherent Light Generators, subclasses 43 through 50 for semiconductor lasers which may contain heterojunctions.

183.1 Charge transfer device:

This subclass is indented under subclass 183. Subject matter in which storage sites for packets of electric charge are induced at or below the surface of the active solid-state (semiconductor) device by an electric field applied to the device and wherein carrier potential energy per unit charge minima is established at a given storage site and such minima is transferred to one or more adjacent storage sites in a serial manner and which contains a junction between two semiconductor materials of different chemical compositions each different composition having a different carrier affinity.

(1) Note. Typically, heterojunctions are between materials which additionally have different band gaps, but that is not true of all heterojunctions.

SEE OR SEARCH THIS CLASS, SUBCLASS:

215, for charge transfer devices which do not involve heterojunctions.

184 Light responsive structure:

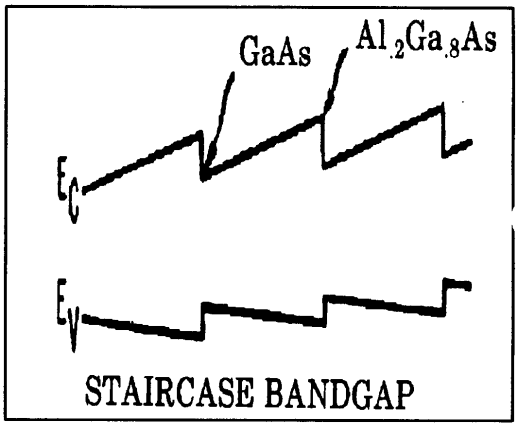
This subclass is indented under subclass 183. Subject matter wherein the heterojunction generates an electrical output when light impinges on it.

185 Staircase (including graded composition) device:

This subclass is indented under subclass 184. Subject matter wherein the active region contains a number of layers forming plural heterojunctions and the carrier (i.e., electron or hole) affinities of each layer incrementally increase or decrease progressively across the active region thickness, so that the energy level diagram of the active region, when under electrical bias, resembles a staircase.

(1) Note. Staircase effect devices may also be provided with a graded composition, i.e., wherein the chemical composition of the semiconductor forming the heterojunction varies in a direction either perpendicular or parallel to the junction.

(2) Note. See illustration, below, for an example of a staircase bandgap.



186 Avalanche photodetection structure:
This subclass is indented under subclass 184. Subject matter wherein carriers generated in the active region of the device in response to light incident thereupon, achieve enough kinetic energy to knock further carriers from the crystalline lattice of the active region producing an avalanche or snowball increase in operating current level.

(1) Note. Avalanche photodetector devices may have bipolar transistor structure, i.e., wherein the heterojunction device has three terminals - an emitter, a collector and a base, the operating current comprising both positive and negative electrical charges.

187 Having transistor structure:
This subclass is indented under subclass 184. Subject matter wherein the light responsive heterojunction device has three terminals - an emitter, collector, and a base; a source, drain, and gate; or a hybrid combination of each, which can provide gain or can be used as a switch.

188 Having narrow energy band gap (<<1eV) layer (e.g., PbSnTe, HgCdTe, etc.):
This subclass is indented under subclass 184. Subject matter wherein the light responsive device contains a narrow energy band gap (<<1eV) layer (e.g., PbSnTe or HgCdTe).

189 Layer is a group III-V semiconductor compound:
This subclass is indented under subclass 188. Subject matter wherein the narrow energy band gap layer is a semiconductor compound made of one element taken from periodic table group III elements and another element taken from periodic table group V elements.

190 With lattice constant mismatch (e.g., with buffer layer to accommodate mismatch):
This subclass is indented under subclass 183. Subject matter wherein at least one of the materials that form the heterojunction has a crystalline lattice constant which is made to differ from the lattice constant of the other material which forms the heterojunction.

(1) Note. Typically, lattice mismatches are sought to be avoided. However, sometimes they are desired, as for example, when the resulting strain favorably affects the properties of the strained semiconductor.

(2) Note. A buffer layer may be provided to accommodate a lattice mismatch, i.e., a layer of material which mechanically separates the layers which have different lattice constants.

SEE OR SEARCH THIS CLASS, SUBCLASS:
18, for strained layer heterojunctions in a superlattice.

191 Having graded composition:
This subclass is indented under subclass 183. Subject matter wherein the chemical composition of the semiconductor forming the heterojunction varies continuously in a direction either perpendicular or parallel to the junction.

192 Field effect transistor:
This subclass is indented under subclass 183. Subject matter wherein the heterojunction is part of a field effect transistor, i.e., wherein the current through the active heterojunction is controlled by a voltage applied between gate and source terminals of the device.

194 Doping on side of heterojunction with lower carrier affinity (e.g., high electron mobility transistor (HEMT)):
This subclass is indented under subclass 192. Subject matter wherein the heterojunction field effect transistor has impurity dopant on the side of the heterojunction with lower affinity for the charge carriers (holes or electrons) supplied by the dopant, so that the charge carriers spill over the heterojunction into the side with higher carrier affinity.

(1) Note. Typically, the spilled over charge carriers constitute the conductive channel connecting the source and drain electrodes.

(2) Note. Such devices may be provided with a channel layer of semiconductor material other than group III-V compound semiconductor (e.g., IV-VI compound semiconductor, germanium semiconductor, etc.).

SEE OR SEARCH THIS CLASS, SUBCLASS:
12, through 27, for other closely related quantum well and ballistic transport field effect devices.

195 Combined with diverse type device:
This subclass is indented under subclass 194. Subject matter wherein the heterojunction field effect transistor with impurity dopant on the side of the heterojunction with lower affinity for the charge carriers supplied by the dopant is combined with another electronic device.

(1) Note. Typical diverse devises include complementary field effect transistors, i.e., a field effect transistor of opposite conductivity type to the heterojunction field effect transistor; and field effect transistors of different threshold voltages (e.g., enhancement and depletion HEMTs in same integrated circuit).

196 Both semiconductors of the heterojunction are the same conductivity type (i.e., either n or p):
This subclass is indented under subclass 183. Subject matter wherein the semiconductor materials which define the heterojunction are of the same conductivity type (e.g., both p or both n).

197 Bipolar transistor:
This subclass is indented under subclass 183. Subject matter wherein the heterojunction is part of a bipolar transistor, i.e., a transistor structure whose working current passes through semiconductor material of both polarities (p and n) which form a heterojunction portion of the transistor.

SEE OR SEARCH CLASS:
438, Semiconductor Device Manufacturing: Process, particularly subclasses 312+ for methods of forming a heterojunction bipolar transistor.

198 Wide band gap emitter:
This subclass is indented under subclass 197. Subject matter wherein the bipolar transistor with an active heterojunction region involves a charge carrier emitter region made of a semiconductor material having an energy gap between its conduction and valence bands which is greater than the energy gap of the base region forming a heterojunction therewith.

199 Avalanche diode (e.g., so-called "Zener" diode having breakdown voltage greater than 6 volts, including heterojunction IMPATT type microwave diodes):
This subclass is indented under subclass 183. Subject matter wherein the heterojunction device is a diode in which conduction under reverse bias conditions is caused by avalanche breakdown at an applied voltage greater than 6 volts.

(1) Note. One example of such a device is a microwave transit time device (e.g., IMPATT diode).

SEE OR SEARCH THIS CLASS, SUBCLASS:
481, for a Schottky barrier avalanche diode.
551, for an avalanche diode used as a voltage reference element combined with pn junction isolation means in an integrated circuit.
603, through 606, for avalanche diodes not classified above those subclasses in this schedule, i.e., not involving a het-

erojunction in a non-charge transfer device, or a Schottky barrier, or one used as a voltage reference element with pn junction isolation means in an integrated circuit.

SEE OR SEARCH CLASS:
331, Oscillators, subclasses 107+ for solid-state active element oscillators.

200 Heterojunction formed between semiconductor materials which differ in that they belong to different periodic table groups (e.g., Ge (group IV) - GaAs (group III-V) or InP (group III-V) - CdTe (group II-VI)):
This subclass is indented under subclass 183. Subject matter wherein the heterojunction is formed between semiconductor materials which differ in that they belong to different periodic table groups (e.g., Ge (group IV) - GaAs (group III-V) or InP (group III-V) - CdTe (group II-VI)).

201 Between different group IV-VI or II-VI or III-V compounds other than GaAs/GaAlAs:
This subclass is indented under subclass 183. Subject matter wherein the heterojunction forms a boundary between different group IV-VI or group II-VI or group III-V compounds other than GaAs/GaAlAs.

202 GATE ARRAYS:
This subclass is indented under the class definition. Subject matter comprising a repeating geometric arrangement of individual structural units of solid-state devices, the solid-state devices of each individual structural unit being connectable into various different types of logic circuits in one integrated, monolithic chip.

(1) Note. The significant distinction between a “gate array” and other arrays of active solid state devices, such as read-only memories (ROMs), and programmable logic arrays (PLAs), is that the solid-state devices of each individual structural of a “gate array” can be connected into various different types of logic circuits, whereas in a ROM or PLA, each of the individual structural units is configured so that they must be connected into the same type of logic circuit (e.g., wherein all individual structural units are connected as NOR gates).

SEE OR SEARCH CLASS:
438, Semiconductor Device Manufacturing: Process, particularly subclasses 128+ for methods of forming an array of devices upon a semiconductor substrate and selectively interconnecting the same.

203 With particular chip input/output means:
This subclass is indented under subclass 202. Subject matter wherein the gate array integrated circuit is provided with specific means to input and output electrical signals to operate the device.

(1) Note. Examples of particular chip input/output means include (a) interface circuits, i.e., circuits that connect the chip to another device or to a circuit and which produces necessary current and voltage characteristics for the interconnected devices and circuits to function properly, with particular active solid-state devices used in the interface circuits; (b) structure permitting electrical interconnection to either receive an input signal or to output an output signal; or (c) specific bonding pad or electrode configurations (i.e., wherein the input/output means includes a particular electrically conductive surface to which electrical interconnecting element (e.g., electrical leads) can be connected, or has a specified electrode configuration such as a power supply bus for the input/output means separate from those used to power the gate array devices.

204 Having specific type of active device (e.g., CMOS):
This subclass is indented under subclass 202. Subject matter wherein the gate array is adapted to use a particular type of solid-state electronic device, e.g., complementary metal oxide semiconductor device (CMOS).

205 With bipolar transistors or with FETs of only one channel conductivity type (e.g., enhancement-depletion FETs):
This subclass is indented under subclass 202. Subject matter wherein the specific type of active device comprises bipolar transistors or FETs of only one channel conductivity type (i.e, field effect transistors that can be used in the enhancement or depletion mode of operation, e.g., IGFETS).

206 Particular layout of complementary FETs with regard to each other:
This subclass is indented under subclass 204. Subject matter wherein the CMOS device includes a plurality of CMOS field effect transistors specifically arranged with regard to each other.

207 With particular power supply distribution means:
This subclass is indented under subclass 202. Subject matter wherein the gate array is provided with specific means to provide electrical power to the array.

208 With particular signal path connections:
This subclass is indented under subclass 202. Subject matter wherein the gate array is provided with specific signal path connections.

209 Programmable signal paths (e.g., with fuse elements, laser programmable, etc):
This subclass is indented under subclass 208. Subject matter wherein the gate array is provided with means (e.g., fuse elements or laser beam irradiation) to program the selection of signal paths in the array.

210 With wiring channel area:
This subclass is indented under subclass 208. Subject matter wherein the signal paths in the array are located in an area separate from the active devices forming the elements of the array.

211 Multi-level metallization:
This subclass is indented under subclass 208. Subject matter wherein the particular signal path connections include more than one layer of conductive metal deposited on a substrate.

(1) Note. The multilayer metallization may include a layer of material made up of silicon in polycrystalline form or a silicide compound.

212 CONDUCTIVITY MODULATION DEVICE (E.G., UNIJUNCTION TRANSISTOR, DOUBLE-BASE DIODE, CONDUCTIVITY-MODULATED TRANSISTOR):
This subclass is indented under the class definition. Subject matter wherein the active solid-state device has a high resistivity semiconductor region of one conductivity type having a region of opposite conductivity type forming a pn junction with a central portion of the high resistivity layer, with structural means provided to forward bias the pn junction to inject minority carriers into the high resistivity region to increase its conductivity through conductivity modulation.

SEE OR SEARCH CLASS:

327, Miscellaneous Active Electrical Nonlinear Devices, Circuits, and Systems, subclasses 397 and 402 for a delay controlled switch using a unijunction transistor and having a variable or fixed delay respectively; subclasses 438+ for gating circuits utilizing a unijunction transistor, and subclass 569 for a miscellaneous circuit which utilizes a unijunction transistor.

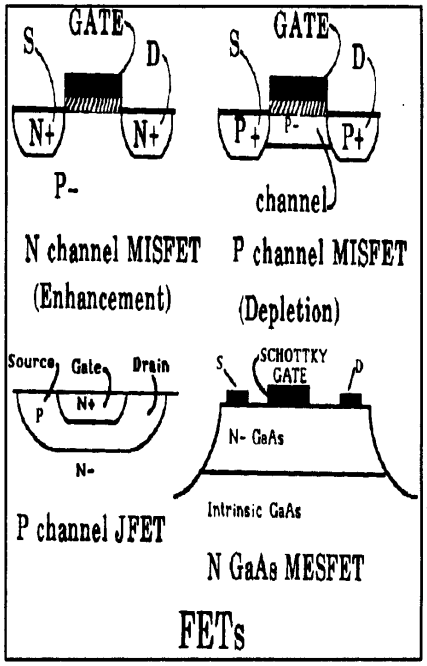
361, Electricity: Electrical Systems and Devices, subclass 91.3 for overvoltage protection with time delay, and subclass 198 for time delay with unijunction devices.

388, Electricity: Motor Control Systems, subclass 919 for unijunction transistor circuit trigger control means.

213 FIELD EFFECT DEVICE:
This subclass is indented under the class definition. Subject matter comprising a field effect transistor, in which the density of electrical charge (electrons or holes) in a semiconductor region is controlled by a voltage applied to an adjacent region or electrode which in operation is prevented from conducting direct electrical current to or from the semiconductor region by an insulator or barrier region.

(1) Note. The conduction of current in a field effect device is along a path called a channel.

(2) Note. See Illustration, below, for various types of field effect devices.



SEE OR SEARCH CLASS:

331, Oscillators, subclasses 116 and 117 for field effect transistor oscillator active elements.

341, Coded Data Generation or Conversion, subclass 136 for analog to or from digital conversion devices with a field effect transistor.

214 Charge injection device:

This subclass is indented under subclass 213. Subject matter wherein the field effect device is a device in which storage sites for packets of electric charge are induced at or below the surface of the active solid-state (semiconductor) device by an electric field applied to the device and wherein carrier potential energy per unit charge minima are established at a given storage site and such charge packets are injected into the device substrate or into a data bus.

(1) Note. This type device differs from a charge transfer device in that, in the latter, charge is transferred to adjacent charge storage sites in a serial manner whereas in the former, the charge is injected in a non-serial manner to the device substrate or a data bus.

215 Charge transfer device:

This subclass is indented under subclass 213. Subject matter in which storage sites for packets of electric charge are induced at or below the surface of the active solid-state (semiconductor) device by an electric field applied to the device and wherein carrier potential energy per unit charge minima are established at a given storage site and such minima are transferred to one or more adjacent storage sites in a serial manner.

SEE OR SEARCH THIS CLASS, SUBCLASS:

183.1, for heterojunction type charge transfer devices.

SEE OR SEARCH CLASS:

438, Semiconductor Device Manufacturing: Process, subclass 60 for methods of making a photo-responsive semiconductor integrated circuit having a charge transfer device combined with another electrical device, subclasses 75+ for methods of making a photoresponsive charge transfer device, and subclasses 144+ for methods of making a charge transfer device.

216 Majority signal carrier (e.g., buried or bulk channel, or peristaltic):

This subclass is indented under subclass 215. Subject matter wherein the transfer is by majority carriers of the semiconductor material, i.e., by electrons in n-type semiconductor material, and is by holes in p-type semiconductor material.

217 Having a conductive means in direct contact with channel (e.g., non-insulated gate):

This subclass is indented under subclass 216. Subject matter wherein an electrical conductor (e.g., electrode) directly contacts the channel

region of the charge transfer device (e.g., a non-insulated gate (control) electrode).

(1) Note. The conductive means in direct contact with the channel may be directly connected to the substrate.

(2) Note. The conductive means in direct contact with the channel may be made of metal, forming a Schottky contact with the semiconductor channel material, i.e., a metal-semiconductor junction.

218 High resistivity channel (e.g., accumulation mode) or surface channel (e.g., transfer of signal charge occurs at the surface of the semiconductor) or minority carriers at input (i.e., surface channel input):
This subclass is indented under subclass 216. Subject matter wherein the majority signal carrier charge transfer device has a channel made of relatively high electrical resistivity material, or where the transfer of signal charge takes place at the surface of the semiconductor, or where minority charge carriers are input into a surface channel, but majority carriers are input into the bulk or buried channel portion of the device.

219 Impurity concentration variation:
This subclass is indented under subclass 216. Subject matter wherein the majority signal carrier charge transfer device contains impurity dopant ions which vary in terms of concentration in all or part of the channel of the device.

(1) Note. The impurity dopant ion concentration may vary across the channel and channel substrate interface.

220 Vertically within channel (e.g., profiled):
This subclass is indented under subclass 219. Subject matter wherein the impurity dopant ion concentration in the channel of the device varies across the channel in a direction perpendicular to a main surface of the device, regardless of the orientation of the channel (e.g., parallel or perpendicular to a main surface of the device).

221 Along the length of the channel (e.g., doping variations for transfer directionality):
This subclass is indented under subclass 219. Subject matter wherein the impurity dopant ion concentration in the channel of the device varies along the length of the channel, whether the channel is horizontally or vertically oriented.

222 Responsive to non-electrical external signal (e.g., imager):
This subclass is indented under subclass 216. Subject matter wherein the majority signal carrier charge transfer device transfers charge from one charge storage device to another in response to a non-electric signal (e.g., light, pressure, etc.).

223 Having structure to improve output signal (e.g., antiblooming drain):
This subclass is indented under subclass 222. Subject matter wherein the non-external signal responsive device includes structural means, e.g., a drain element which reduces or eliminates optical blooming to improve the signal generated by the device in response to the non-electrical input signal.

224 Channel confinement:
This subclass is indented under subclass 216. Subject matter wherein the majority carrier charge transfer device has means to restrict the dimensions of the thin semiconductor conductive path region (charge transfer channel) between the source and drain of the device.

225 Non-electrical input responsive (e.g., light responsive imager, input programmed by size of storage sites for use as a read-only memory, etc.):
This subclass is indented under subclass 215. Subject matter wherein the means that creates charge to be transferred is non-electrical (e.g., light).

226 Sensor element and charge transfer device are of different materials or on different substrates (e.g., “hybrid”):
This subclass is indented under subclass 225. Subject matter wherein charge carriers generated in response to the non-electrical input are generated in material which is different than, or is located on a different substrate than, the

semiconductor material that contains the charge carrier storage sites.

227 With specified dopant (e.g., photoionizable, "extrinsic" detectors for infrared):
This subclass is indented under subclass 225. Subject matter wherein the non-electrical responsive device contains specific impurity dopants.

228 Light responsive, back illuminated:
This subclass is indented under subclass 225. Subject matter wherein the non-electrical input responsive device has two major opposed surfaces, the channel containing the charge carrier storage sites being at or below one surface, and wherein the device is responsive to light which is incident on the other major surface.

229 Having structure to improve output signal (e.g., exposure control structure):
This subclass is indented under subclass 225. Subject matter wherein the non-electrical input responsive device contains structural means to improve the electrical signal it generates in response to the non-electrical input signal.

(1) Note. The structural means to improve the output signal may control the amount of charge generated by light incident on the device which is transferred as output signal charge.

230 With blooming suppression structure:
This subclass is indented under subclass 229. Subject matter wherein the structural means to improve the output signal prevents spill over of a large amount of signal charge generated at a storage site which receives a non-electrical input signal of very high intensity to adjacent storage sites.

(1) Note. The antiblooming suppression structure may include a drain structure for removing charge from storage sites.

(2) Note. The antiblooming drain structure may be located in the device beneath storage sites rather than on its surface.

231 2-dimensional area architecture:
This subclass is indented under subclass 225. Subject matter wherein the device has a plurality of non-electrical input responsive means spread out over a two dimensional area, e.g., a matrix or array of such means.

(1) Note. One 2-dimensional architecture area may be provided for light imaging elements and a separate 2-dimensional architecture area may be provided for electrical signal storage elements.

(2) Note. The imaging element sites may also be charge transfer storage sites (e.g., frame transfer imaging device).

232 Having alternating strips of sensor structures and register structures (e.g., interline imager):
This subclass is indented under subclass 231. Subject matter wherein the 2-dimensional area architecture has alternate strips of sensor structures and charge transfer channels.

233 Sensors not overlaid by electrode (e.g., photodiodes):
This subclass is indented under subclass 232. Subject matter wherein the light responsive sensor elements do not have an electrode overlying them.

234 Single strip of sensors (e.g., linear imager):
This subclass is indented under subclass 225. Subject matter wherein the non-electrical input responsive device is in the form of a line of individual sensors.

(1) Note. The single strip of sensors may be combined with a structure forming readout registers, i.e., short term storage devices for accumulating charge packets generated by the sensors and for transferring charge packets to an amplifier or output device, and wherein the sensors are placed adjacent to the readout register structure.

(2) Note. The device may have plural readout register structures.

235 Electrical input:
This subclass is indented under subclass 215. Subject matter wherein the input to the charge transfer device to create the charge to be transferred is an electrical signal.

236 Signal applied to field effect electrode:
This subclass is indented under subclass 235. Subject matter wherein means is provided to apply an electrical signal to an electrode which has an electrical potential barrier between the electrode and the semiconductor material of the device (e.g., a MOS dielectric or Schottky contact or reverse-biased junction), as contrasted with an ohmic electrical contact to the semiconductor.

237 Charge-presetting/linear input type (e.g., fill and spill):
This subclass is indented under subclass 236. Subject matter wherein means is provided for the input signal to form a potential well, overfill it, drain away the excess charge and input the preset charge in the potential well into the channel.

238 Input signal responsive to signal charge in charge transfer device (e.g., regeneration or feedback):
This subclass is indented under subclass 235. Subject matter wherein means is provided to take charge from the output of a charge transfer device and put it back into the input electrode thereof or into the input electrode of a second charge transfer device.

239 Signal charge detection type (e.g., floating diffusion or floating gate non-destructive output):
This subclass is indented under subclass 215. Subject matter wherein means is provided to detect the amount of charge being transferred in the device.

(1) Note. The charge being transferred may be measured without destroying the charge, i.e., the charge packet remains intact.

(2) Note. The charge transfer device may have a region diffused with impurity ions not electrically connected to ground to detect the magnitude of charge being transferred in the device and to output a signal proportional to that sensed charge. This is known as a floating diffusion output device. One example of such a device is a floating diffusion amplifier (FDA).

(3) Note. The charge transfer device may have a control electrode not electrically connected to ground to detect the magnitude of charge being transferred in the device and to output a signal proportional to that sensed charge. This type device is known as a floating gate output device. One example of such a device is a floating gate amplifier (FGA). Devices with plural floating gate outputs include distributed floating gate amplifiers (DFGA).

240 Changing width or direction of channel (e.g., meandering channel):
This subclass is indented under subclass 215. Subject matter wherein the charge transfer path region changes its width or direction throughout all or part of the distance from source to drain electrode.

241 Multiple channels (e.g., converging or diverging or parallel channels):
This subclass is indented under subclass 215. Subject matter wherein the charge transfer device contains more than one channel for charge transfer path.

(1) Note. The channels may converge or diverge, i.e., they are not parallel to each other, but change direction either toward or away from each other along their length.

(2) Note. In such devices, the charge transfer path may lie in two different (e.g., orthogonal) directions.

(3) Note. The device may include two or more parallel channels (e.g., serial- parallel-serial) wherein the charge transfer takes place in different directions, but the device includes charge transfer paths that are parallel to each other.

242 Vertical charge transfer:
This subclass is indented under subclass 215. Subject matter wherein the charge transfer device is provided with structure for vertical charge transfer perpendicular to a main device surface.

243 Channel confinement:
This subclass is indented under subclass 215. Subject matter containing means (e.g., pn junctions or dielectric layers) to restrict the boundaries of the charge transfer path through the device.

(1) Note. Typical channel confinement means include use of (a) an electrically insulating medium; (b) a layer of silicon polymer material (polysilicon) used to reduce electric field interaction with charge to be transferred via the channel; or (c) an impurity ion located in the device substrate, i.e., in the material on which the device is fabricated (e.g., an implanted channel stop).

244 Comprising a groove:
This subclass is indented under subclass 215. Subject matter wherein a surface of the device includes an elongated indentation.

(1) Note. The location of the groove relative to the charge storage sites of the device is deliberately not specified in this definition.

245 Structure for applying electric field into device (e.g., resistive electrode, acoustic traveling wave in channel):
This subclass is indented under subclass 215. Subject matter including structure (e.g., electrodes) for applying electrical energy into the device.

(1) Note. Structure for applying electrical energy into the device is typically an electrode with a relatively high electrical resistance value.

246 Phase structure (e.g., doping variations to provide asymmetry for 2-phase operation; more than four phases or "electrode per bit"):
This subclass is indented under subclass 245. Subject matter including a plurality of gate regions or doping variation regions to permit unidirectional charge packet transfer by symmetrical or unsymmetrically phased electrical control signals applied to the device gate or gates.

(1) Note. The phase structure may be multiphase (e.g., 3-phase or 4-phase), i.e., with three sets or four sets of electrodes, respectively.

(2) Note. Search subclass 249, below, for 2-phase structure devices.

(3) Note. Means may also be provided to generate a traveling wave of non-electrical energy (e.g., acoustic energy) in the device.

247 Uniphase or virtual phase structure:
This subclass is indented under subclass 246. Subject matter wherein the device has one set of gates (control electrodes) or virtual phase structure.

248 2-phase:
This subclass is indented under subclass 246. Subject matter wherein the device has two sets of gate electrodes.

249 Electrode structures or materials:
This subclass is indented under subclass 245. Subject matter wherein the charge transfer device is provided with specified electrode structures or materials to apply electric field into the device.

250 Plural gate levels:
This subclass is indented under subclass 249. Subject matter wherein the electrode structures include more than one level of gate electrodes relative to a main surface of the device.

251 Substantially incomplete signal charge transfer (e.g., bucket brigade):
This subclass is indented under subclass 215. Subject matter wherein the charge transferred is less than the entire charge stored in the storage site from which it originates.

252 Responsive to non-optical, non-electrical signal:
This subclass is indented under subclass 213. Subject matter which produces an electrical output in response to an input which is other than optical or electrical.

253 Chemical (e.g., ISFET, CHEMFET):
This subclass is indented under subclass 252. Subject matter wherein the input is a chemical reaction or the presence of a particular chemical in close proximity to the field effect device.

254 Physical deformation (e.g., strain sensor, acoustic wave detector):
This subclass is indented under subclass 252. Subject matter wherein the input is a physical deformation.

SEE OR SEARCH THIS CLASS, SUBCLASS:
416, for acoustic wave responsive devices, generally.

255 With current flow along specified crystal axis (e.g., axis of maximum carrier mobility):
This subclass is indented under subclass 213. Subject matter wherein the field effect device employs current flow along a specified crystal axis, such as a (100) axis or a (311) axis.

256 Junction field effect transistor (unipolar transistor):
This subclass is indented under subclass 213. Subject matter wherein the field effect device is a junction field effect transistor, i.e., in which current flow through a thin channel of semiconductor material is controlled by an electric field applied to a control region or electrode in rectifying contact (i.e., a pn junction or Schottky barrier junction) with the semiconductor material of the channel, so that the depletion region extending into the channel from the rectifying contact reduces the thickness of the undepleted portion of the channel to reduce the current flow through the channel.

SEE OR SEARCH CLASS:
438, Semiconductor Device Manufacturing: Process, particularly subclasses 167+ for methods of forming a Schottky gate field effect device and subclasses 186+ for methods of forming a junction gate field effect device.

257 Light responsive or combined with light responsive device:
This subclass is indented under subclass 256. Subject matter wherein the JFET generates an electrical signal when light energy is incident upon it or is combined with a light responsive device.

258 In imaging array:
This subclass is indented under subclass 257. Subject matter wherein a plurality of light responsive JFETs or JFETs combined with a light responsive device are in the form of a one or two dimensional array (e.g., line or area array) for forming an image of an object, light from which is incident upon the array.

259 Elongated active region acts as transmission line or distributed active element (e.g., "transmission line" field effect transistor):
This subclass is indented under subclass 256. Subject matter including at least one elongated active region (source, gate, or drain) which transmits or distributes charge carriers.

(1) Note. When the impedance of an element at the operating frequency is due primarily to the parameters of the element itself, and in considering the inductance, capacitance, and resistance of the element they must be considered as mixed together and spread out along the element rather than being considered as separate discrete lumps or components as in the case of simple series and parallel circuits, the element may be said to have distributed parameters.

SEE OR SEARCH CLASS:
333, Wave Transmission Lines and Networks, appropriate subclasses for transmission lines or distributed elements, per se.
438, Semiconductor Device Manufacturing: Process, particularly subclasses 167+ for methods of forming a Schottky gate field effect device and subclasses 186+ for methods of forming a junction gate field effect device.

260 Same channel controlled by both junction and insulated gate electrodes, or by both

Schottky barrier and pn junction gates (e.g., "taper isolated" memory cell):
This subclass is indented under subclass 256. Subject matter including plural gate electrodes or regions, at least one of which is isolated from the channel by a rectifying junction and at least another of which is isolated from the channel by an insulating layer therebetween, or wherein one rectifying junction may be a metal-to-semiconductor (Schottky) type and the other a pn junction.

(1) Note. In such devices, the junction gate region may be free of direct electrical connection (e.g., "taper isolated" memory cell), i.e., wherein the JFET has at least one gate electrode region which is isolated from the channel by a rectifying junction and is not directly provided with an electrical connection or terminal.

261 Junction gate region free of direct electrical connection (e.g., floating junction gate memory cell structure):
This subclass is indented under subclass 256. Subject matter including at least one gate electrode region which is isolated from the channel by a rectifying junction and is not directly provided with an electrical connection or terminal.

(1) Note. This type of gate is a floating junction gate, as contrasted with a floating insulated gate.

(2) Note. See this class, subclass 315, for floating insulated gate field effect devices.

(3) Note. The floating gate region may capacitively store electrical charge and be used as a memory element.

262 Combined with insulated gate field effect transistor (IGFET):
This subclass is indented under subclass 256. Subject matter including a field effect transistor having a gate (control) electrode which is electrically insulated from the channel and other electrodes of the transistor.

(1) Note. The combined JFET and IGFET may be electrically connected so that the source or drain electrode of one FET is connected to the gate electrode of the other FET.

263 Vertical controlled current path:
This subclass is indented under subclass 256. Subject matter wherein the operating current of the JFET has a path perpendicular to a main surface of the JFET and is controlled by the gate electrode of the device.

264 Enhancement mode or with high resistivity channel (e.g., doping of $10^{15}cm^{-3}$ or less):
This subclass is indented under subclass 263. Subject matter wherein an increase in the magnitude of the gate bias voltage increases the operating current, only leakage current flows when the gate voltage is zero, and conduction does not begin until the gate voltage reaches a threshold value; or the JFET has a channel made of relatively high electrical resistivity, e.g., due to doping with impurity ions of 10^{15} cm^{-3} or less.

265 In integrated circuit:
This subclass is indented under subclass 263. Subject matter in a single monolithic semiconductor chip with other active and/or passive devices.

266 With multiple parallel current paths (e.g., grid gate):
This subclass is indented under subclass 263. Subject matter having plural paths for operating current flow, each of which is parallel with the other paths (e.g., having a gate electrode in the form of a matrix or grid).

267 With Schottky barrier gate:
This subclass is indented under subclass 266. Subject matter including a gate which is formed by a metal to semiconductor rectifying junction.

268 Enhancement mode:
This subclass is indented under subclass 256. Subject matter wherein an increase in the magnitude of the gate bias voltage increases the operating current, only leakage current flows when the gate voltage is zero, and conduction does not begin until the gate voltage reaches a threshold value.

269 With means to adjust barrier height (e.g., doping profile):
This subclass is indented under subclass 268. Subject matter including means to adjust the electronic height of the Schottky barrier gate junction, e.g., a profiled impurity dopant concentration.

270 Plural, separately connected, gates control same channel region:
This subclass is indented under subclass 256. Subject matter including more than one gate region or portion to control the same channel region, the regions being provided with separate electrical connections.

271 Load element or constant current source (e.g., with source to gate connection):
This subclass is indented under subclass 256. Subject matter structured to function as an electrical load element or a source of constant current, e.g., with a source to gate electrical connection.

272 Junction field effect transistor in integrated circuit:
This subclass is indented under subclass 256. Subject matter located in a single monolithic semiconductor chip with other active and/or passive devices.

273 With bipolar device:
This subclass is indented under subclass 272. Subject matter located in an integrated circuit with a device which operates using both positive and negative charge carriers.

(1) Note. An active solid-state electronic device that contains both bipolar and field effect transistors may be referred to as a BI-FET device.

274 Complementary junction field effect transistors:
This subclass is indented under subclass 272. Subject matter which is located in and integrated with an opposite conductivity type JFET, i.e., an N channel JFET together with a P channel JFET.

275 Microwave integrated circuit (e.g., microstrip type):
This subclass is indented under subclass 272. Subject matter structured to operate at microwave frequencies in an integrated circuit containing microwave components (e.g., microstrip transmission lines).

276 With contact or heat sink extending through hole in semiconductor substrate, or with electrode suspended over substrate (e.g., air bridge):
This subclass is indented under subclass 275. Subject matter containing a hole in the semiconductor substrate and an electrical contact or a heat dissipation means extending through the hole.

SEE OR SEARCH THIS CLASS, SUBCLASS:
522, for integrated circuit devices employing air isolation.

277 With capacitive or inductive elements:
This subclass is indented under subclass 275. Subject matter having passive elements with electrical inductance or capacitance.

278 With devices vertically spaced in different layers of semiconductor material (e.g., "3-dimensional" integrated circuit):
Subject matter under 272 wherein the JFET and other active and/or passive devices in that chip are located in mutually perpendicular planes in different layers of semiconductor device material.

279 Pn junction gate in compound semiconductor material (e.g., GaAs):
This subclass is indented under subclass 256. Subject matter including a pn junction gate formed in a semiconductor material that is a compound, e.g., GaAs, as contrasted to an elemental semiconductor such as silicon or germanium.

280 With Schottky gate:
This subclass is indented under subclass 256. Subject matter including a metal to semiconductor rectifying (i.e., Schottky barrier) gate electrode.

(1) Note. A Schottky barrier gate JFET is referred to commonly as a MESFET (METal-Semiconductor field effect transistor).

281 Schottky gate to silicon semiconductor:
This subclass is indented under subclass 280. Subject matter wherein the semiconductor material contacting the gate electrode material is made of silicon.

282 Gate closely aligned to source region:
This subclass is indented under subclass 280. Subject matter wherein the gate region is closely aligned with the source region.

SEE OR SEARCH THIS CLASS, SUBCLASS:
332, 346, 387, and 797, for other self-aligned gate devices.

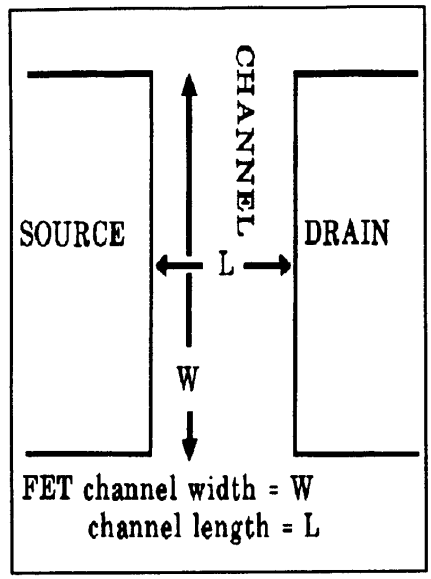
283 With groove or overhang for alignment:
This subclass is indented under subclass 282. Subject matter wherein the device has a groove or overhang for alignment of the gate and source regions.

284 Schottky gate in groove:
This subclass is indented under subclass 280. Subject matter wherein the MESFET has a groove in at least one of its surfaces and the Schottky gate is located therein.

285 With profiled channel dopant concentration or profiled gate region dopant concentration (e.g., maximum dopant concentration below surface):
This subclass is indented under subclass 256. Subject matter wherein the JFET has a variable impurity atom dopant concentration in the channel or gate region, e.g., wherein the maximum dopant concentration is located below the surface of the device, in either the channel or gate region.

286 With non-uniform channel thickness or width:
This subclass is indented under subclass 256. Subject matter wherein the channel has a non-uniform width or thickness (which lies in a plane perpendicular to both the channel length and width).

(1) Note. Channel length is measured along a line connecting the source and drain, while channel width is measured perpendicular to the length. Both length and width lie in a plane, parallel to the device surface. See the illustration, below.



287 With multiple channels or channel segments connected in parallel, or with channel much wider than length between source and drain (e.g., power JFET):
This subclass is indented under subclass 256. Subject matter including more than one channel or channel segments/portions which are electrically connected in parallel, or wherein the device has a channel whose width is much wider than the channel length, the channel length being the distance between the source and drain of the JFET.

SEE OR SEARCH THIS CLASS, SUBCLASS:
134+, for JFET devices, in general.
504, for JFET type isolation.

288 Having insulated electrode (e.g., MOSFET, MOS diode):
This subclass is indented under subclass 213. Subject matter including an electrode which is electrically insulated from the active semicon-

ductor region of the device (e.g., a metal oxide semiconductor insulated electrode).

(1) Note. Typically the insulated electrode is the control or gate electrode.

SEE OR SEARCH CLASS:
438, Semiconductor Device Manufacturing: Process, particularly subclasses 197+ for methods of forming an insulated gate field effect device.

289 Significant semiconductor chemical compound in bulk crystal (e.g., GaAs):
This subclass is indented under subclass 288. Subject matter wherein the insulated electrode field effect device contains a significant semiconductor chemical compound in a bulk (as contrasted with thin film) crystal (e.g., GaAs).

SEE OR SEARCH THIS CLASS, SUBCLASS:
1+, for bulk effect devices.

290 Light responsive or combined with light responsive device:
This subclass is indented under subclass 288. Subject matter which generates an electrical signal when light is incident on it or is combined with a light responsive device.

291 Imaging array:
This subclass is indented under subclass 290. Subject matter comprising a one or more dimensional array of light responsive devices which generate an electronic image of light from an object incident thereupon.

292 Photodiodes accessed by FETs:
This subclass is indented under subclass 291. Subject matter comprising light responsive diodes electrically coupled to field effect transistors.

293 Photoresistors accessed by FETs, or photodetectors separate from FET chip:
This subclass is indented under subclass 291. Subject matter comprising light responsive resistors coupled to field effect transistors.

294 With shield, filter, or lens:
This subclass is indented under subclass 291. Subject matter including means to shield the array from unwanted light, to filter light incident on the array, or to refract light incident on the array (e.g., to focus an image of an object on the array).

295 With ferroelectric material layer:
This subclass is indented under subclass 288. Subject matter including a layer of material which exhibits a spontaneous dipole moment.

296 Insulated gate capacitor or insulated gate transistor combined with capacitor (e.g., dynamic memory cell):
This subclass is indented under subclass 288. Subject matter wherein the device gate acts as a capacitor (i.e., wherein a positive potential placed on the gate electrode creates a negative charge on the other side of the insulator in the semiconductor material of the device, and vice versa) or the device is a transistor and it is combined with a capacitor.

SEE OR SEARCH CLASS:
438, Semiconductor Device Manufacturing: Process, particularly subclasses 239+ for methods of forming an insulated gate field effect transistor combined with a capacitor and subclasses 386 through 399 for manufacture of a capacitors, per se, utilizing a semiconductor substrate.

297 With means for preventing charge leakage due to minority carrier generation (e.g., alpha generated soft error protection or "dark current" leakage protection):
This subclass is indented under subclass 296. Subject matter wherein the device further includes means (1) to prevent electrical charge in the capacitor or capacitive type insulated gate region of the transistor to leak therefrom, or (2) to prevent excess leakage currents across pn junctions due to generation of minority carriers in the device for example (a) alpha particles incident on the device or (b) thermal generation of electron-hole pairs, or (c) minority carriers injected into the semiconductor substrate by other devices in the same substrate.

(1) Note. Junctions across which excess leakage is sought to be prevented typically include (a) the source or drain junction of an insulated gate field effect transistor or (b) a connecting BIT line of

a memory array which is isolated by a pn junction from a semiconductor substrate.

298 Capacitor for signal storage in combination with non-volatile storage means:
This subclass is indented under subclass 296. Subject matter including a capacitor to store an electrical signal in combination with charge storage means that can retain the charge even in the absence of operating power.

299 Structure configured for voltage converter (e.g., charge pump, substrate bias generator):
This subclass is indented under subclass 296. Subject matter including structure for use as a voltage converter (e.g., a device for changing AC to DC or vice versa, or for producing a negative DC voltage relative to a reference potential from a positive DC voltage relative to that reference potential).

300 Capacitor coupled to, or forms gate of, insulated gate field effect transistor (e.g., non-destructive readout dynamic memory cell structure):
This subclass is indented under subclass 296. Subject matter wherein the capacitor is electrically connected to or forms the gate of an insulated gate field effect transistor (IGFET), e.g., a non-destructive readout dynamic memory cell structure in which the charge state of the capacitor may be read out or determined by the conduction state of the field effect transistor, without discharging the capacitor in the readout process.

301 Capacitor in trench:
This subclass is indented under subclass 296. Subject matter wherein the capacitor is located in a recess in the semiconductor substrate.

302 Vertical transistor:
This subclass is indented under subclass 301. Subject matter combined with a vertical transistor (i.e., one in which the operating current flow is perpendicular to a main surface of the device).

303 Stacked capacitor:
This subclass is indented under subclass 301. Subject matter wherein the trench capacitor device contains a number of capacitor electrode regions stacked vertically above each other or wherein the capacitor and the transistor are located such that one overlies the other.

304 Storage node isolated by dielectric from semiconductor substrate:
This subclass is indented under subclass 301. Subject matter including an electrode upon which the charge varies as an indication of the memory state of the device (e.g., memory cell), and wherein the electrode is electrically isolated by a dielectric material from the semiconductor substrate of the device.

305 With means to insulate adjacent storage nodes (e.g., channel stops or field oxide):
This subclass is indented under subclass 301. Subject matter including means for electrically insulating an electrode upon which the charge varies as an indication of the memory state of the device (e.g., a memory cell).

(1) Note. The insulating means may, for example, comprise a channel stop or a field oxide.

306 Stacked capacitor:
This subclass is indented under subclass 296. Subject matter wherein the capacitor device contains a number of capacitor electrode regions overlying each other or where the capacitor and the transistor are located such that one overlies the other.

307 Parallel interleaved capacitor electrode pairs (e.g., interdigitized):
This subclass is indented under subclass 306. Subject matter wherein the number of overlying capacitor electrodes is more than one and the overlapping region of each capacitor electrode pair is made up of electrodes from one capacitor interleaved with the electrodes of another capacitor.

308 With capacitor electrodes connection portion located centrally thereof (e.g., fin electrodes with central post):
This subclass is indented under subclass 307. Subject matter wherein the capacitor electrodes are connected together at a centrally located portion thereof, e.g., by a center post.

309 With increased effective electrode surface area (e.g., tortuous path, corrugated, or textured electrodes):
This subclass is indented under subclass 306. Subject matter wherein a capacitor electrode has an increased effective surface relative to a flat capacitor plate, because of twists, turns, curves, corrugations, windings or other surface area increasing features of a capacitor electrode.

310 With high dielectric constant insulator (e.g., Ta_2O_5):
This subclass is indented under subclass 296. Subject matter wherein the capacitor device includes an insulating element which has a dielectric constant (e.g., Ta_2O_5) greater than 7.5, the dielectric constant of Si_3N_4.

311 Storage Node isolated by dielectric from semiconductor substrate:
This subclass is indented under subclass 296. Subject matter wherein the device has an electrode upon which the charge varies as an indication of the memory state of the device (e.g., memory cell) which electrode is electrically isolated by a dielectric material from the semiconductor substrate of the device.

312 Voltage variable capacitor (i. e., capacitance varies with applied voltage):
This subclass is indented under subclass 296. Subject matter wherein the device changes its capacitance depending on the amount of voltage applied thereto.

313 Inversion layer capacitor:
This subclass is indented under subclass 296. Subject matter wherein one plate of the capacitor device is a layer of minority carriers opposite in conductivity type to the doping of the semiconductor which are induced by applied voltage.

314 Variable threshold (e.g., floating gate memory device):
This subclass is indented under subclass 288. Subject matter wherein the device has a threshold voltage for current conduction which may be varied (e.g., by storage of charge in an insulator layer adjacent the channel in response to an electrical “write” signal).

SEE OR SEARCH THIS CLASS, SUBCLASS:
239, for a floating gate signal charge detection type charge transfer device.
261, for a floating gate JFET.

SEE OR SEARCH CLASS:
365, Static Information Storage and Retrieval, appropriate subclass for read/write static storage systems, and subclasses 185.01+ for predominate structure of floating gate memory storage (e.g., flash memory), particularly subclass 185.24 for threshold setting (e.g., conditioning).

315 With floating gate electrode:
This subclass is indented under subclass 314. Subject matter including a gate electrode which is free of direct electrical connection.

SEE OR SEARCH CLASS:
365, Static Information Storage and Retrieval, appropriate subclass for read/write static storage systems, and subclasses 185.01+ for predominate structure of floating gate memory storage (e.g., flash memory), particularly subclass 185.24 for threshold setting (e.g., conditioning).

316 With additional contacted control electrode:
This subclass is indented under subclass 315. Subject matter including an additional control (gate) electrode that has a direct electrical contact thereto.

317 With irregularities on electrode to facilitate charging or discharging of floating electrode:
This subclass is indented under subclass 316. Subject matter wherein the floating or additional control (gate) electrode has physical surface irregularities to facilitate charging or discharging of the floating gate electrode.

318 Additional control electrode is doped region in semiconductor substrate:
This subclass is indented under subclass 316. Subject matter wherein the additional control (gate) electrode is a specific region in the semiconductor substrate which is doped with impurity ions.

319 Plural additional contacted control electrodes:
This subclass is indented under subclass 316. Subject matter including more than one additional control (gate) electrode.

320 Separate control electrodes for charging and for discharging floating electrode:
This subclass is indented under subclass 319. Subject matter wherein the device has separate control (gate) electrodes for charging and discharging a floating electrode.

321 With thin insulator region for charging or discharging floating electrode by quantum mechanical tunneling:
This subclass is indented under subclass 316. Subject matter including a thin insulator region for charging of discharging a floating electrode by means of quantum mechanical tunneling of charge carriers.

SEE OR SEARCH THIS CLASS, SUBCLASS:
9, through 25, 28, and 30 through 39, for active solid-state devices involving this discrete layer type of quantum mechanical tunneling.

322 With charging or discharging by control voltage applied to source or drain region (e.g., by avalanche breakdown of drain junction):
This subclass is indented under subclass 316. Subject matter wherein the variable threshold device is structured to charge or discharge a floating gate electrode by a control voltage applied to source or drain region (e.g., by avalanche breakdown of drain junction).

323 With means to facilitate light erasure:
This subclass is indented under subclass 315. Subject matter including means to make erasure of the electrical charge content of the device by light easier (e.g., by providing an ultraviolet light window layer over the floating gate electrode to reduce absorption of erasing light).

324 Multiple insulator layers (e.g., MNOS structure):
This subclass is indented under subclass 314. Subject matter including more than one layer of electrically insulating material (e.g., metal-nitride-oxide (MNOS) semiconductor).

325 Non-homogeneous composition insulator layer (e.g., graded composition layer or layer with inclusions):
This subclass is indented under subclass 324. Subject matter wherein at least one layer has a non-homogeneous composition (e.g., a layer which varies in composition along at least one dimension thereof, or has inclusions of foreign material therein).

326 With additional, non-memory control electrode or channel portion (e.g., accessing field effect transistor structure):
This subclass is indented under subclass 324. Subject matter wherein the multiple insulator layer device has an additional, non-memory control electrode or channel portion, for example, for forming an accessing field effect transistor structure.

327 Short channel insulated gate field effect transistor:
This subclass is indented under subclass 288. Subject matter wherein the field effect device is an insulated gate field effect transistor with a short channel (i.e., one wherein the length of the channel is sufficiently short that the threshold voltage of the transistor depends on the length of the channel, or where the channel is specified to be less than 2 micrometers in length).

328 Vertical channel or double diffused insulated gate field effect device provided with means to protect against excess voltage (e.g., gate protection diode):
This subclass is indented under subclass 327. Subject matter wherein the short channel IGFET has a vertical current channel structure or the short channel IGFETs active channel region has a graded dopant concentration decreasing with distance from source region (e.g., double diffused, DMOS transistor) and wherein means are provided to protect the short channel against overvoltages (e.g., a gate insulator protection diode).

(1) Note. Gate protection diodes in IGFETs in general may be found in this class, subclass 355, and indented subclasses.

329 Gate controls vertical charge flow portion of channel (e.g., VMOS device):
This subclass is indented under subclass 327. Subject matter wherein the short channel IGFET has a channel portion in which charge flows in a substantially vertical direction and wherein the charge flowing therein is controlled by the gate electrode.

(1) Note. An IGFET's short channel may have horizontal as well as vertical charge flow portions. This subclass provides for those devices in which the vertical charge flow portion, i.e., the portion of the channel in which charge is flowing substantially in a vertical direction, of the channel is controlled by the gate.

330 Gate electrode in groove:
This subclass is indented under subclass 329. Subject matter wherein the gate controlled vertical channel device has a groove located therein and a gate electrode located in the groove.

331 Plural gate electrodes or grid shaped gate electrode:
This subclass is indented under subclass 330. Subject matter wherein there is more than one gate electrode located in a groove or wherein the gate electrode has a grid or mesh type shape.

332 Gate electrode self-aligned with groove:
This subclass is indented under subclass 330. Subject matter wherein the gate electrode is self-aligned with the groove.

SEE OR SEARCH THIS CLASS, SUBCLASS:
282, 283, 346, 387, and 797, for other self-aligned gate devices.

333 With thick insulator to reduce gate capacitance in non-channel areas (e.g., thick oxide over source or drain region):
This subclass is indented under subclass 330. Subject matter wherein the device with a gate electrode in a groove is provided with a thick insulator material layer to reduce gate capacitance in non-channel areas, e.g., a thick layer of oxide located over the source or drain region.

334 In integrated circuit structure:
This subclass is indented under subclass 330. Subject matter wherein the device is located in an integrated circuit structure.

335 Active channel region has a graded dopant concentration decreasing with distance from source region (e.g., double diffused device, DMOS transistor):
This subclass is indented under subclass 327. Subject matter wherein the short channel IGFET's active channel region has a graded dopant concentration decreasing with distance from source region, e.g., double diffused device or a DMOS transistor.

336 With lightly doped portion of drain region adjacent channel (e.g., LDD structure):
This subclass is indented under subclass 335. Subject matter wherein the graded channel doping short channel IGFET has a relatively light concentration of dopant in the portion of the drain region which lies adjacent to the current conducting channel.

337 In integrated circuit structure:
This subclass is indented under subclass 335. Subject matter wherein the graded channel doping short channel IGFET is contained in a single monolithic chip with other active or passive solid-state electronic devices.

338 With complementary field effect transistor:
This subclass is indented under subclass 337. Subject matter wherein the graded channel doping short channel IGFET is contained in a single monolithic chip with a field effect transistor with a polarity type opposite to that of the graded channel doping short channel IGFET.

339 With means to increase breakdown voltage:
This subclass is indented under subclass 335. Subject matter wherein the graded channel doping short channel IGFET includes means to increase the voltage that may be applied to the device without electrical breakdown of the device occurring.

340 With means (other than self-alignment of the gate electrode) to decrease gate capacitance (e.g., shield electrode):
This subclass is indented under subclass 335. Subject matter wherein the graded channel doping short channel IGFET has means (other than self-alignment of the gate electrode) (e.g., an shielding electrode) to decrease the capacitance of the gate electrode.

341 Plural sections connected in parallel (e.g., power MOSFET):
This subclass is indented under subclass 335. Subject matter wherein the graded channel doping short channel IGFET has more than one section and a plurality of those sections are connected electrically in parallel (e.g., to form a power MOSFET).

342 With means to reduce ON resistance:
This subclass is indented under subclass 341. Subject matter wherein the device further contains means to reduce the resistance of the device when it is conducting electricity, i.e., in the ON condition.

343 All contacts on same surface (e.g., lateral structure):
This subclass is indented under subclass 335. Subject matter wherein all electrical contacts of the device are located on the same external surface of the device, e.g., a lateral structure device.

344 With lightly doped portion of drain region adjacent channel (e.g., LDD structure):
This subclass is indented under subclass 327. Subject matter wherein the short channel IGFET has a lightly doped portion of the drain region adjacent channel (e.g., a lightly doped drain structure).

345 With means to prevent sub-surface currents, or with non-uniform channel doping:
This subclass is indented under subclass 327. Subject matter wherein the short channel IGFET contains means to prevent current from flowing below the surface of the device.

346 Gate electrode overlaps the source or drain by no more than depth of source or drain (e.g., self-aligned gate):
This subclass is indented under subclass 327. Subject matter wherein the short channel IGFET has a gate electrode which overlaps the source or drain or both by no more than the thickness of the depth of the source or drain (e.g., a self-aligned gate).

(1) Note. A self-aligned gate is one which is aligned between the source and drain via a masking process which uses the gate material itself to achieve the alignment.

SEE OR SEARCH THIS CLASS, SUBCLASS:
282, 283, 332, 387, and 797, for other self-aligned gate devices.

347 Single crystal semiconductor layer on insulating substrate (SOI):
This subclass is indented under subclass 288. Subject matter wherein the field effect device has a single crystal semiconductor layer located on a substrate made of electrically insulating material.

(1) Note. See this class, subclass 49, for active solid-state devices in non-single crystalline layers which may be on insulating substrates. See this class, subclass 506, for active devices in single crystal layers which are dielectrically isolated, but do not include field effect devices.

(2) Note. Material deposited as polycrystalline or amorphous and then recrystallized, as by a scanning laser beam, is considered to be non-single crystalline for purposes of determining classification between this subclass and subclass 49, since such recrystallization typically leaves residual grain boundaries and is thus large grained polycrystalline mate-

rial, rather than true single crystal material.

SEE OR SEARCH CLASS:

438, Semiconductor Device Manufacturing: Process, particularly subclasses 149+ for methods of forming a field effect transistor on an insulating substrate or layer (e.g., SOS, SOI, etc.).

348 Depletion mode field effect transistor:
This subclass is indented under subclass 347. Subject matter wherein the SOI device is a field effect transistor which operates in the depletion mode, i.e., a FET which passes maximum operating current with the gate to source biased to zero volts.

349 With means (e.g., a buried channel stop layer) to prevent leakage current along the interface of the semiconductor layer and the insulating substrate:
This subclass is indented under subclass 347. Subject matter wherein the SOI device includes means to prevent undesirable stray current to flow along the interface between the semiconductor layer and the insulating substrate.

(1) Note. The means to prevent this stray current may be, for example, a thin layer of doped semiconductor material for trapping charge /which would otherwise flow through a channel in the device.

350 Insulated electrode device is combined with diverse type device (e.g., complementary MOSFETs, FET with resistor, etc.):
This subclass is indented under subclass 347. Subject matter wherein the SOI device is combined with a different solid-state active or passive device, e.g., to form complementary MOSFETs or a FET combined with a resistor, etc.

351 Complementary field effect transistor structures only (i.e., not including bipolar transistors, resistors, or other components):
This subclass is indented under subclass 350. Subject matter wherein the field effect transistor and the diverse type device are field effect transistors which are complementary in conductivity type to each other (e.g., provide a CMOS structure).

352 Substrate is single crystal insulator (e.g., sapphire or spinel):
This subclass is indented under subclass 347. Subject matter wherein the SOI substrate is a single crystal insulator (e.g., sapphire or spinel).

353 Single crystal islands of semiconductor layer containing only one active device:
This subclass is indented under subclass 352. Subject matter wherein the single crystal insulator SOI substrate contains single crystal islands of semiconductor material, each island containing only one active solid-state device.

354 Including means to eliminate island edge effects (e.g., insulating filling between islands, or ions in island edges):
This subclass is indented under subclass 353. Subject matter wherein means are provided to eliminate deleterious effects caused by the edges of each island, such means including, for example, electrically insulating filling between islands, or channel stop regions located in the edges of islands.

355 With overvoltage protective means:
This subclass is indented under subclass 288. Subject matter wherein the device has means to protect it against applied voltage which exceeds that which the device can tolerate before being damaged.

356 For protecting against gate insulator breakdown:
This subclass is indented under subclass 355. Subject matter wherein the overvoltage protection means is structured to protect against electrical breakdown (shorting) of the gate insulator.

357 In complementary field effect transistor integrated circuit:
This subclass is indented under subclass 356. Subject matter wherein the device includes complementary field effect transistors located in a single monolithic chip.

358 Including resistor element:
This subclass is indented under subclass 357. Subject matter wherein the device includes an electrical resistor.

359 As thin film structure (e.g., polysilicon resistor):
This subclass is indented under subclass 358. Subject matter wherein the resistor is in the form of a thin film resistor (e.g., a polysilicon resistor).

360 Protection device includes insulated gate transistor structure (e.g., combined with resistor element):
This subclass is indented under subclass 356. Subject matter wherein the means for protecting against insulator breakdown is an insulated gate transistor structure.

361 For operation as bipolar or punchthrough element:
This subclass is indented under subclass 360. Subject matter wherein the insulated gate transistor structure protection device is configured to operate as a bipolar transistor or to conduct by punchthrough of a depletion region from one pn junction to another pn junction upon application of an overvoltage.

362 Punchthrough or bipolar element:
This subclass is indented under subclass 356. Subject matter wherein the means for protecting against insulator breakdown is a bipolar device or is configured to conduct by punchthrough of a depletion region from one pn junction to another pn junction upon application of an overvoltage.

363 Including resistor element:
This subclass is indented under subclass 356. Subject matter including an electrical resistive element.

364 With resistive gate electrode:
This subclass is indented under subclass 288. Subject matter including a gate (control) electrode which has high electrical resistivity.

365 With plural, separately connected, gate electrodes in same device:
This subclass is indented under subclass 288. Subject matter wherein the device has more than one gate (control) electrode, in the same device, with separate electrical connections to the plural gate (control) electrodes.

366 Overlapping gate electrodes:
This subclass is indented under subclass 365. Subject matter wherein at least one of the plural gate electrodes overlaps another gate electrode.

367 Insulated gate controlled breakdown of pn junction (e.g., field plate diode):
Subject matter under 288 including an electrically insulated gate electrode which is used to control the voltage applied to the device to cause breakdown of the pn junction.

368 Insulated gate field effect transistor in integrated circuit:
This subclass is indented under subclass 288. Subject matter wherein the device is an insulated gate field effect transistor located in a single monolithic semiconductor chip circuit.

369 Complementary insulated gate field effect transistors:
This subclass is indented under subclass 368. Subject matter wherein the device is made up of IGFETs that have opposite conductivity channels (p-type and n-type).

370 Combined with bipolar transistor:
This subclass is indented under subclass 369. Subject matter including at least one bipolar transistor.

(1) Note. An active solid-state electronic device that contains both bipolar and field effect transistors may be referred to as a BI-FET device.

371 Complementary transistors in wells of opposite conductivity types more heavily doped than the substrate region in which they are formed, e.g., twin wells:
This subclass is indented under subclass 369. Subject matter wherein the complementary IGFETs are located in wells of semiconductor material with electrical conductivity opposite to that of the respective transistors and wherein the wells contain a higher concentration of dopant ions than the semiconductor substrate in which they are located (e.g., twin wells).

372 With means to prevent latchup or parasitic conduction channels:
This subclass is indented under subclass 369. Subject matter including means to prevent conduction between regions of complementary IGFETs which form a (parasitic) regenerative structure which remains ON in the absence of a triggering signal.

(1) Note. For a definition of the regenerative structure of this subclass type, see subclass 107.

373 With pn junction to collect injected minority carriers to prevent parasitic bipolar transistor action:
This subclass is indented under subclass 372. Subject matter wherein the means for preventing latchup includes a pn junction for collecting minority carriers injected into the device to prevent operation of parasitic bipolar transistors which are otherwise capable of forming part of a parasitic regenerative switching structure.

374 Dielectric isolation means (e.g., dielectric layer in vertical grooves):
This subclass is indented under subclass 372. Subject matter wherein the means to prevent latchup includes means to dielectrically isolate the individual IGFETs from each other.

375 With means to reduce substrate spreading resistance (e.g., heavily doped substrate):
This subclass is indented under subclass 372. Subject matter wherein the means to prevent latchup includes means to reduce the electrical resistance of the substrate to reduce voltage differences between different parts of the substrate due to currents flowing therethrough.

376 With barrier region of reduced minority carrier lifetime (e.g., heavily doped P+ region to reduce electron minority carrier lifetime, or containing deep level impurity or crystal damage), or with region of high threshold voltage (e.g., heavily doped channel stop region):
This subclass is indented under subclass 372. Subject matter wherein the means to prevent latchup includes an electrical barrier region whose minority carrier lifetime is reduced from its normal value (e.g., by employing heavily doped P+ region to reduce electron minority carrier lifetime, or contains a deep level impurity or crystal damage) or has a region of high threshold voltage (e.g., a heavily doped channel stop region).

377 With polysilicon interconnections to source or drain regions (e.g., polysilicon laminated with silicide):
This subclass is indented under subclass 369. Subject matter wherein the device contains electrical interconnections to the source and/or drain regions of the IGFETs which are made of polycrystalline silicon (e.g., polysilicon laminated with a silicide).

378 Combined with bipolar transistor:
This subclass is indented under subclass 368. Subject matter wherein the IGFET is combined with a bipolar transistor in a single semiconductor chip.

(1) Note. An active solid-state electronic device that contains both bipolar and field effect transistors may be referred to as a BI-FET device.

379 Combined with passive components (e.g., resistors):
This subclass is indented under subclass 368. Subject matter wherein the IGFET is combined with passive electronic solid-state devices (e.g., resistors, inductors, transmission lines, etc.) in the integrated circuit.

380 Polysilicon resistor:
This subclass is indented under subclass 379. Subject matter wherein the device is combined with a resistor made of a polycrystalline form of silicon.

381 With multiple levels of polycrystalline silicon:
This subclass is indented under subclass 380. Subject matter wherein the integrated circuit has more than one layer of polycrystalline silicon.

382 With contact to source or drain region of refractory material (e.g., polysilicon, tungsten, or silicide):
This subclass is indented under subclass 368. Subject matter wherein the device has an electrical contact to its source region or drain

region wherein the contact is made of a refractory or platinum group metal, or of other material which has a melting point above that of the iron group of metals and which is resistant to heat (e.g., of polysilicon, tungsten or silicide).

(1) Note. Refractory materials include refractory metals and platinum group metals which include metals found in groups IVA, VA, VIA, or VIIIA (other than iron (Fe), nickel (Ni) or cobalt (Co)) of the periodic table of the elements.

383 Contact of refractory or platinum group metal (e.g., molybdenum, tungsten, or titanium):
This subclass is indented under subclass 382. Subject matter wherein the contact to the source or drain region is made of a refractory or platinum group metal (e.g., molybdenum, tungsten, or titanium).

384 Including silicide:
This subclass is indented under subclass 382. Subject matter wherein the contacts are made of a silicide.

385 Multiple polysilicon layers:
This subclass is indented under subclass 382. Subject matter wherein the refractory material contact to source or drain region includes more than one layer of polysilicon.

386 With means to reduce parasitic capacitance:
This subclass is indented under subclass 368. Subject matter wherein the device contains means to reduce unwanted capacitance between elements of the field effect transistor.

387 Gate electrode overlaps at least one of source or drain by no more than depth of source or drain (e.g., self-aligned gate):
This subclass is indented under subclass 386. Subject matter wherein the gate electrode overlaps at least one source or drain by no more than the depth of the source or the drain (e.g., self-aligned gate).

SEE OR SEARCH THIS CLASS, SUBCLASS:
282, 283, 328, 342, and 794, for other self-aligned gate devices.

388 Gate electrode consists of refractory or platinum group metal or silicide:
This subclass is indented under subclass 387. Subject matter wherein the gate electrode contains only refractory or platinum group metal (e.g., molybdenum, titanium or tungsten, or a silicide).

389 With thick insulator over source or drain region:
This subclass is indented under subclass 386. Subject matter wherein the means to reduce the parasitic capacitance is a thick insulating material layer located over the source or drain region.

390 Matrix or array of field effect transistors (e.g., array of FETs only some of which are completed, or structure for mask programmed read-only memory (ROM)):
This subclass is indented under subclass 368. Subject matter wherein the integrated circuit contains a two dimensional array of IGFETs, only some of which are completed devices, or the integrated circuit contains structure for a mask programmed read-only memory device.

391 Selected groups of complete field effect devices having different threshold voltages (e.g., different channel dopant concentrations):
This subclass is indented under subclass 390. Subject matter wherein selected groups of complete IGFETs have different threshold voltages above which the IGFETs will operate (e.g., different IGFETs have different current carrying channel impurity dopant concentrations).

392 Insulated gate field effect transistors of different threshold voltages in same integrated circuit (e.g., enhancement and depletion mode):
This subclass is indented under subclass 368. Subject matter wherein the IGFETs have different threshold voltages in the same integrated circuit (e.g., both enhancement and depletion mode IGFETs in the same integrated circuit).

393 Insulated gate field effect transistor adapted to function as load element for switching insulated gate field effect transistor:
This subclass is indented under subclass 368. Subject matter wherein the device is configured to function as a load element for another IGFET which is switched OFF and ON by signals applied thereto.

394 With means to prevent parasitic conduction channels:
This subclass is indented under subclass 368. Subject matter wherein the device includes means to prevent the formation of unwanted parasitic field effect transistor elements.

395 Thick insulator portion:
This subclass is indented under subclass 394. Subject matter wherein the means to prevent parasitic conduction channels from forming includes a thick insulator portion.

396 Recessed into semiconductor surface:
This subclass is indented under subclass 395. Subject matter wherein the thick insulator portion is recessed into the semiconductor device surface.

397 In vertical-walled groove:
This subclass is indented under subclass 396. Subject matter wherein the recessed thick isolator portion is in a groove in the surface of the overall device which extends perpendicular to the surface of the overall device.

398 Combined with heavily doped channel stop portion:
This subclass is indented under subclass 396. Subject matter wherein the device is combined with regions of heavy doping concentration.

399 Combined with heavily doped channel stop portion:
This subclass is indented under subclass 395. Subject matter wherein the device is combined with regions of heavy doping concentration.

400 With heavily doped channel stop portion:
This subclass is indented under subclass 394. Subject matter wherein the means to prevent parasitic conduction channels from forming comprises a region of heavy doping concentration.

401 With specified physical layout (e.g., ring gate, source/drain regions shared between plural FETs, plural sections connected in parallel to form power MOSFET):
This subclass is indented under subclass 368. Subject matter wherein the device has a specific physical configuration or layout (e.g., ring gate).

402 With permanent threshold adjustment (e.g., depletion mode):
This subclass is indented under subclass 288. Subject matter wherein the device includes means for permanently adjusting the threshold voltage at which the device conducts (e.g., depletion mode IGFETs).

403 With channel conductivity dopant same type as that of source and drain:
This subclass is indented under subclass 402. Subject matter wherein the device has a channel which is doped with impurity dopant to be the same conductivity type (n or p) as the source and drain.

404 Non-uniform channel doping:
This subclass is indented under subclass 403. Subject matter wherein the dopant concentration varies along at least one dimension of the channel.

405 With gate insulator containing specified permanent charge:
This subclass is indented under subclass 402. Subject matter wherein the device has a gate insulator with a specified permanent electrostatic charge therein.

406 Plural gate insulator layers:
This subclass is indented under subclass 405. Subject matter wherein the gate insulator is made up of a plurality of gate insulator layers.

407 With gate electrode of controlled workfunction material (e.g., low workfunction gate material):
This subclass is indented under subclass 402. Subject matter wherein the device has a gate electrode selected to have a controlled amount of minimum energy needed to be applied thereto to liberate an electron from its Fermi-level and send it into free space.

SEE OR SEARCH THIS CLASS, SUBCLASS:
10, and 11, for low workfunction material layer used for electron emission.

408 Including lightly doped drain portion adjacent channel (e.g., lightly doped drain, LDD device):
This subclass is indented under subclass 288. Subject matter wherein the device includes a drain portion adjacent the current channel which is lightly doped with impurities.

409 With means to increase breakdown voltage (e.g., field shield electrode, guard ring, etc.):
This subclass is indented under subclass 288. Subject matter wherein the device has means to increase the voltage that can be applied to the device without causing electrical breakdown of the device.

410 Gate insulator includes material (including air or vacuum) other than SiO_2:
This subclass is indented under subclass 288. Subject matter wherein the gate electrode insulator includes material other than silicon dioxide.

411 Composite or layered gate insulator (e.g., mixture such as silicon oxynitride):
This subclass is indented under subclass 410. Subject matter wherein the gate insulator is made of a composite material or layers of different materials.

412 Gate electrode of refractory material (e.g., polysilicon or a silicide of a refractory or platinum group metal):
This subclass is indented under subclass 288. Subject matter wherein the device has a gate electrode which is made of a refractory material (e.g., polysilicon or a silicide of a metal found in groups IVA, VA, VIA, or VIIIA (other than iron (Fe), nickel (Ni) or cobalt (Co)) of the periodic table of the elements.

413 Polysilicon laminated with silicide:
This subclass is indented under subclass 412. Subject matter wherein the refractory material is a laminate comprising at least one layer of polysilicon and one layer of a silicide.

414 RESPONSIVE TO NON-ELECTRICAL SIGNAL (E.G., CHEMICAL, STRESS, LIGHT, OR MAGNETIC FIELD SENSORS):
This subclass is indented under the class definition. Subject matter wherein the device generates an electrical signal in response to a non-electrical signal (e.g., light, heat, pressure) incident thereon.

415 Physical deformation:
This subclass is indented under subclass 414. Subject matter wherein the non-electrical signal incident upon the active solid-state device is a force which physically deforms the device.

SEE OR SEARCH CLASS:
438, Semiconductor Device Manufacturing: Process, particularly subclasses 50+ for methods of forming semiconductor devices which are responsive to physical deformation.

416 Acoustic wave:
This subclass is indented under subclass 415. Subject matter wherein the physically deforming force is in the form of a traveling vibration made up of sound energy.

SEE OR SEARCH THIS CLASS, SUBCLASS:
254, for field effect acoustic wave responsive devices.

417 Strain sensors:
This subclass is indented under subclass 415. Subject matter wherein the physically deforming force is that of an applied stress.

SEE OR SEARCH THIS CLASS, SUBCLASS:
254, for field effect strain sensor devices.

418 With means to concentrate stress:
This subclass is indented under subclass 417. Subject matter wherein the active solid-state device has means to concentrate the physically deforming stress.

419 With thinned central active portion of semiconductor surrounded by thick insensitive portion (e.g. diaphragm type strain gauge):
This subclass is indented under subclass 418. Subject matter wherein the means to concentrate the physically deforming stress is a thinned central active portion of semiconductor surrounded by a thick insensitive portion (e.g., a diaphragm type strain gauge).

420 Means to reduce sensitivity to physical deformation:
This subclass is indented under subclass 415. Subject matter wherein the device contains means to reduce the change in electrical output signal in response to physical deformation of the active junction.

421 Magnetic field:
This subclass is indented under subclass 414. Subject matter wherein the non-electrical signal to which the active solid-state device responds, is a magnetic field.

SEE OR SEARCH THIS CLASS, SUBCLASS:
108, for regenerative type magnetic field responsive devices

422 With magnetic field directing means (e.g., shield, pole piece, etc.):
This subclass is indented under subclass 421. Subject matter wherein means is provided for directing a magnetic field to the active solid-state device.

423 Bipolar transistor magnetic field sensor (e.g., lateral bipolar transistor):
This subclass is indented under subclass 421. Subject matter wherein the active solid-state device includes a bipolar transistor as the magnetic field sensor.

424 Sensor with region of high carrier recombination (e.g., magnetodiode with carriers deflected to recombination region by magnetic field):
This subclass is indented under subclass 421. Subject matter wherein the device has a region of high carrier recombination, e.g., a magnetodiode with carriers deflected to the recombination region by the magnetic field.

425 Magnetic field detector using compound semiconductor material (e.g., GaAs, InSb, etc.):
This subclass is indented under subclass 421. Subject matter wherein the device is made of a compound semiconductor material (e.g., GaAs, InSb, etc.).

426 Differential output (e.g., with offset adjustment means or with means to reduce temperature sensitivity):
This subclass is indented under subclass 421. Subject matter wherein the device has two output terminals and the electrical signal generated by the active solid-state device is the electrical signal difference between the outputs.

427 Magnetic field sensor in integrated circuit (e.g., in bipolar transistor integrated circuit):
This subclass is indented under subclass 421. Subject matter wherein the device is located in an integrated circuit (i.e., a solid monolithic semiconductor chip).

428 Electromagnetic or particle radiation:
This subclass is indented under subclass 414. Subject matter wherein the electrical signal is generated by the device in response to radiant energy in the electromagnetic energy spectrum or in the form of neutral or charged particles (e.g., alpha or beta particles).

429 Charged or elementary particles:
This subclass is indented under subclass 428. Subject matter wherein the particle energy is in the form of electrically charged or elementary particles (e.g., alpha or beta particles).

430 With active region having effective impurity concentration less than 10^{12} atoms/cm^3:
This subclass is indented under subclass 429. Subject matter wherein the active region of the device has an effective impurity ion dopant concentration less than 10^{12} atoms/cm^3.

431 Light:
This subclass is indented under subclass 428. Subject matter wherein the non-electrical signal to which the device responds is electromagnetic energy in the light frequency/wavelength

range (i.e., from infrared (except where the response is mainly due to thermal heating due to the infrared radiation) to visible and ultraviolet).

SEE OR SEARCH THIS CLASS, SUBCLASS:

21, for light responsive superlattice quantum well heterojunction tunneling devices.

53, through 56, for amorphous semiconductor junction material devices which are responsive to non-electrical (e.g., light) signals.

80, through 85, for light emitters combined with or also constituting a light responsive device.

113, through 118, for light activated regenerative type devices.

184, through 189, for light responsive heterojunction devices in non-charge transfer devices.

225, through 234, for charge transfer devices with non-electrical (e.g., light) input.

257, through 258, for light responsive JFET devices.

290, through 294, for light responsive insulated electrode field effect devices.

SEE OR SEARCH CLASS:

438, Semiconductor Device Manufacturing: Process, particularly subclasses 54+ for methods of making a temperature responsive semiconductor device.

432 With optical element:
This subclass is indented under subclass 431. Subject matter wherein the light incident upon the active region passes through an optical element (e.g., a fiber, lens, filter, etc.).

433 With housing or encapsulation:
This subclass is indented under subclass 431. Subject matter wherein means is provided to physically protect the device in the form of a housing or medium which embeds the device.

434 With window means:
This subclass is indented under subclass 433. Subject matter with means to optically couple the light to the device through a transparent window.

435 With optical shield or mask means:
This subclass is indented under subclass 431. Subject matter with means to spatially or temporally block all or part of the light incident on the portions of the device receptor region, other than the intended region.

436 With means for increasing light absorption (e.g., redirection of unabsorbed light):
This subclass is indented under subclass 431. Subject matter with means for increasing the amount of light absorbed by the device (e.g., antireflection coatings applied to the device, doping with energy converters, providing reflectors to redirect initially unabsorbed light onto the receptor, etc.).

437 Antireflection coating:
This subclass is indented under subclass 436. Subject matter wherein the means for increasing light absorption by the junction is a coating applied to the device which reduces reflection of the incident light (e.g., by use of interference films).

438 Avalanche junction:
This subclass is indented under subclass 431. Subject matter wherein the device has a junction which is operated in the avalanche portion of its operating curve to utilize the avalanche multiplication of photocurrent by means of hole-electron pairs created by absorbed photons.

(1) Note. When the reverse bias voltage applied to the device approaches breakdown level, the holes or electrons collide with substrate atoms to produce an avalanche of hole-electron pairs.

439 Containing dopant adapted for photoionization:
This subclass is indented under subclass 431. Subject matter wherein the junction region is provided with impurity dopant atoms which are only ionized to produce free carriers by the incident light.

440 With different sensor portions responsive to different wavelengths (e.g., color imager):
This subclass is indented under subclass 431. Subject matter wherein the device has different portions, some of which respond to different wavelengths of light than do others.

441 Narrow band gap semiconductor (<<1eV) (e.g., PbSnTe):
This subclass is indented under subclass 431. Subject matter wherein the device contains a semiconductor material which has a gap between its conduction and valence bands which is less than one electron volt.

442 II-VI compound semiconductor (e.g., HgCdTe):
This subclass is indented under subclass 441. Subject matter wherein the narrow band gap semiconductor is a compound semiconductor taken from columns II and VI of the periodic table.

443 Matrix or array (e.g., single line arrays):
This subclass is indented under subclass 431. Subject matter wherein the device is in the form of regularly spaced individual light responsive elements.

444 Light sensor elements overlie active switching elements in integrated circuit (e.g., where the sensor elements are deposited on an integrated circuit):
This subclass is indented under subclass 443. Subject matter wherein the active switching elements are in a monolithic chip which is combined with an array of light responsive elements which overlie the former.

445 With antiblooming means:
This subclass is indented under subclass 443. Subject matter with means to prevent more than one individual light responsive element from being activated by a very bright spot of light incident on a point of the matrix or array.

(1) Note. The anti-blooming means may drain charge from adjacent individual array elements to some other area, e.g., the substrate. This is known as an overflow drain.

446 With specific isolation means in integrated circuit:
This subclass is indented under subclass 443. Subject matter wherein the matrix or array of devices is provided with means to electrically isolate the device from other devices and the overall device is contained in a monolithic semiconductor chip.

447 With backside illumination (e.g., having a thinned central area or a non-absorbing substrate):
This subclass is indented under subclass 443. Subject matter wherein the matrix or array device is structured to permit incident light to reach the receptor region from the backside of the device.

448 With particular electrode configuration:
This subclass is indented under subclass 443. Subject matter wherein the matrix or array device has a particular electrode arrangement.

449 Schottky barrier (e.g., a transparent Schottky metallic layer or a Schottky barrier containing at least one of indium or tin (e.g., SnO_2, indium tin oxide)):
This subclass is indented under subclass 431. Subject matter wherein the device has a rectifying junction which is formed between a metal and a semiconductor material (i.e., a Schottky barrier).

(1) Note. The Schottky barrier may, for example, be transparent or contain indium or tin (e.g., SnO_2, indium tin oxide).

450 With doping profile to adjust barrier height:
This subclass is indented under subclass 449. Subject matter wherein the height of the Schottky barrier is changed by varying the concentration of the impurity dopant in the semiconductor portion of the active junction region of the device.

451 Responsive to light having lower energy (i.e., longer wavelength) than forbidden band gap

energy of semiconductor (e.g., by excitation of carriers from metal into semiconductor):
This subclass is indented under subclass 449. Subject matter wherein the device responds to light having lower energy than the energy difference between the bottom of the conduction band and the top of the valance band of the semiconductor material that forms a junction with the metal.

(1) Note. One way to achieve this result is to photoelectrically excite electrons from the metal adjacent the semiconductor into the semiconductor.

452 With edge protection, e.g., doped guard ring or mesa structure:
This subclass is indented under subclass 449. Subject matter wherein means is provided to reduce electric field concentration or breakdown at edges of the metal and semiconductor.

453 With specified Schottky metallic layer:
This subclass is indented under subclass 449. Subject matter wherein the device includes a layer of metal which has a specified chemical composition.

454 Schottky metallic layer is a silicide:
This subclass is indented under subclass 453. Subject matter wherein the specified Schottky material layer is a compound of metal and silicon.

455 Silicide of Platinum group metal:
This subclass is indented under subclass 454. Subject matter wherein the Schottky layer is a silicide of a metal found in the period table listed as a platinum group metal (i.e., ruthenium, rhodium, palladium, osmium, iridium, and platinum).

456 Silicide of refractory metal:
This subclass is indented under subclass 454. Subject matter wherein the Schottky layer comprises a silicide of the refractory metals (i.e., W, Ti, Ta, Hf, Zr, V, Nb, Mo, and Cr).

457 With particular contact geometry (e.g., ring or grid):
This subclass is indented under subclass 449. Subject matter wherein the device has a specific geometrical arrangement of electrical contacts.

458 PIN detector, including combinations with non-light responsive active devices:
This subclass is indented under subclass 431. Subject matter wherein the device has a pn junction with an intrinsic semiconductor material region (i.e., one with no deliberate impurity dopants) portion between the p- and n-impurity doped regions.

459 With particular contact geometry (e.g., ring or grid, or bonding pad arrangement):
This subclass is indented under subclass 431. Subject matter wherein the device has a specified electrical contact geometry.

460 With backside illumination (e.g., with a thinned central area or non-absorbing substrate):
This subclass is indented under subclass 431. Subject matter wherein the device is structured to permit incident light to reach the receptor portion from the backside of the device.

461 Light responsive pn junction:
This subclass is indented under subclass 431. Subject matter wherein the device has a junction between p-type and n-type material which responds to light incident upon it by generating a signal proportional thereto.

462 Phototransistor:
This subclass is indented under subclass 461. Subject matter wherein the pn junction device is a transistor wherein the device generates an electrical signal in response to light incident on the transistor.

463 With particular doping concentration:
This subclass is indented under subclass 461. Subject matter wherein the pn junction has a particular impurity dopant concentration or spatial distribution.

464 With particular layer thickness (e.g., layer less than light absorption depth):
This subclass is indented under subclass 461. Subject matter wherein the thickness of the junction region is of a specified thickness (e.g., less than the thickness in which light is absorbed).

465 Geometric configuration of junction (e.g., fingers):
This subclass is indented under subclass 461. Subject matter wherein the junction has a specified geometrical configuration (e.g., finger shaped).

466 External physical configuration of semiconductor (e.g., mesas, grooves):
This subclass is indented under subclass 431. Subject matter wherein the device has a specified external configuration (e.g., with mesas).

467 Temperature:
This subclass is indented under subclass 414. Subject matter wherein the non-electrical signal to which the device responds is thermal energy.

(1) Note. Infrared energy incident on the active junction which does not cause significant thermal heating of the device is classified in subclass 431.

SEE OR SEARCH CLASS:
438, Semiconductor Device Manufacturing: Process, particularly subclasses 54+ for methods of making a temperature responsive semiconductor device.

468 Semiconductor device operated at cryogenic temperature:
This subclass is indented under subclass 467. Subject matter wherein means are provided to cool the device for operation at cryogenic levels (e.g., below 100 degrees Kelvin).

469 With means to reduce temperature sensitivity (e.g., reduction of temperature sensitivity of junction breakdown voltage by using a compensating element):
This subclass is indented under subclass 467. Subject matter wherein means are provided to reduce the sensitivity of the electrical output of the device to changes in temperature of the device.

470 Pn junction adapted as temperature sensor:
This subclass is indented under subclass 467. Subject matter wherein the active junction is a pn junction (i.e., forms a boundary between p-type and n-type carrier materials) and generates an electrical signal in response to thermal energy incident upon the active junction.

471 SCHOTTKY BARRIER:
This subclass is indented under the class definition. Subject matter wherein the device contains a Schottky barrier (i.e., a rectifying interface between a semiconductor material and a metal).

SEE OR SEARCH THIS CLASS, SUBCLASS:
54, for Schottky barrier to amorphous semiconductor material device.
73, for Schottky barrier to polycrystalline semiconductor material device.
155, for a regenerative type switching device with switching speed enhancement means (e.g., a Schottky contact).
260, for JFET having the same channel controlled by, for example, Schottky barrier and PN junction gates.
280, through 284, for JFETs with a Schottky gate electrode.
449, through 457, for a light responsive device with a Schottky barrier.
928, for a shorted pn or Schottky junction device.

SEE OR SEARCH CLASS:
438, Semiconductor Device Manufacturing: Process, particularly subclasses 570+ for methods of forming a rectifying (Schottky) contact to a semiconductor.

472 To compound semiconductor:
This subclass is indented under subclass 471. Subject matter wherein the Schottky metal is interfaced with a compound semiconductor.

473 With specified Schottky metal:
This subclass is indented under subclass 472. Subject matter wherein the Schottky metal interfaced with the compound semiconductor is specifically claimed.

474 As active junction in bipolar transistor (e.g., Schottky collector):
This subclass is indented under subclass 471. Subject matter wherein the Schottky barrier junction is used as an active bipolar transistor junction (e.g., a Schottky collector).

475 With doping profile to adjust barrier height:
This subclass is indented under subclass 471. Subject matter wherein the difference in electrical potential from one side of an active junction to the other has been adjusted by a distribution of impurity dopant in the semiconductor adjacent the Schottky junction.

476 In integrated structure:
This subclass is indented under subclass 471. Subject matter wherein the Schottky barrier device is located in a single monolithic integrated semiconductor chip.

477 With bipolar transistor:
This subclass is indented under subclass 476. Subject matter wherein the Schottky barrier device is located in a single integrated monolithic semiconductor chip with a bipolar transistor.

478 Plural Schottky barriers with different barrier heights:
This subclass is indented under subclass 477. Subject matter wherein the integrated circuit containing a Schottky barrier device contains more than one Schottky barrier with different potential differences existing across the different barriers.

479 Connected across base-collector junction of transistor (e.g., Baker clamp):
This subclass is indented under subclass 477. Subject matter wherein a Schottky barrier device is electrically connected across the base-collector junction of a bipolar transistor.

480 In voltage variable capacitance diode:
This subclass is indented under subclass 471. Subject matter wherein the Schottky barrier is used in a variable capacitance diode (e.g., "varactor").

481 Avalanche diode (e.g., so-called "Zener" diode having breakdown voltage greater than 6 volts):
This subclass is indented under subclass 471. Subject matter wherein the Schottky barrier is in a device designed to operate in avalanche breakdown.

SEE OR SEARCH THIS CLASS, SUBCLASS:

199, for an avalanche diode in a non-charge transfer device having a heterojunction.

551, for an avalanche diode used as a voltage reference element combined with pn junction isolation means in an integrated circuit.

603, through 606, for avalanche diodes not classified above those subclasses in this schedule, i.e., not involving a heterojunction in a non-charge transfer device, or a Schottky barrier, or one used as a voltage reference element with pn junction isolation means in an integrated circuit.

482 Microwave transit time device (e.g., IMPATT diode):
This subclass is indented under subclass 481. Subject matter wherein the avalanche breakdown provides a power oscillation in the microwave region.

483 With means to prevent edge breakdown:
This subclass is indented under subclass 471. Subject matter wherein the Schottky barrier device has means which help to reduce the electrical field around the edge of the device.

484 Guard ring:
This subclass is indented under subclass 483. Subject matter wherein the means to prevent edge breakdown is a guard ring (e.g., a pn junction surrounding the periphery of the Schottky metal).

485 Specified materials:
This subclass is indented under subclass 471. Subject matter wherein the Schottky barrier device uses a material of specified composition.

486 Layered (e.g., a diffusion barrier material layer or a silicide layer or a precious metal layer):
This subclass is indented under subclass 485. Subject matter wherein the material, e.g., metal, which forms the Schottky barrier is comprised of layers, for example, a diffusion barrier material layer or a silicide layer or a precious metal layer.

487 WITH MEANS TO INCREASE BREAKDOWN VOLTAGE THRESHOLD:
This subclass is indented under the class definition. Subject matter wherein the device is provided with means to increase the voltage that may be applied thereto without causing electrical breakdown.

488 Field relief electrode:
This subclass is indented under subclass 487. Subject matter wherein the means to increase breakdown voltage comprises an electrode insulated from the semiconductor material of the active solid-state device, and configured so as to reduce the electric field strength at a given voltage applied to the device.

489 Resistive:
This subclass is indented under subclass 488. Subject matter wherein the field relief electrode is a high resistance layer adapted to have a current flow therethrough and a corresponding voltage variation therein.

490 Combined with floating pn junction guard region:
This subclass is indented under subclass 488. Subject matter wherein the means for increasing breakdown voltage includes, in addition to a field relief electrode, a floating pn junction guard region, i.e., a region free of direct electrical connection located in the material forming one side of an active pn, or other rectifying semiconductor junction, which region forms a pn junction with the material of the one side of the active junction, the guard region being spaced from the active junction, but sufficiently close thereto that the reverse bias depletion region from the active junction can reach the guard junction, whereby the guard junction modifies the shape of the depletion region from the active junction thus lowering the electric field intensity at a given applied reverse voltage across the active junction.

491 In integrated circuit:
This subclass is indented under subclass 487. Subject matter wherein the device with means to increase breakdown voltage is combined in a unitary monolithic semiconductor chip with other active or passive electronic devices.

(1) Note. The means for increasing breakdown voltage in the integrated circuit active device may include a floating pn junction guard region, that is, a region, free of direct electrical connection, located in the material forming one side of an active pn or other rectifying semiconductor junction, which region forms a pn junction with the material of the one side of the active junction, the guard region being spaced from the active junction but sufficiently close thereto that the reverse bias depletion region from the active junction can reach the guard junction, whereby the guard junction modifies the shape of the depletion region from the active junction thus lowering the electric field intensity at a given applied reverse voltage across the active junction.

(2) Note. The means for increasing the breakdown voltage of the integrated circuit device may include a semiconductor surface portion having a physical configuration, such as a bevel or mesa, to reduce electric field strength at a given applied voltage. Typically, the physical configuration will be such that the depletion region from a reverse biased junction in the active device reaches the physically configured surface and is forced by the shape of the surface to spread wider at a given applied reverse voltage than it would otherwise, thus reducing the electric field strength in the depletion layer.

492 With electric field controlling semiconductor layer having a low enough doping level in relationship to its thickness to be fully depleted prior to avalanche breakdown (e.g., RESURF devices):
This subclass is indented under subclass 491. Subject matter wherein the means to increase breakdown voltage of the device includes a layer of semiconductor material having a sufficiently low doping concentration that it may be fully depleted by the depletion region of a reverse biased junction of the active device prior to avalanche breakdown of the active device, so that upon depletion of the layer of semiconductor material, the effective width of

the depletion layer of the reverse biased junction of the active device is greatly expanded, thus resulting in smaller increases in electric field intensity with further increases of reverse voltage.

(1) Note. Devices provided with such a layer are sometimes called "RESURF" (Reduced SURFace Field) devices.

(2) Note. In silicon, to be fully depleted without avalanche breakdown, a layer must typically have an integrated doping density (the line integral of doping density along a path through the thickness of the layer) of less than $2x10^{12}$ dopant atoms/cm^2. The critical integrated doping density varies depending on the properties of the particular semiconductor material.

493 With electric field controlling semiconductor layer having a low enough doping level in relationship to its thickness to be fully depleted prior to avalanche breakdown (e.g., RESURF devices):
This subclass is indented under subclass 487. Subject matter wherein the means to increase breakdown voltage of the device includes a layer of semiconductor material having a sufficiently low doping concentration that it may be fully depleted by the depletion region of a reverse biased junction of the active device prior to avalanche breakdown of the active device, so that upon depletion of the layer of semiconductor material, the effective width of the depletion layer of the reverse biased junction of the active device is greatly expanded, thus resulting in smaller increases in electric field intensity with further increases of reverse voltage.

494 Reverse-biased pn junction guard region:
This subclass is indented under subclass 487. Subject matter wherein the means for increasing breakdown voltage in the device includes a reverse biased pn junction guard region, that is, a region located in the material forming one side of an active pn or other rectifying semiconductor junction, which region forms a pn junction with the material of the one side of the active junction, the guard region being adapted to be reverse biased with respect to the material forming one side of the active junction, and being spaced from the active junction, but sufficiently close thereto that the reverse bias depletion region from the active junction can reach the depletion region from the reverse biased guard junction, whereby the depletion region of the guard junction modifies the shape of the depletion region from the active junction thus lowering the electric field intensity at a given applied reverse voltage across the active junction.

495 Floating pn junction guard region:
This subclass is indented under subclass 487. Subject matter wherein the means for increasing breakdown voltage in the device includes a floating pn junction guard region, that is, a region, free of direct electrical connection, located in the material forming one side of an active pn or other rectifying semiconductor junction, which region forms a pn junction with the material of the one side of the active junction, the guard region being spaced from the active junction, but sufficiently close thereto that the reverse bias depletion region from the active junction can reach the guard junction, whereby the guard junction modifies the shape of the depletion region from the active junction thus lowering the electric field intensity at a given applied reverse voltage across the active junction.

496 With physical configuration of semiconductor surface to reduce electric field (e.g., reverse bevels, double bevels, stepped mesas, etc.):
This subclass is indented under subclass 487. Subject matter wherein the means to increase breakdown voltage includes a semiconductor surface portion having a physical configuration, such as a bevel or mesa, to reduce electric field strength at a given applied voltage. Typically, the physical configuration will be such that the depletion region from a reverse biased junction in the active device reaches the physically configured surface and is forced by the shape of the surface to spread wider at a given applied reverse voltage than it would otherwise, thus reducing the electric field strength in the depletion layer.

497 PUNCHTHROUGH STRUCTURE DEVICE (E.G., PUNCHTHROUGH

TRANSISTOR, CAMEL BARRIER DIODE):

This subclass is indented under the class definition. Subject matter having at least one active pn, Schottky barrier, or other rectifying junction which can be reverse biased to produce a depletion layer, the active junction being spaced from a second junction by a layer of semiconductor material in which the depletion region extending from the active junction is produced, the second junction being one capable of supplying minority carriers to the layer of semiconductor material upon forward bias of the second junction, and in which the second junction is located sufficiently close to the active junction that the depletion region from the active junction can reach the second junction, thereby forward biasing the second junction and causing the injection of minority carriers therefrom which traverse the depletion layer and reach the active junction.

SEE OR SEARCH THIS CLASS, SUBCLASS:

361+, for punchthrough structure elements used to protect against overvoltage gate insulator breakdown of insulated gate devices.

498 Punchthrough region fully depleted at zero external applied bias voltage (e.g., camel barrier or planar doped barrier devices, or so-called "Bipolar SIT" devices):

This subclass is indented under subclass 497. Subject matter wherein the active junction and the second junction are sufficiently closely spaced that the depletion region from the active junction due to the built-in potential of the active junction reaches the second junction even in the absence of a reverse bias voltage across the active junction.

499 INTEGRATED CIRCUIT STRUCTURE WITH ELECTRICALLY ISOLATED COMPONENTS:

This subclass is indented under the class definition. Subject matter wherein at least one active solid-state device is provided in a single, monolithic semiconductor chip along with other active or passive elements in the chip, and means are provided to electrically isolate different devices in the monolithic chip from each other.

SEE OR SEARCH THIS CLASS, SUBCLASS:

7, for intervalley transfer bulk effect devices (e.g., Gunn effect devices) in a monolithic integrated circuit.

93, for plural light emitting devices with electrical isolation means in integrated circuit structure.

265, for JFET devices having vertical current path in integrated circuit.

272, through 278, for JFET devices in integrated circuits.

334, for short channel IGFET devices having a gate electrode controlling the vertical portion of the channel and being in a groove in an integrated circuit.

337, and 338, for graded channel short channel IGFET devices in integrated circuit structure.

357, through 359, for insulated electrode field effect devices with gate insulator overvoltage protection means in complementary field effect transistor integrated circuit devices.

368, through 401, for IGFET devices in integrated circuit.

427, for a magnetic field sensor in an integrated circuit.

446, for matrix or array type photodetectors with specific isolation means in an integrated circuit.

491, and 492, for devices with means to increase breakdown voltage in an integrated circuit, including, for example, RESURF devices.

663, for a superconductive contact or lead on an integrated circuit.

713, for cooling means for an integrated circuit device.

758, through 760, for multi-level metallization in, e.g., an integrated circuit device.

922, for a device with means to prevent inspection of or tampering with an integrated circuit.

929, for pn junction isolated integrated circuits with isolation walls having minimum dopant concentration at intermediate depth in epitaxial layer.

SEE OR SEARCH CLASS:

438, Semiconductor Device Manufacturing: Process, particularly subclasses 294+ for methods of making laterally spaced, electrically isolated semiconductor regions in combination with insulated gate field effect transistors; subclasses 353+ for methods of making laterally spaced, electrically isolated semiconductor regions in combination with bipolar transistors; and subclasses 400+ for methods of making laterally spaced, electrically isolated semiconductor regions or various

500 Including high voltage or high power devices isolated from low voltage or low power devices in the same integrated circuit:

This subclass is indented under subclass 499. Subject matter wherein the monolithic chip includes both electronic components specifically configured for operation at high voltages or high power levels, along with other electronic components which are configured for operation only at low voltages or power levels.

(1) Note. See this class, subclass 491 for monolithic chips which include active components with specific means provided to increase the breakdown voltage of those active components. The combination of high voltage and low voltage active solid-state devices on the same monolithic chip will only be classified in this subclass (500), if no particular structure is provided to increase the breakdown voltage of the high voltage components.

501 Including dielectric isolation means:

This subclass is indented under subclass 500. Subject matter wherein the means to electrically isolate different devices in the same monolithic chip, containing both high voltage or power and low voltage or power devices, from each other includes a region of electrical insulator material.

502 High power or high voltage device extends completely through semiconductor substrate (e.g., backside collector contact):

This subclass is indented under subclass 500. Subject matter wherein at least one high voltage or high power device extends completely through the monolithic chip from the top surface to the bottom surface of the chip.

503 With contact or metallization configuration to reduce parasitic coupling (e.g., separate ground pads for different parts of integrated circuit):

This subclass is indented under subclass 499. Subject matter wherein the chip includes contacts or electrical interconnections, such as metal strips deposited on the surface of the chip, which contacts or interconnections are configured in such a manner as to reduce or eliminate unwanted parasitic coupling of electrical signals from one part or component of the integrated circuit to another.

(1) Note. Such configuration might be, for example, a shielding conductive layer connected to fixed potential, or large area metal pads for connection to external supply voltages with plural separate pads provided to connect different parts or components of the same integrated circuit to the same external voltage, to prevent voltage drops from electrical current flowing between a pad and one component from producing a parasitic varying voltage applied to another component.

SEE OR SEARCH THIS CLASS, SUBCLASS:

659, for electrical shielding, in general, in active solid-state devices.

664, for transmission line connections, in general, in active solid-state devices.

504 Including means for establishing a depletion region throughout a semiconductor layer for isolating devices in different portions of the layer (e.g., "JFET" isolation):

This subclass is indented under subclass 499. Subject matter wherein means are provided for producing a region in a layer which is fully depleted of charge carriers and thereby nonconductive as part of the means for electrically

isolating different devices in the chip from each other.

505 With polycrystalline semiconductor isolation region in direct contact with single crystal active semiconductor material:
This subclass is indented under subclass 499. Subject matter wherein the means for electrically isolating different devices in the chip from each other includes at least one region of polycrystalline (i.e., made up of many small crystals) semiconductor material, which polycrystalline isolation region is in direct contact with at least one region of single crystal semiconductor material which forms part of an active solid-state device in the chip.

(1) Note. The polycrystalline isolation region may be either undoped or doped with recombination center doping, in order to make it high resistivity and thus, effectively, an electrical insulator, or may be doped with a p or n dopant in order to form a pn junction with the single crystal material of the active solid-state device so that the rectifying junction between the doped isolation region and the single crystal active portion, when reverse biased, electrically isolates the devices in the chip from each other.

506 Including dielectric isolation means:
This subclass is indented under subclass 499. Subject matter wherein the means to electrically isolate different devices in the same monolithic chip from each other includes a region of electrical insulator material.

507 With single crystal insulating substrate (e.g., sapphire):
This subclass is indented under subclass 506. Subject matter wherein the means to electrically isolate different devices from each other includes a substrate of single crystal insulating material, upon which the semiconductor material of the active devices is grown in heteroepitaxial relationship therewith.

(1) Note. The substrate may typically be the alpha crystalline phase of aluminum oxide, commonly called sapphire or single crystalline beryllium oxide or single crystal magnesium aluminate known as spinel.

508 With metallic conductor within isolating dielectric or between semiconductor and isolating dielectric (e.g., metal shield layer or internal connection layer):
This subclass is indented under subclass 506. Subject matter wherein a metallic (metal or metal-like) conductor is located within the region of electrical insulator material which isolates the components on the chip from each other or is provided between the single crystal semiconductor material of the semiconductor components and the electrical insulator material forming the dielectric isolation.

(1) Note. The metallic conductor may be used to provide interconnections between components on the chip or as an electrical shielding layer.

509 Combined with pn junction isolation (e.g., isoplanar, LOCOS):
This subclass is indented under subclass 506. Subject matter wherein the means for electrically isolating components in the chip from each other includes, in addition to portions of electrical insulator material, pn junctions separating regions of active devices from each other and/or from a supporting semiconductor substrate.

(1) Note. There are several names in common use for isolation of this type, particularly where the pn junctions provide isolation between active devices and the supporting semiconductor substrate with the dielectric material recessed into the semiconductor between active devices and extending down to the isolating pn junctions to separate devices laterally from each other. Such common names include LOCOS (Local Oxidation of Silicon), ROI (Recessed Oxide Isolation), Isoplanar, and Planox. These terms do not represent different isolation structures, but are merely alternative names for the same type of isolation.

510 Dielectric in groove:
This subclass is indented under subclass 509. Subject matter wherein the electrical insulator material forming part of the isolation means is located in grooves in the semiconductor surface (e.g., LOCOS)

SEE OR SEARCH THIS CLASS, SUBCLASS:

374, for CMOS FET dielectric isolation means (e.g., dielectric layer in vertical groove.)

511 With complementary (npn and pnp) bipolar transistor structures:

This subclass is indented under subclass 509. Subject matter wherein the device includes, on the same monolithic chip, both pnp bipolar transistors and npn bipolar transistor structures.

512 Complementary devices share common active region (e.g., integrated injection logic, I^2L):

This subclass is indented under subclass 511. Subject matter wherein the device includes structures wherein a pnp transistor shares a semiconductor region with an npn transistor, e.g., where the base region of the pnp transistor serves also as the emitter of the npn transistor and the collector of the pnp transistor serves as the base region of the npn transistor.

(1) Note. Search this class, subclass 107 for regenerative switching devices, which typically are in the form of a pnp transistor and an npn transistor, the collector and base of the pnp transistor forming the base and collector, respectively, of the npn transistor.

(2) Note. A typical structure in which pnp transistors and npn transistors share regions in common is that called Integrated injection logic, I^2L (formerly alternatively called merged transistor logic, MTL), in which a pnp transistor serves to supply base region current to a multicollector npn transistor, with the base region of the npn being the logic circuit input and the multiple collectors providing logic fan out to plural further logic gates.

513 Vertical walled groove:

This subclass is indented under subclass 510. Subject matter wherein the dielectric isolation is located in grooves in the surface of the overall device which extend perpendicular to the surface of the overall device.

514 With active junction abutting groove (e.g., "walled emitter"):

This subclass is indented under subclass 513. Subject matter wherein at least one pn junction forming a part of an active solid-state device terminates against the dielectric filling in the vertical walled isolation groove.

(1) Note. If the emitter-base junction terminates against a dielectric isolation sidewall, this is termed a "walled emitter" transistor structure.

515 With active junction abutting groove (e.g., "walled emitter"):

This subclass is indented under subclass 510. Subject matter wherein at least one pn junction forming a part of an active solid-state device terminates against the dielectric filling in the isolation groove.

516 With passive component (e.g., resistor, capacitor, etc.):

This subclass is indented under subclass 510. Subject matter wherein the device contains, in addition to at least one active solid-state device, at least one passive component, such as a resistor or capacitor.

517 With bipolar transistor structure:

This subclass is indented under subclass 510. Subject matter wherein the device contains at least one bipolar transistor structure.

518 With polycrystalline connecting region (e.g., polysilicon base contact):

This subclass is indented under subclass 517. Subject matter wherein the device has portions of polycrystalline (i.e., made up of many small crystals) semiconductor material serving as electrical contacts or connections.

519 Including heavily doped channel stop region adjacent groove:

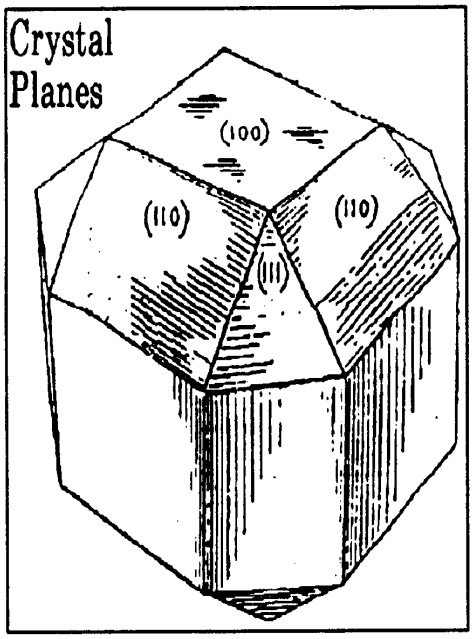
This subclass is indented under subclass 510. Subject matter wherein the device has at least one heavily doped semiconductor region adjacent a dielectric filled groove to prevent formation of parasitic inversion channels in the semiconductor material.

520 Conductive filling in dielectric-lined groove (e.g., polysilicon backfill):
This subclass is indented under subclass 510. Subject matter wherein the device has the grooves filled with a lining of dielectric material together with a conductive filling in the groove, the conductive filling being separated from the semiconductor material by the dielectric lining of the groove.

521 Sides of grooves along major crystal planes (e.g., (111), (100) planes, etc.):
This subclass is indented under subclass 510. Subject matter wherein the device has grooves for the isolation whose sides are oriented along one or more major crystal planes of the semiconductor material in which the grooves are formed.

(1) Note. Major crystal planes are considered to be the (111), (110), and (100) planes in a crystal with cubic symmetry.

(2) Note. See illustration, below.



522 Air isolation (e.g., beam lead supported semiconductor islands):
This subclass is indented under subclass 506. Subject matter wherein the isolation means is air (e.g., islands of semiconductor material supported by beam leads and separated by air).

SEE OR SEARCH CLASS:
438, Semiconductor Device Manufacturing: Process, particularly subclass 411 for methods of forming electrically isolated semiconductor islands held in place by beam lead metallization; subclass 461 for methods of forming beam leads on a semiconductor substrate combined with dicing of the substrate into plural separate bodies; and subclass 611 for methods of forming beam lead metallization on a semiconductor substrate.

523 Isolation by region of intrinsic (undoped) semiconductor material (e.g., including region physically damaged by proton bombardment):
This subclass is indented under subclass 506. Subject matter wherein the electrical insulator material which provides the dielectric isolation includes a region of intrinsic (undoped) semiconductor material, with resulting high resistivity.

(1) Note. The isolation region may contain a region which has been physically damaged by proton bombardment or by other means.

524 Full dielectric isolation with polycrystalline semiconductor substrate:
This subclass is indented under subclass 506. Subject matter wherein the integrated circuit substrate is made of polycrystalline semiconductor material and the isolation means is a dielectric material which surrounds each active solid-state semiconductor device, resulting is those devices becoming islands in a sea of dielectric material.

525 With complementary (npn and pnp) bipolar transistor structures:
This subclass is indented under subclass 524. Subject matter wherein the device includes complementary bipolar transistors (i.e., includes both pnp and npn bipolar transistors).

(1) Note. The device may include complementary lateral bipolar transistor structures.

526 With bipolar transistor structure:
This subclass is indented under subclass 524. Subject matter wherein the device includes at least one bipolar transistor structure.

527 Sides of isolated semiconductor islands along major crystal planes (e.g., (111), (100) planes, etc.):
This subclass is indented under subclass 524. Subject matter wherein the device has sides of the isolated single crystal semiconductor islands which are oriented along one or more major crystal planes of the semiconductor material of the islands.

528 Passive components in ICs:
This subclass is indented under subclass 499. Subject matter wherein the device is contained in a single, monolithic chip with electrical components which are passive, i.e., which do not have gain, for example, pure capacitors, inductors, or resistors.

SEE OR SEARCH THIS CLASS, SUBCLASS:
379, for a passive component combined with an IGFET device in an integrated circuit.
516, for passive components in an integrated circuit with dielectric in groove and pn junction isolation.
904, for a FET combined with passive components adapted for use as a static memory cell.

529 Including programmable passive component (e.g., fuse):
This subclass is indented under subclass 528. Subject matter wherein a passive component is programmable, i.e., may be permanently altered (e.g., a fuse - a protective device designed to open a circuit in response to an excessive current).

SEE OR SEARCH CLASS:
438, Semiconductor Device Manufacturing: Process, particularly subclasses 467, 600, and 601 for methods of forming or modifying electrically alterable structures for selectively interconnecting electrical devices on a semiconductor substrate.

530 Anti-fuse:
This subclass is indented under subclass 529. Subject matter wherein an element which is normally non-conductive is made conductive (e.g., a capacitor) that is, that can be selectively electrically shorted.

531 Including inductive element:
This subclass is indented under subclass 528. Subject matter wherein the device includes an electrical inductor, i.e., an element that tends to oppose any change of current applied thereto because of a magnetic field generated by the inductor itself.

532 Including capacitor component:
This subclass is indented under subclass 528. Subject matter wherein the device includes an electrical capacitor, i.e., a passive element with electrical conductors separated by a dielectric material which stores electrical charge when potential differences exist between the conductive elements of the capacitor.

533 Combined with resistor to form RC filter structure:
This subclass is indented under subclass 532. Subject matter wherein the capacitor element is combined with an electrical resistance element to form an electrical filter in the form of an integrated RC filter circuit.

534 With means to increase surface area (e.g., grooves, ridges, etc.):
This subclass is indented under subclass 532. Subject matter wherein the device includes means to increase the surface area of the device by, for example, grooves or ridges in the surface of the device.

535 Both terminals of capacitor isolated from substrate:
This subclass is indented under subclass 532. Subject matter wherein the device includes a capacitor, both terminals of which are electrically isolated from the integrated circuit chip substrate.

536 Including resistive element:
This subclass is indented under subclass 528. Subject matter wherein the device includes an electrical resistance element.

537 Using specific resistive material:
This subclass is indented under subclass 536. Subject matter wherein the passive resistive element is a specific chemical element, compound, or composition.

538 Polycrystalline silicon (doped or undoped):
This subclass is indented under subclass 537. Subject matter wherein the specific resistive material is a silicon material made up of many single crystals having a random orientation.

539 Combined with bipolar transistor:
This subclass is indented under subclass 536. Subject matter wherein the device includes at least one bipolar transistor structure along with the resistive element.

540 With compensation for non-linearity (e.g., dynamic isolation pocket bias):
This subclass is indented under subclass 539. Subject matter wherein means are provided to compensate for non-linearity of the resistor, such as by provision of varying bias voltage to a semiconductor pocket which forms a pn junction with the resistive element and provides electrical isolation therefor.

541 Pinch resistor:
This subclass is indented under subclass 539. Subject matter wherein the resistor element has a structure in the form of a layer of one conductivity type sandwiched between a pair of regions of opposite conductivity type, so that the upper region of opposite conductivity type restricts the thickness of the resistive layer and thus increases its resistivity.

(1) Note. Typically, the resistor will have the same doping profile as the base region of the bipolar transistor, while the lower opposite conductivity type region will have the same doping profile as the bipolar transistor collector, and the upper, or “pinching” region, will have the same doping profile as the bipolar transistor emitter.

542 Resistor has same doping as emitter or collector of bipolar transistor:
This subclass is indented under subclass 539. Subject matter wherein the resistor region has the same doping concentration and profile (e.g., is formed in the same step as) either the emitter or the collector region of the bipolar transistor with which the resistor is combined in the same integrated circuit.

(1) Note. Most resistors in bipolar integrated circuits are formed with the same doping step as the bipolar transistor base regions. Resistors that are instead formed at the same doping step as the emitter or collector, rather than the base, go in this subclass.

543 Lightly doped junction isolated resistor (e.g., ion implanted resistor):
This subclass is indented under subclass 539. Subject matter wherein the resistive element is of the form of a lightly doped layer of one conductivity type located in a region of opposite conductivity type, such that the pn junction between the resistor region and its containing opposite conductivity type region serves to isolate the resistor.

(1) Note. A resistor region is considered to be lightly doped if it is substantially less heavily doped than the base region of the bipolar transistors in the same integrated circuit, or if it is has a doping density not greater than 100 times that of the opposite conductivity type region in which it is contained.

(2) Note. Such lightly doped resistors are typically formed by the process of ion implantation, wherein desired dopant atoms are placed in the semiconductor body by ionizing the dopant material and accelerating the resulting ions through a carefully controlled voltage to impinge on the surface of the semiconductor

material, so that the depth of the resulting dopant atoms is determined by the accelerating voltage and the doping density is determined by the flux of the ion beam.

544 With pn junction isolation:
This subclass is indented under subclass 499. Subject matter wherein the means for electrically isolating different devices from each other includes a pn junction located between the devices to be isolated.

545 With means to control isolation junction capacitance (e.g., lightly doped layer at isolation junction to increase depletion layer width):
This subclass is indented under subclass 544. Subject matter wherein the device is provided with means, such as a lightly doped semiconductor layer at the isolation junction, to control (e.g., increase or decrease) the capacitance of the isolation junction.

546 With structural means to protect against excess or reversed polarity voltage:
This subclass is indented under subclass 544. Subject matter wherein means is provided to protect the circuit or its components from application of an excessive or reversed polarity voltage.

547 With structural means to control parasitic transistor action or leakage current:
This subclass is indented under subclass 544. Subject matter including means to control or reduce parasitic bipolar transistor action, i.e., bipolar transistor action in which the substrate and isolation junctions of the integrated circuit act as active junctions of an unintended bipolar transistor, or to control or reduce leakage currents associated with the pn isolation junctions.

548 At least three regions of alternating conductivity types with dopant concentration gradients decreasing from surface of semiconductor (e.g., "triple-diffused" integrated circuit):
This subclass is indented under subclass 544. Subject matter including at least three regions of alternating conductivity type (p or n), with each successive region contained within the previous region, and each of the regions having a doping concentration which decreases with distance from the same external surface of the semiconductor body.

(1) Note. Junction isolated integrated circuits of this type are typically manufactured by starting with an uniformly doped p-type semiconductor body to serve as the substrate, then diffusing spaced n-type regions into the P substrate to form collectors of npn transistors, and then successively diffusing p-type base and n-type emitters into the spaced n-type regions. Junction isolated integrated circuits of this type are simple to manufacture, due to the reduced number of processing steps involved, but suffer from non-optimum doping concentration profiles, particularly in the collector regions.

549 With substrate and lightly doped surface layer of same conductivity type, separated by subsurface heavily doped region of opposite conductivity type (e.g., "collector diffused isolation" integrated circuit):
This subclass is indented under subclass 544. Subject matter wherein the junction isolation is formed in an integrated circuit with a substrate and lightly doped surface layer of the same conductivity type, separated by subsurface heavily doped region of opposite conductivity type (e.g., "collector diffused isolation" integrated circuit).

550 With lightly doped surface layer of one conductivity type on substrate of opposite conductivity type, having plural heavily doped portions of the one conductivity type between the layer and substrate, different ones of the heavily doped portions having differing depths or physical extent:
This subclass is indented under subclass 544. Subject matter wherein the junction isolation is formed in an integrated circuit with a lightly doped surface layer of one conductivity type on substrate of opposite conductivity type, having plural heavily doped portions of the one conductivity type between the layer and substrate, different ones of the heavily doped portions having differing depths or physical extent.

(1) Note. The heavily doped portions are usually "subcollector" contact regions, low resistance connections to the bottom

of the collector region of a bipolar transistor.

551 Including voltage reference element (e.g., avalanche diode, so-called "Zener diode" with breakdown voltage greater than 6 volts or with positive temperature coefficient of breakdown voltage):
This subclass is indented under subclass 544. Subject matter including a voltage reference element, i.e., a device which limits the operating voltage of one or more active devices in the integrated circuit (e.g., an avalanche diode, so-called "Zener diode" with breakdown voltage greater than 6 volts, or with positive temperature coefficient of breakdown voltage).

SEE OR SEARCH THIS CLASS, SUBCLASS:

199, for an avalanche diode in a non-charge transfer device having a heterojunction.

481, and 482, for Schottky barrier avalanche diodes.

603, through 606, for avalanche diodes not classified above those subclasses in this schedule, i.e., not involving a heterojunction in a non-charge transfer device or a Schottky barrier, or one used as a voltage reference element with pn junction isolation means in an integrated circuit.

552 With bipolar transistor structure:
This subclass is indented under subclass 544. Subject matter wherein the junction isolation is formed in an integrated circuit between active devices at least one of which has a bipolar transistor structure.

553 Transistors of same conductivity type (e.g., npn) having different current gain or different operating voltage characteristics:
This subclass is indented under subclass 552. Subject matter wherein plural bipolar transistor structures are present which have the same electrical conductivity type (e.g., npn) but have different current gain or different operating voltage characteristics.

554 With connecting region made of polycrystalline semiconductor material (e.g., polysilicon base contact):
This subclass is indented under subclass 552. Subject matter wherein a connecting region or contact made of a polycrystalline semiconductor material is present in the bipolar integrated circuit.

555 Complementary bipolar transistor structures (e.g., integrated injection logic, I^2L):
This subclass is indented under subclass 552. Subject matter wherein the device contains complementary bipolar transistor structures (i.e., both pnp and npn bipolar transistor structures).

556 Including lateral bipolar transistor structure:
This subclass is indented under subclass 555. Subject matter wherein at least one of the pnp or npn complementary bipolar transistors is a lateral structure (i.e., has current flow between its emitter and collector parallel to a major surface of the semiconductor chip).

557 Lateral bipolar transistor structure:
This subclass is indented under subclass 499. Subject matter wherein the device includes at least one bipolar transistor which has a lateral structure (i.e., has current flow between its emitter and collector parallel to a major surface of the semiconductor chip).

558 With base region doping concentration step or gradient or with means to increase current gain:
This subclass is indented under subclass 557. Subject matter wherein the device has a base region with a variable impurity dopant concentration across it, or wherein means are provided to increase the current gain of the transistor.

559 With active region formed along groove or exposed edge in semiconductor:
This subclass is indented under subclass 557. Subject matter wherein the device has a groove or exposed edge and an active region of the bipolar transistor is formed along the groove or exposed edge.

560 With multiple collectors or emitters:
This subclass is indented under subclass 557. Subject matter wherein the device has more than one collector region or more than one emitter region.

561 With different emitter to collector spacings or facing areas:
This subclass is indented under subclass 560. Subject matter wherein the device has different emitter to collector spacings for different collectors or emitters.

562 With auxiliary collector/re-emitter between emitter and output collector (e.g., "Current Hogging Logic" device):
This subclass is indented under subclass 560. Subject matter wherein the device has a region located between its emitter and its collector which serves as an auxiliary collector/re-emitter, i.e., the auxiliary region collects carriers emitted by the emitter and re-emits them to the collector (e.g., a "Current Hogging Logic" device).

563 With multiple separately connected emitter, collector, or base regions in same transistor structure:
This subclass is indented under subclass 499. Subject matter wherein the device includes two or more separately connected (i.e., not commonly connected) emitter, collector, or base regions.

564 Multiple base or collector regions:
This subclass is indented under subclass 563. Subject matter wherein the device contains two or more separately connected base or collector regions, but not more than one separately connected emitter region.

565 BIPOLAR TRANSISTOR STRUCTURE:
This subclass is indented under the class definition. Subject matter wherein the active solid-state device comprises at least one bipolar transistor.

SEE OR SEARCH THIS CLASS, SUBCLASS:
47, for bipolar transistor structure having a metal contact alloyed to elemental semiconductor type pn junction in a non-regenerative structure.
511, for complementary bipolar transistor structure having dielectric-in-groove isolation and pn junction isolation in an integrated circuit.
517, and 518, for bipolar transistor structure having dielectric-in-groove isolation and pn junction isolation in an integrated circuit.
525, for complementary bipolar structure with full dielectric isolation in an integrated circuit.
526, for bipolar structure with full dielectric isolation in an integrated circuit.
552, through 556, for bipolar transistor structure combined with pn junction isolation in an integrated circuit.
557, through 562, for integrated circuits with electrically isolated lateral bipolar transistor structure.

SEE OR SEARCH CLASS:
148, Metal Treatment, digests 10 and 11 for bipolar transistor devices.
326, Electronic Digital Logic Circuitry, particularly subclasses 18+, 42+, 48, 75+, 89+, 109+, and 124+ for logic circuits utilizing bipolar transistors.
327, Miscellaneous Active Electrical Nonlinear Devices, Circuits, and Systems, particularly subclasses 204, 207, 405, 411+, 417, 432+, 439, 459, 462, 463, 474, 475, and 478+ for miscellaneous nonlinear circuits with explicitly recited bipolar transistors.
330, Amplifiers, subclasses 250+ for amplifiers with transistors which may be bipolar transistors and subclass 300 which explicitly provides for bipolar or field effect transistors.
341, Coded Data Generation or Conversion, subclasses 127+ for bipolar analog to or from digital converters and subclass 133 for such device with a drift (graded base) transistor element.
438, Semiconductor Device Manufacturing: Process, subclasses 309+ for methods of forming bipolar transistors.

566 Plural non-isolated transistor structures in same structure:
This subclass is indented under subclass 565. Subject matter wherein the bipolar structure includes more than one bipolar transistor in a

structure without electrical isolation between transistors.

(1) Note. See subclass 499, above, for integrated circuits with electrical isolation, including with bipolar transistors.

567 Darlington configuration (i.e., emitter to collector current of input transistor supplied to base region of output transistor):
This subclass is indented under subclass 566. Subject matter wherein the plural non-electrically isolated transistor structures are arranged in a Darlington configuration (i.e., wherein the emitter to collector current of an input transistor is supplied to the base region of an output transistor).

568 More than two Darlington-connected transistors:
This subclass is indented under subclass 567. Subject matter wherein the device contains more than two Darlington-connected bipolar transistors.

569 Complementary Darlington-connected transistors:
This subclass is indented under subclass 567. Subject matter wherein the Darlington configuration comprises two bipolar transistors which have a complementary connection, i.e., the input transistor is of one conductivity type (e.g., npn) and the other is of the opposite conductivity type (e.g., pnp).

570 With active components in addition to Darlington transistors (e.g., antisaturation diode, bleeder diode connected antiparallel to input transistor base-emitter junction, etc.):
This subclass is indented under subclass 567. Subject matter wherein the device contains active solid-state devices in addition to Darlington bipolar transistors.

571 Non-planar structure (e.g., mesa emitter, or having a groove to define resistor):
This subclass is indented under subclass 567. Subject matter wherein the device is a non-planar structure (i.e., the upper surface is not a completely flat, unbroken surface).

572 With resistance means connected between transistor base regions:
This subclass is indented under subclass 567. Subject matter wherein the device includes a resistor element structure connecting the base regions of the Darlington bipolar transistors.

573 With housing or contact structure or configuration:
This subclass is indented under subclass 567. Subject matter wherein a housing or electrical contact structure is provided for the device.

574 Complementary transistors share common active region (e.g., integrated injection logic, I^2L):
This subclass is indented under subclass 566. Subject matter wherein the device includes complementary transistors (i.e., bipolar transistors of different conductivity types) which share a common active region (e.g., integrated injection logic, I^2L).

575 Including lateral bipolar transistor structure:
This subclass is indented under subclass 574. Subject matter wherein at least one of the complementary bipolar transistors sharing a common region is a lateral bipolar transistor (i.e., has current flow between its emitter and collector parallel to a major surface of the semiconductor chip).

SEE OR SEARCH THIS CLASS, SUBCLASS:
423, for lateral and other bipolar transistor magnetic field responsive structure.
557+, for electrically isolated lateral bipolar transistor structures in an integrated circuit.

576 With contacts of refractory material (e.g., polysilicon, silicide of refractory or platinum group metal):
This subclass is indented under subclass 575. Subject matter wherein the device has electrical contacts which are made of a refractory material (e.g., polysilicon, or a silicide of a metal found in groups IVA, VA, VIA or VIIIA (other than iron (Fe) nickel (Ni) or cobalt (Co)) of the periodic table of the elements.

577 Including additional component in same, non-isolated structure (e.g., transistor with diode, transistor with resistor, etc.):
This subclass is indented under subclass 565. Subject matter wherein the device includes an additional component (e.g., a diode or a resistor) in the same non-electrically isolated structure with the bipolar transistor structure.

578 With enlarged emitter area (e.g., power device):
This subclass is indented under subclass 565. Subject matter wherein the device has relatively enlarged emitter cross-sectional areas (e.g., power devices).

579 With separate emitter areas connected in parallel:
This subclass is indented under subclass 578. Subject matter wherein there are a plurality of separate emitter areas which are electrically connected in parallel.

580 With current ballasting means (e.g., emitter ballasting resistors or base current ballasting means):
This subclass is indented under subclass 579. Subject matter wherein current ballasting means is provided to divide emitter current more evenly between the plurality of separate emitter areas which are electrically interconnected in parallel.

SEE OR SEARCH THIS CLASS, SUBCLASS:
164, for regenerative devices having multi-emitter regions which may include emitter ballasting resistors.

581 Thin film ballasting means (e.g., polysilicon resistor):
This subclass is indented under subclass 580. Subject matter wherein the ballasting means comprises thin film resistor means (e.g., a thin film polysilicon resistor).

582 With current ballasting means (e.g., emitter ballasting resistors or base current ballasting resistors):
This subclass is indented under subclass 578. Subject matter wherein the enlarged emitter area has a current ballasting means (e.g., emitter ballasting resistors).

583 With means to reduce transistor action in selected portions of transistor (e.g., heavy base region doping under central web of emitter to prevent secondary breakdown):
This subclass is indented under subclass 578. Subject matter wherein there are means in selected portions of the transistor to reduce the transistor action in those portions.

584 With housing or contact (i.e., electrode) means:
This subclass is indented under subclass 578. Subject matter wherein the enlarged emitter area device is provided with a housing (means to protect the device from the environment) or with electrical contact means.

585 With means to increase inverse gain:
This subclass is indented under subclass 565. Subject matter wherein there are means associated with the transistor to increase the gain in an inverse mode of operation.

586 With non-planar semiconductor surface (e.g., groove, mesa, bevel, etc.):
This subclass is indented under subclass 565. Subject matter wherein the device has a non-planar upper or side surface.

587 With specified electrode means:
This subclass is indented under subclass 565. Subject matter wherein the device has specific electrode means.

588 Including polycrystalline semiconductor as connection:
This subclass is indented under subclass 587. Subject matter wherein the electrode means includes polysilicon semiconductor material to make an electrical connection.

589 Avalanche transistor:
This subclass is indented under subclass 565. Subject matter wherein the device is a bipolar transistor designed to be operated with its base-collector junction biased into avalanche breakdown.

590 With means to reduce minority carrier lifetime (e.g., region of deep level dopant or region of crystal damage):
This subclass is indented under subclass 565. Subject matter wherein the device has means to reduce the minority carrier lifetime, i.e., before recombination with a majority carrier, by, for example, a region of deep level dopant or a region of damage to the semiconductor crystal.

591 With emitter region having specified doping concentration profile (e.g., high-low concentration step):
This subclass is indented under subclass 565. Subject matter wherein the device has an emitter region with a specified impurity dopant concentration profile (e.g., a specified concentration gradient across the emitter region).

592 With base region having specified doping concentration profile or specified configuration (e.g., inactive base more heavily doped than active base or base region has constant doping concentration portion (e.g., epitaxial base)):
This subclass is indented under subclass 565. Subject matter wherein the device has a base region with a cross section that has a specified impurity dopant concentration across it or has a particular geometric configuration.

593 With means to increase current gain or operating frequency:
This subclass is indented under subclass 565. Subject matter wherein the device includes means to increase the current gain or the operating frequency of the devices.

594 WITH GROOVE TO DEFINE PLURAL DIODES:
This subclass is indented under the class definition. Subject matter wherein the active solid-state device has more than one diode and has a groove therein to separate the diodes.

595 VOLTAGE VARIABLE CAPACITANCE DEVICE:
This subclass is indented under the class definition. Subject matter wherein the active solid-state device has a capacitance which varies with the voltage applied thereto.

(1) Note. This type of voltage variable capacitor device is to be distinguished from voltage variable capacitors (also referred to as varactors) which are passive devices only and which may be found, for example, in Class 361, Electricity: Electrical Systems and Devices, subclass 277, and Class 332, Modulators, subclass 136, modulators with varactors.

SEE OR SEARCH THIS CLASS, SUBCLASS:

312, for insulated gate type voltage variable capacitor devices or voltage variable capacitor devices combined with an insulated gate transistor.

438, Semiconductor Device Manufacturing: Process, subclass 379 for methods of forming a voltage variable capacitance device utilizing a semiconductor substrate.

480, for a voltage variable capacitor diode with a Schottky barrier.

596 With specified dopant profile:
This subclass is indented under subclass 595. Subject matter wherein the device has a cross section which has a specified impurity dopant concentration across it.

597 Retrograde dopant profile (e.g., dopant concentration decreases with distance from rectifying junction):
This subclass is indented under subclass 596. Subject matter wherein the device contains a rectifying junction and wherein the variable dopant concentration decreases with distance from the rectifying junction.

598 With plural junctions whose depletion regions merge to vary voltage dependence:
This subclass is indented under subclass 595. Subject matter wherein the device has more than one junction with depletion regions that merge to achieve a capacitance that varies with applied voltage.

599 With means to increase active junction area (e.g., grooved or convoluted surface):
This subclass is indented under subclass 595. Subject matter wherein the device is provided with an increased active junction area (e.g.,

grooves or a convoluted surface to increase the active junction area).

600 With physical configuration to vary voltage dependence (e.g., mesa):
This subclass is indented under subclass 595. Subject matter wherein the device has a physical configuration (e.g., a mesa) to vary the voltage dependency of the capacitance.

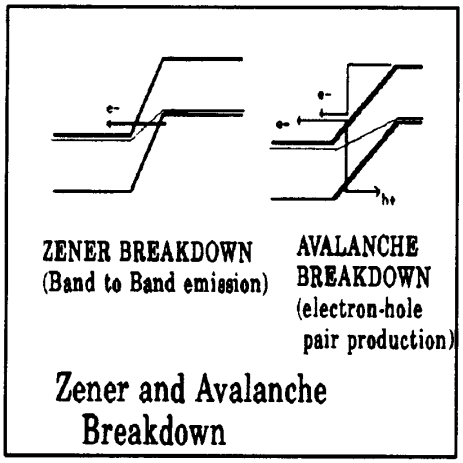
601 Plural diodes in same non-isolated structure, or device having three or more terminals:
This subclass is indented under subclass 595. Subject matter wherein the device is comprised of more than one diode located in the same non-isolated structure, or is a device which has three or more electrical terminals.

602 With specified housing or contact:
This subclass is indented under subclass 595. Subject matter wherein the device is provided with a specific housing (structure to protect the device from the environment) or electrical contact structure.

603 AVALANCHE DIODE (E.G., SO-CALLED "ZENER" DIODE HAVING BREAKDOWN VOLTAGE GREATER THAN 6 VOLTS):
This subclass is indented under the class definition. Subject matter configured to operate in a manner in which an external voltage is applied in the reverse-conducting direction of the device junction with sufficient magnitude to cause the potential barrier at the junction to breakdown due to electrons or holes gaining sufficient speed to dislodge valence electrons and thus create more hole-electron current carriers by an avalanche process.

(1) Note. This includes the so-called "Zener" diode using silicon as a semiconductor which has a breakdown voltage greater than 6 volts. True Zener diodes conduct by reverse tunneling, and are classified in subclass 106. However, many avalanche breakdown diodes which are classifiable in subclass 603 are called "Zener" diodes even though the breakdown mechanism is avalanche multiplication, rather than tunneling. In silicon, pn junctions which break down at less than 5 volts, do so by reverse tunneling, while those that break down at above 6 volts, do so by avalanche multiplication.

(2) Note. See the illustration, below:



Zener and Avalanche Breakdown

SEE OR SEARCH THIS CLASS, SUBCLASS:

106, for a reverse bias tunneling diode (Zener diode).

199, for an avalanche diode having a heterojunction.

481, for a Schottky barrier avalanche diode.

551, for an avalanche diode used as a voltage reference element combined with pn junction isolation means in an integrated circuit.

SEE OR SEARCH CLASS:

327, Miscellaneous Active Electrical Nonlinear Devices, Circuits, and Systems, subclasses 185+ for stable state circuits which may include an avalanche diode; subclass 326 for limiting, clipping, or clamping utilizing an avalanche diode; subclass 502 for gating circuits utilizing an avalanche diode; and subclass 584 for miscellaneous circuits utilizing an avalanche diode.

438, Semiconductor Device Manufacturing: Process, subclass 91 for methods of making a light responsive avalanche diode and subclass 380 for making an avalanche diode utilizing a semiconductor substrate.

604 Microwave transit time device (e.g., IMPATT diode):
This subclass is indented under subclass 603. Subject matter wherein the device is structured to operate as a transit time device at microwave frequencies, the frequency at which it operates being determined by the transit time of charge carriers through the depletion region which extends on both sides of the reverse biased junction (e.g., an Impact ionization avalanche transit time (IMPATT) diode).

605 With means to limit area of breakdown (e.g., guard ring having higher breakdown voltage):
This subclass is indented under subclass 603. Subject matter in which the avalanche diode device is provided with means to limit the area of the device in which electrical breakdown occurs (e.g., a guard ring having a higher breakdown voltage than the area it surrounds).

606 Subsurface breakdown:
This subclass is indented under subclass 605. Subject matter wherein the voltage breakdown occurs below the surface of the device.

607 WITH SPECIFIED DOPANT (e.g., plural dopants of same conductivity in same region):
This subclass is indented under the class definition. Subject matter wherein the active solid-state device contains impurity dopant atoms which are specified and are used to change the conductive properties of the semiconductor material.

(1) Note. If the dopant is in Si or Ge, it may be a shallow level dopant, other than an element from group III or group V of the periodic table (e.g., a dopant such as Li in Ge).

608 Switching device based on filling and emptying of deep energy levels:
This subclass is indented under subclass 607. Subject matter wherein the device utilizes charge carrier filling and emptying of deep energy levels within the forbidden gap of semiconductor material of the device to produce a switching or ON/OFF action.

609 For compound semiconductor (e.g., deep level dopant):
This subclass is indented under subclass 607. Subject matter wherein the specified dopant is in a compound semiconductor (e.g., GaAs).

610 Deep level dopant:
This subclass is indented under subclass 607. Subject matter including a specified dopant which establishes traps in the forbidden band of a semiconductor into which carriers may drop or rise.

611 With specified distribution (e.g., laterally localized, with specified concentration distribution or gradient):
This subclass is indented under subclass 610. Subject matter wherein the deep level dopant has a particular, specified distribution (e.g., with a specified concentration distribution or gradient).

612 Deep level dopant other than gold or platinum:
This subclass is indented under subclass 610. Subject matter wherein the deep level dopant is other than gold or platinum.

613 INCLUDING SEMICONDUCTOR MATERIAL OTHER THAN SILICON OR GALLIUM ARSENIDE (GaAs) (E.G., $Pb_xSn_{1-x}Te$):
Subject matter under the subclass definition which includes semiconducting material other than silicon or gallium arsenide (GaAs).

614 Group II-VI compound (e.g., CdTe, $Hg_xCd_{1-x}Te$):
This subclass is indented under subclass 613. Subject matter wherein the semiconducting material other than silicon or gallium arsenide is a compound of the periodic table group II-VI (e.g., CdTe).

615 Group III-V compound (e.g., InP):
This subclass is indented under subclass 613. Subject matter wherein the semiconducting material other than silicon or gallium arsenide is a compound of the periodic table group III-V (e.g., InP).

616 Containing germanium, Ge:
This subclass is indented under subclass 613. Subject matter wherein the semiconducting material other than silicon or gallium arsenide contains germanium (Ge).

617 INCLUDING REGION CONTAINING CRYSTAL DAMAGE:
This subclass is indented under the class definition. Subject matter wherein the device includes a region which has crystal damage.

(1) Note. The crystal damage may have been caused by charged or elementary particles bombardment of a particular region.

618 PHYSICAL CONFIGURATION OF SEMICONDUCTOR (E.G., MESA, BEVEL, GROOVE, ETC.):
This subclass is indented under the class definition. Subject matter wherein the device has a particular physical form, such as a mesa or bevel or groove.

SEE OR SEARCH THIS CLASS, SUBCLASS:
171, for regenerative devices with edge features (e.g., bevels).
496, for devices with physical configuration (e.g., bevels) to increase breakdown voltage threshold.
586, for bipolar transistor devices with non-planar semiconductor surfaces (e.g., bevels).

619 With thin active central semiconductor portion surrounded by thicker inactive shoulder (e.g., for mechanical support):
This subclass is indented under subclass 618. Subject matter wherein the device has a thin active central configuration which is surrounded by a thicker inactive shoulder region (e.g., for mechanical support).

620 With peripheral feature due to separation of smaller semiconductor chip from larger wafer (e.g., scribe region, or means to prevent edge effects such as leakage current at peripheral chip separation area):
This subclass is indented under subclass 618. Subject matter wherein the physical configuration is at the periphery of the semiconductor chip due to the separation of the chip from a larger wafer.

SEE OR SEARCH THIS CLASS, SUBCLASS:
297, for insulated gate capacitor or insulated gate transistor combined with capacitor devices with charge leakage (e.g., dark current leakage) protection means.
349, for SOI devices with means to prevent leakage current.
547, for integrated circuit devices with pn junction isolation and structural means to control leakage current.

621 With electrical contact in hole in semiconductor (e.g., lead extends through semiconductor body):
This subclass is indented under subclass 618. Subject matter wherein the physical configuration is a hole in the semiconductor through which an electrical contact extends.

622 Groove:
This subclass is indented under subclass 618. Subject matter in which there is a physical groove in a surface of the semiconductor device.

SEE OR SEARCH THIS CLASS, SUBCLASS:
117, and 118, for light activated regenerative type devices having a groove, e.g., that contains a light conductor.
127, for a bidirectional rectifier with control electrode and a groove or guard ring to separate the device into sections having different conductive polarity.
170, for a regenerative type device with a groove or other surface feature to increase breakdown voltage.
244, for a charge transfer device having a groove.
283, for a JFET with Schottky gate closely aligned with source region with a groove or overhang for alignment.
284, for a JFET with Schottky gate in a groove.
330, through 334, for a short channel IGFET with a gate electrode in a groove for controlling a vertical portion of the device channel.

397, for an IGFET in an integrated circuit with a thick insulator portion recessed in a vertical walled groove in the semiconductor surface to prevent parasitic conduction channels.

466, for a light responsive device with a physical configuration feature (e.g., a groove).

534, for a passive component located in a groove in an integrated circuit device.

571, for Darlington configuration bipolar transistor structure having a nonplanar structure (e.g., a groove).

586, for a bipolar transistor structure with a nonplanar surface (e.g., a groove).

589, for a voltage variable capacitance device with means to increase active junction area (e.g., a groove).

623 Mesa structure (e.g., including undercut or stepped mesa configuration or having constant slope taper):

This subclass is indented under subclass 618. Subject matter wherein the physical configuration is that of a mesa (e.g., there is at least one flat topped protrusion above the rest of the surface of the semiconductor body).

SEE OR SEARCH THIS CLASS, SUBCLASS:

170, for regenerative devices with mesa structure.

452, and 466, for light responsive devices with mesa structure.

571, for bipolar transistors with mesa structure.

600, for voltage variable capacitance active solid-state devices with mesa structure.

624 With low resistance ohmic connection means along exposed mesa edge (e.g., contact or heavily doped region along exposed mesa to reduce "skin effect" losses in microwave diode):

This subclass is indented under subclass 623. Subject matter wherein there is a low resistance ohmic connection means along the exposed edge of the mesa.

625 Semiconductor body including mesa is intimately bonded to thick electrical and/or thermal conductor member of larger lateral extent than semiconductor body (e.g., "plated heat sink" microwave diode):

This subclass is indented under subclass 623. Subject matter wherein the mesa semiconductor body is intimately bonded (e.g., by electroplating the semiconductor with a thick metal layer) to a thick electrical and/or thermal conductor member of larger lateral extent than the semiconductor body.

626 Combined with passivating coating:

This subclass is indented under subclass 623. Subject matter wherein there is a surface protectant or passivating coating on the surface of the mesa physical configuration.

627 With specified crystal plane or axis:

This subclass is indented under subclass 618. Subject matter wherein the physical configuration of the device is along a specified crystal plane or axis.

628 Major crystal plane or axis other than (100), (110), or (111) (e.g., (731) axis, crystal plane several degrees from (100) toward (011), etc.):

This subclass is indented under subclass 627. Subject matter wherein the major crystal plane or axis is other than (100), (110), or (111).

629 WITH MEANS TO CONTROL SURFACE EFFECTS:

This subclass is indented under the class definition. Subject matter wherein the active junction device has means to modify (e.g., reduce, or eliminate) electrical field effects which take place at the device surface or to modify (e.g., reduce or eliminate) inhomogeneities in electrical properties of a semiconductor crystal region due to effects caused by the discontinuity of the crystal lattice at the surface.

(1) Note. Such effects include formation of an inversion layer of minority carriers at the semiconductor surface, or depletion of majority carriers at the semiconductor surface, due to charge in an insulating coating on the surface or due to dangling bonds where the crystal structure of the semiconductor ends at the surface, leakage current via charge flow over a surface rather than through it, etc.

SEE OR SEARCH THIS CLASS, SUBCLASS:

487, for a semiconductor device provided with means to increase breakdown voltage of the device (which may involve surface effects).

630 With inversion-preventing shield electrode:
This subclass is indented under subclass 629. Subject matter wherein the means to control surface effects includes an electrode, insulated from the semiconductor surface, which electrode is configured to prevent inversion of the conductivity type of the surface due to surface effects.

631 In compound semiconductor material (e.g., GaAs):
This subclass is indented under subclass 629. Subject matter wherein the means to control surface effects are provided in a compound semiconductor material (e.g., GaAs).

632 Insulating coating:
This subclass is indented under subclass 629. Subject matter wherein there is a surface coating of electrically insulating material on the semiconductor body to control surface effects.

633 With thermal expansion compensation (e.g., thermal expansion of glass passivant matched to that of semiconductor):
This subclass is indented under subclass 632. Subject matter wherein the insulating coating includes means to compensate for mismatches in thermal expansion coefficient between different portions of the device, such as forming the insulating coating of a material which closely matches the thermal expansion coefficient of the underlying semiconductor.

(1) Note. Typical semiconductor materials, such as silicon, have extremely low thermal expansion coefficients, and thus, low thermal expansion materials such as Corning Code 7740 PYREX® borosilicate glass closely match the expansion coefficient of the semiconductor, and help to prevent thermal expansion induced stress or cracking.

634 Insulating coating of glass composition containing component to adjust melting or softening temperature (e.g., low melting point glass):
This subclass is indented under subclass 632. Subject matter wherein the insulating coating comprises a glass composition containing a component to adjust the melting or softening temperature.

(1) Note. A commonly used additive to lower the melting point of silica (silicon dioxide) is phosphorous oxide, producing phosphosilicate glass.

(2) Note. Such layers are typically provided so that the device can be heated to the softening point of the glass to cause it to flow and smooth out sharp edges on the semiconductor surface that might adversely affect subsequently deposited layers. Hence, such a layer is often called a reflow glass layer.

635 Multiple layers:
This subclass is indented under subclass 632. Subject matter wherein the insulating coating comprises multiple layers on the surface of the semiconductor body.

636 At least one layer of semi-insulating material:
This subclass is indented under subclass 635. Subject matter wherein at least one of the multiple insulating layers is made of a semi-insulating material (i.e., has a resistivity between that of a semiconductor and that of an insulator).

637 Three or more insulating layers:
This subclass is indented under subclass 635. Subject matter wherein there are three or more insulating coatings on the surface of the semiconductor body.

638 With discontinuous or varying thickness layer (e.g., layer covers only selected portions of semiconductor):
This subclass is indented under subclass 635. Subject matter wherein there are discontinuous or varying thickness layers in at least one of the multiple insulating layers over the semiconductor body.

639 At least one layer of silicon oxynitride:
This subclass is indented under subclass 635. Subject matter wherein at least one of the multiple insulating layers is made of a mixture of the oxides and nitrides of silicon.

640 At least one layer of silicon nitride:
This subclass is indented under subclass 635. Subject matter wherein there is at least one layer of silicon nitride in the multiple insulating layers on the semiconductor body.

641 Combined with glass layer:
This subclass is indented under subclass 640. Subject matter wherein in addition to the layer of silicon nitride, there is at least one layer of glass in the multiple insulating layers on the semiconductor body.

(1) Note. For purposes of the definitions of this class, a material is considered to be a glass if it is amorphous (i.e., non-crystalline, and its major constituents are a mixture of oxides of more than one element). An oxide of a single element, such as silicon dioxide, is not regarded as a glass layer, while a mixture of phosphorus oxide and silicon dioxide (phosphosilicate glass) would be regarded as a glass.

642 At least one layer of organic material:
This subclass is indented under subclass 635. Subject matter wherein at least one insulating layer comprises an organic compound, i.e., one which has a molecule characterized by two carbon atoms bonded together, one atom of carbon being bonded to at least one atom of hydrogen or a halogen, or one atom or carbon bonded to at least one atom of nitrogen by a single or double bond, certain compounds such as HCN, CN-CN, HNCO, HNCS, cyanogen halides, cyanamide, fulminic acid and metal carbides, being exceptions to this rule.

(1) Note. The definition of an organic compound here is the same as in Class 260, Chemistry of Carbon Compounds.

643 Polyimide or polyamide:
This subclass is indented under subclass 642. Subject matter wherein the at least one organic insulating layer comprises polyamide (i.e., a polymeric compound) resulting from replacement of an atom of hydrogen in an organic amine by an organic univalent acid radical, or polyimide, i.e., a polymeric compound resulting from replacement of both atoms of hydrogen in an organic amine by organic univalent acid radicals or by an organic divalent acid radical.

(1) Note. Polyamides are copolymers (polymers formed from at least two different starting organic materials) which have a linkage, as illustrated below, between the starting materials, where R is typically hydrogen and Q_1 and Q_2 are the organic residues of the starting monomers.

(2) Note. Linkage between the starting materials, illustrated below.

644 At least one layer of glass:
This subclass is indented under subclass 635. Subject matter wherein there is at least one layer of glass in the multiple insulating layers on the semiconductor body.

(1) Note. For purposes of the definitions of this class, a material is considered to be a glass if it is amorphous (i.e., non-crystalline) and its major constituents are a mixture of oxides of more than one element. An oxide of a single element, such as silicon dioxide, is not regarded as a glass layer, while a mixture of phosphorus oxide and silicon dioxide (phosphosilicate glass) would be regarded as a glass.

645 Insulating layer containing specified electrical charge (e.g., net negative electrical charge):
This subclass is indented under subclass 635. Subject matter wherein the multiple insulating layers, or at least one of the insulating layers, has a specified electrical charge.

646 Coating of semi-insulating material (e.g., amorphous silicon or silicon-rich silicon oxide):
This subclass is indented under subclass 632. Subject matter wherein the insulating layer is composed of a semi-insulating material.

647 Insulating layer recessed into semiconductor surface (e.g., LOCOS oxide):
This subclass is indented under subclass 632. Subject matter wherein the insulating layer is recessed into the semiconductor surface.

(1) Note. This type of recessed insulator may typically be LOCOS (Local Oxidation of Silicon) oxide, which is formed by oxidizing the silicon surface in areas not covered by an oxidation resistant mask, so that oxide is formed which is recessed into the semiconductor by approximately 1/2 of its thickness due to consumption of silicon to form the silicon oxide. LOCOS oxide may also be recessed fully to be substantially flush with the surface (except in areas at the edge of the oxide, wherein ridges known as "birdheads" (due to their shape) occur, which taper off to small thickness oxide portions in areas protected by the oxidation resistant mask (these tapering portions are called the "bird's beak").

648 Combined with channel stop region in semiconductor:
This subclass is indented under subclass 647. Subject matter wherein the recessed insulating layer is combined with a channel stop region, i.e., a region of heavy doping concentration in the underlying semiconductor surface to prevent inversion of the surface by formation of a layer of induced minority carriers.

649 Insulating layer of silicon nitride or silicon oxynitride:
This subclass is indented under subclass 632. Subject matter wherein the insulating layer is composed of silicon nitride or of a mixture of silicon oxide and silicon nitride.

650 Insulating layer of glass:
This subclass is indented under subclass 632. Subject matter wherein the insulating layer is composed of glass.

(1) Note. For purposes of the definitions of this class, a material is considered to be a glass if it is amorphous (i.e., non-crystalline) and its major constituents are a mixture of <u>oxides</u> of <u>more than one</u> element. An oxide of a single element, such as silicon dioxide, is not regarded as a glass layer, while a mixture of phosphorus oxide and silicon dioxide (phosphosilicate glass) would be regarded as a glass.

651 Details of insulating layer electrical charge (e.g., negative insulator layer charge):
This subclass is indented under subclass 632. Subject matter wherein the electrical charge characteristics of an insulating layer are specified.

652 Channel stop layer:
This subclass is indented under subclass 629. Subject matter wherein the means to control surface effects comprises a channel stop region (i.e., a region of heavy doping concentration in the underlying semiconductor surface to prevent inversion of the surface by formation of a layer of induced minority carriers).

SEE OR SEARCH THIS CLASS, SUBCLASS:

305, for insulated gate capacitor in trench or insulated gate transistor combined with capacitor in trench with a channel stop.

349, for SOI devices with buried channel stop layer.

354, for SOI devices with channel stop regions in single crystal island edges.

376, and 398 through 400, for IGFET integrated circuit devices with channel stop layers used to prevent parasitic conduction channels.

519, for integrated circuit devices with PN junction and dielectric in groove isolation with heavily doped channel stop region adjacent to groove.

653 WITH SPECIFIED SHAPE OF PN JUNCTION:
This subclass is indented under the class definition. Subject matter wherein the device has at least one junction between semiconductor regions of opposite conductivity type (P and N), and wherein the interface between at least one P region and its adjoining N region has a specified shape or geometrical configuration.

654 Interdigitated pn junction or more heavily doped side of junction is concave:
This subclass is indented under subclass 653. Subject matter wherein the device has at least one pn junction which is interdigitated (i.e., in which plural layers or fingers of n type material alternate with plural layers or fingers of p-type material, with then-type layers or fingers being parts of a single unitary n region and the p-type layers or fingers being parts of a single unitary p-region).

(1) Note. Interdigitated configurations are frequently used to increase the amount of PN junction area in a given volume of semiconductor material.

655 WITH SPECIFIED IMPURITY CONCENTRATION GRADIENT:
This subclass is indented under the class definition. Subject matter wherein the active solid-state device includes at least one region of semiconductor material with a specified profile or gradient of impurity doping concentration.

(1) Note. Examples of impurity concentration gradients include reverse gradient profiles (i.e., wherein the doping concentration is lighter toward the semiconductor surface or away from a pn junction) or a radial concentration profile).

SEE OR SEARCH THIS CLASS, SUBCLASS:
101, for light emitting devices with specified dopant concentration or concentration profile.
219, through 221, for charge transfer field effect majority signal carrier devices with impurity concentration variations (e.g., in the device channel).
335, through 343, for short channel IGFETs with graded dopant concentration in the active channel region that decreases with distance from the source region.
548, for integrated circuits with pn junction isolation having at least three regions of alternating conductivity types with dopant concentration gradients decreasing from the surface of the semiconductor.
596, and 597, for a voltage variable capacitance device with specified dopant profile (e.g., retrograde dopant profile).
929, for a pn junction isolated integrated circuit with isolation walls having minimum dopant concentration at an intermediate depth in an epitaxial layer.

656 With high resistivity (e.g., “intrinsic”) layer between P and N layers (e.g., PIN diode):
This subclass is indented under subclass 655. Subject matter wherein the device has a P doped region and an N doped region, separated by a region with very low impurity doping, so that the region is of high resistivity or “intrinsic” (undoped) semiconductor.

SEE OR SEARCH THIS CLASS, SUBCLASS:
458, for light responsive PIN devices

657 Stepped profile:
This subclass is indented under subclass 655. Subject matter wherein the device includes at least one region of the same conductivity type (P or N) wherein the doping concentration varies abruptly (e.g., a P+ to P- junction).

658 PLATE TYPE RECTIFIER ARRAY:
This subclass is indented under the class definition. Subject matter in which the device comprises plates of material each of which is coated with a layer of semiconductor material (e.g., copper oxide or selenium) which forms a rectifying barrier junction, the device being made up of several flat conductive plates and semiconductor material layers to form a rectifier array.

(1) Note. Typical rectifiers of this type include (a) copper oxide rectifiers in which the rectifying barrier is a junction between metallic copper plate and cuprous oxide layer coated on one side of the plate and (b) selenium rectifier in which a thin layer of selenium is formed on one side of an aluminum plate with a highly conductive metal coated over the selenium. If the semiconductor material is specifically recited as selenium or tellurium, or an oxide of a metal such as copper oxide, the patent will be classi-

fied in the appropriate one of subclasses 42 or 43.

(2) Note. This type of device has generally been replaced with more modern devices, including silicon rectifiers.

659 WITH SHIELDING (E.G., ELECTRICAL OR MAGNETIC SHIELDING, OR FROM ELECTROMAGNETIC RADIATION OR CHARGED PARTICLES):

This subclass is indented under the class definition. Subject matter in which means is provided for protecting an active solid-state device by providing a barrier to prevent electrical or magnetic radiation or fields or charged particles from reaching the device, or to limit the amount of such radiation or particles reaching the device.

(1) Note. This subject matter is to be distinguished from that found in the cross-reference art collection entitled "radiation hardening", which encompasses subject matter which does not attempt to shield the device from electric or magnetic or electromagnetic radiation or charged particles, but is used to prevent or limit the damage caused to a device by such radiation or particles which reach the device.

SEE OR SEARCH THIS CLASS, SUBCLASS:

297, for shielding against alpha particles in dynamic random access memory (DRAM) structures.

422, for magnetic field shielding in magnetic field sensor active solid-state devices.

435, for light shields in light responsive active solid-state devices.

SEE OR SEARCH CLASS:

174, Electricity: Conductors and Insulators, subclasses 32 through 397 for miscellaneous anti-inductive structures, particularly subclasses 350-397 for miscellaneous electrical shields and screen structures not elsewhere classifiable.

307, Electrical Transmission or Interconnection Systems, subclass 91 for anti-induction or coupling to other systems with magnetic or electrostatic field control (e.g., shielding).

315, Electric Lamp and Discharge Devices: Systems, subclass 85 for gaseous tube systems with electromagnetic wave radiation prevention or shielding means.

330, Amplifiers, subclass 68 for amplifiers with shielding means.

331, Oscillators, subclass 67 for oscillators combined with electromagnetic or electrostatic shield means.

333, Wave Transmission Lines and Networks, subclass 12 for transmission line inductive or radiation interference systems.

334, Tuners, subclass 85 for radio tuners with shielding means.

336, Inductor Devices, subclass 84 for induction devices with electric or magnetic shield means.

338, Electrical Resistors, subclass 64 for electrical resistors with electrical shield means.

343, Communications: Radio Wave Antennas, subclasses 841+ for antenna structure with electric shield means.

348, Television, subclasses 825+ a for cathode-ray tube support and 836+ for cabinet or chassis of a television receiver in general.

361, Electricity: Electrical Systems and Devices, subclasses 816+ for radio interference type shielding means.

660 With means to shield device contained in housing or package from charged particles (e.g., alpha particles) or highly ionizing radiation (i.e., hard X-rays or shorter wavelength):

This subclass is indented under subclass 659. Subject matter wherein the device is provided with means to shield it from charged particles or highly ionizing radiation contained in a housing or package separate and apart from the shielding means.

661 SUPERCONDUCTIVE CONTACT OR LEAD:

This subclass is indented under the class definition. Subject matter wherein an active solid-state device contains, or is connected to, an electrical contact or lead (pronounced "leed")

which is made of a material whose electrical resistivity drops to zero at a particular temperature called a critical transition temperature (Tc).

SEE OR SEARCH CLASS:

174, Electricity: Conductors and Insulators, subclasses 15.4+ and 125.1 for superconducting conductors.

438, Semiconductor Device Manufacturing: Process, particularly subclass 2 for methods of forming an semiconductor device having a superconductive component thereon.

505, Superconductor Technology: Apparatus, Material, Process, subclass 1 for high temperature superconductor materials and subclasses 884+ for superconductive electrical conductors.

662 Transmission line or shielded:

Subject matter under 661 in which the superconductive electrical lead has controlled electrical characteristics designed to convey high frequency (e.g., greater than 3 megahertz) signals or narrow pulse signals; or is surrounded by a separate electrical conductor or envelope, called a shield, designed to minimize the effects of nearby electrical circuits.

SEE OR SEARCH CLASS:

174, Electricity: Conductors and Insulators, subclasses 32 through 397 for miscellaneous anti-inductive structures, particularly subclasses 350-397 for miscellaneous electrical shields and screen structures not elsewhere classifiable.

307, Electrical Transmission or Interconnection Systems, subclass 91 for anti-induction or coupling to other systems with magnetic or electrostatic field control (e.g., shielding).

315, Electric Lamp and Discharge Devices: Systems, subclass 85 for gaseous tube systems with electromagnetic wave radiation prevention or shielding means.

330, Amplifiers, subclass 68 for amplifiers with shielding means.

331, Oscillators, subclass 67 for oscillators combined with electromagnetic or electrostatic shield means.

333, Wave Transmission Lines and Networks, subclass 12 for transmission line inductive or radiation interference systems.

334, Tuners, subclass 85 for radio tuners with shielding means.

336, Inductor Devices, subclass 84 for induction devices with electric or magnetic shield means.

338, Electrical Resistors, subclass 64 for electrical resistors with electrical shield means.

343, Communications: Radio Wave Antennas, subclasses 841+ for antenna structure with electric shield means.

348, Television, subclass 820 for a cathode-ray tube video display with electric or magnetic shielding means.

361, Electricity: Electrical Systems and Devices, subclasses 816+ for radio interference type shielding means.

663 On integrated circuit:

Subject matter under 661 in which the superconductive contact or lead is associated with an electrical network made up of more than one electronic device, including at least one active solid-state electronic device, in a unitary structure.

664 TRANSMISSION LINE LEAD (E.G., STRIPLINE, COAX, ETC.):

This subclass is indented under the class definition. Subject matter wherein an active solid-state device is provided with an electrical connection or lead with controlled electrical characteristics used to transmit high-frequency, e.g., greater than 3 megahertz, or narrow pulse signals to or from the device.

SEE OR SEARCH CLASS:

333, Wave Transmission Lines and Networks, appropriate subclasses for transmission lines, per se.

665 CONTACTS OR LEADS INCLUDING FUSIBLE LINK MEANS OR NOISE SUPPRESSION MEANS:

This subclass is indented under the class definition. Subject matter wherein an active solid-state device is provided with electrical contacts or leads (pronounced “leeds”) which contain portions which have a composition or are made

so that they will melt at a relatively low temperature to form an open circuit and thereby protect the device in case excessive current, e.g., a current spike from lightning, or voltage is provided to the contact or lead, or contains means designed to suppress unwanted electrical disturbances in the electrical contacts or leads.

SEE OR SEARCH CLASS:

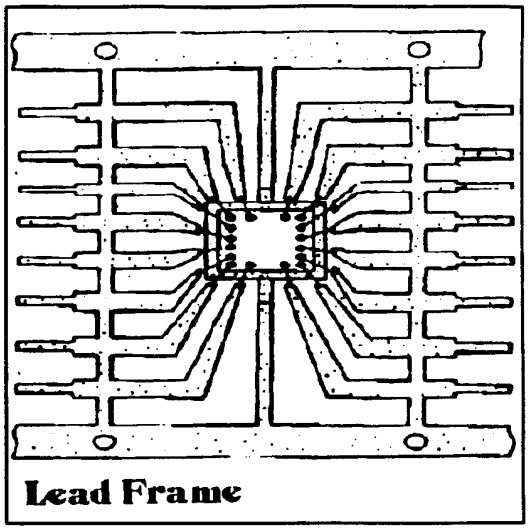
365, Static Information Storage and Retrieval, subclass 96 for a fusible link storage member.

666 LEAD FRAME:

This subclass is indented under the class definition. Subject matter wherein the active solid-state device is provided with a conductive metal network which may have relatively large area portions, commonly called pads or flags, for direct contact with semiconductor chips or dice, and lead elements for facilitating electrical interconnection of the chips or dies via intermediate (e.g., jumper) connections to other electronic devices or components.

(1) Note. Lead frames also have other portions, usually called "ties", which interconnect the pad or flag portions with the lead portions prior to assembly of the lead frame in an electronic package or housing, but which are removed during package assembly.

(1) Note. See the illustration, below:



SEE OR SEARCH CLASS:

29, Metal Working, subclasses 739+, especially subclass 741, for means to fasten electrical component to wiring means, base, or substrate, including a multi-lead component; and subclass 834 for beam lead frames or beam lead devices.

174, Electricity: Conductors and Insulators, subclass 529 for flat pack electronic device mounting means.

361, Electricity: Electrical Systems and Devices, subclass 813 for lead frames, per se, not associated with a solid-state active electronic device of the type classified in Class 257.

428, Stock Material or Miscellaneous Articles, subclasses 571+ for stock materials of metal which have marginal indexing features or weakened portion for severing. Lead frames are commonly made in long strips of repeating patterns with such indexing and/or severing features.

438, Semiconductor Device Manufacturing: Process, particularly subclasses 111+ and 123+ for methods of packaging utilizing a lead frame; see the search notes therein.

667 With dam or vent for encapsulant:
This subclass is indented under subclass 666. Subject matter with a portion or portions to block encapsulant flow, typically from flowing out of a mold during an encapsulation process, or vent means (e.g., grooves in lead frame leads) to permit egress to the atmosphere for air or other gases which are inside a mold during encapsulation.

668 On insulating carrier other than a printed circuit board:
This subclass is indented under subclass 666. Subject matter wherein the lead frame is mounted on an insulating carrier other than a printed circuit board.

(1) Note. Printed circuit boards alone, or with one or more solid-state electronic devices mounted thereon are not classified herein, but are found in Class 174, Electricity: Conductors and Insulators, or Class 361, Electricity: Electrical Systems and Devices. See the class definitions for Classes 174 and 361 for the line of demarkation between these two classes.

SEE OR SEARCH CLASS:
174, Electricity: Conductors and Insulators, subclasses 260 and 520 for printed circuit boards in combination with one or more electronic solid-state devices.

669 With stress relief:
This subclass is indented under subclass 666. Subject matter wherein means are provided to alleviate stresses and strains (e.g., mechanical or thermal stresses) to which a lead frame is subjected.

670 With separate tie bar element or plural tie bars:
This subclass is indented under subclass 666. Subject matter in which a frame element used to tie or connect a semiconductor chip pad/flag and/or lead fingers frame members is a separate element and not part of the lead frame itself or wherein plural tie bar elements are provided as part of a lead frame.

671 Of insulating material:
This subclass is indented under subclass 670. Subject matter wherein the separate tie bar element or the plural tie bars are made of electrically insulating material.

672 Small lead frame (e.g., "spider" frame) for connecting a large lead frame to a semiconductor chip:
This subclass is indented under subclass 666. Subject matter wherein the means used to interconnect a chip or die to a large lead frame is a small lead frame with contact elements radiating <u>from</u> a central location for interconnection with a chip mounted on a large lead frame chip pad at that location <u>to</u> peripheral locations for interconnection with large lead frame leads.

673 With bumps on ends of lead fingers to connect to semiconductor:
This subclass is indented under subclass 666. Subject matter wherein bump contacts are located at or near the ends of lead fingers to provide contact with a semiconductor chip.

674 With means for controlling lead tension:
This subclass is indented under subclass 666. Subject matter wherein means are provided for controlling the tension under which an electrical lead is placed including, for example, a bend in the lead, an area of reduced lead thickness, etc.

675 With heat sink means:
This subclass is indented under subclass 666. Subject matter wherein a heat sink means is provided, either as part of the lead frame or in addition to the lead frame for cooling the active solid-state device.

676 With structure for mounting semiconductor chip to lead frame (e.g., configuration of die bonding flag, absence of a die bonding flag, recess for LED):
This subclass is indented under subclass 666. Subject matter wherein the lead frame is provided with specified structure means to mount a semiconductor chip thereto, or is specified to not have a pad for mounting the chip.

(1) Note. This structure may, for example, have a particular configuration such as a flag shape.

677 Of specified material other than copper (e.g., Kovar (T.M.)):
This subclass is indented under subclass 666. Subject matter wherein the electrically conductive lead frame is made up of a specific material other copper, which is a common material for lead frames.

678 HOUSING OR PACKAGE:
This subclass is indented under the class definition. Subject matter wherein preformed physical means to cover or protect a solid-state electronic device is provided therefor.

SEE OR SEARCH THIS CLASS, SUBCLASS:
81, and 82, for a light emitting device in combination with or also constituting a light responsive device and with specific housing structure.
99, for light emitting device with specific housing structure.
177, through 182, for a regenerative type switching device with housing or external electrode.
433, and 434, for light responsive device with housing or encapsulation means.
573, for Darlington configuration bipolar transistor structure with housing or contact structure.
584, for enlarged emitter device bipolar transistor means having housing or contact.
602, for a voltage variable capacitance device with specified housing or contact.
660, for means to shield a device contained in a housing.

SEE OR SEARCH CLASS:
361, Electricity: Electrical Systems or Devices, subclasses 679+ for housings and mounting assemblies for electronic devices and components.
438, Semiconductor Device Manufacturing: Process, particularly subclasses 106+ for methods of packaging; see the search notes therein.

679 Smart (e.g., credit) card package:
Subject matter under 678 wherein the housing or package is in a form which permits it to be used as a credit card.

(1) Note. A smart card is one which contains a microprocessor chip.

SEE OR SEARCH CLASS:
235, Registers, subclass 487 and indented subclasses for coded records including electronic credit cards, per se.
361, Electricity: Electrical Systems and Devices, subclasses 736+ and 752+ for modules for printed circuits or housing or chassis for printed circuit boards.

680 With window means:
Subject matter under 678 wherein the housing or package has a physical opening or area otherwise transparent to ultraviolet, visible, or infrared light.

681 For erasing EPROM:
This subclass is indented under subclass 680. Subject matter wherein the window means is provided for transmitting light to erase an electrically programmable read-only memory (EPROM).

682 With desiccant, getter, or gas filling:
This subclass is indented under subclass 678. Subject matter including a desiccant (i.e., a material for absorbing moisture); a getter (i.e., a material which absorbs undesirable semiconductor, housing or package contaminants); or wherein a gaseous material fills the housing or package.

683 With means to prevent explosion of package:
This subclass is indented under subclass 678. Subject matter including means to prevent explosion of a housing or package.

684 With semiconductor element forming part (e.g., base, of housing):
This subclass is indented under subclass 678. Subject matter wherein part of the housing is formed by a semiconductor element.

(1) Note. The semiconductor element may have an inactive portion connected to the rest of the housing, and another portion forming an active device, for example. Frequently the semiconductor element

forms the base of the housing, through which leads are inserted.

685 Multiple housings:
This subclass is indented under subclass 678. Subject matter wherein more than one housing is provided for a solid-state active electronic device, or wherein plural housings, each containing one or more solid-state active devices, are constructed as a unitary structure.

(1) Note. One housing may be located within another housing.

686 Stacked arrangement:
This subclass is indented under subclass 685. Subject matter wherein a plurality of housings are placed one upon another, vertically.

687 Housing or package filled with solid or liquid electrically insulating material:
This subclass is indented under subclass 678. Subject matter wherein the housing or package is filled with a solid or liquid electrically insulating material.

(1) Note. Encapsulated devices are excluded from this subclass and are not considered to be housings or packages as defined in subclass 678 which requires them to be preformed.

SEE OR SEARCH CLASS:
361, Electricity: Electrical Systems and Devices, subclasses 729, 730+, and 744+ for various modules for printed circuit boards.

688 With large area flexible electrodes in press contact with opposite sides of active semiconductor chip and surrounded by an insulating element, e.g., ring:
This subclass is indented under subclass 678. Subject matter wherein the package or housing has two large area electrodes which are in press contact with opposite sides of a semiconductor chip and wherein the electrode edges are surrounded by an electrically insulating medium (e.g., a ring).

(1) Note. Search this class, subclass 181 for such housings which specifically contain a regenerative active solid-state device (e.g., an SCR or thyristor).

SEE OR SEARCH THIS CLASS, SUBCLASS:
181+, for similar electrodes with regenerative type devices.
785, for electrodes combined with an active semiconductor electronic device by pressure alone.

689 Rigid electrode portion:
This subclass is indented under subclass 688. Subject matter wherein the large area electrodes are rigid in whole or in part.

(1) Note. These type devices typically employ relatively massive electrodes to operate at large current densities.

690 With contact or lead:
This subclass is indented under subclass 678. Subject matter wherein the device is provided with a contact or lead, in addition to or as part of the package or housing.

691 Having power distribution means (e.g., bus structure):
This subclass is indented under subclass 690. Subject matter wherein the contact or lead includes means for distributing electrical power to one or more active solid-state devices within the package or housing.

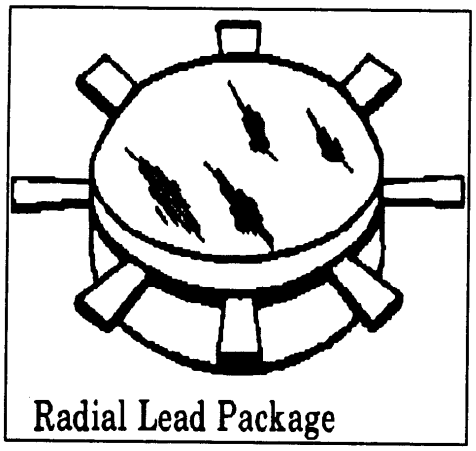
692 With particular lead geometry:
This subclass is indented under subclass 690. Subject matter wherein the contact or lead provided as part of or in addition to the package or housing has a specified geometrical configuration.

693 External connection to housing:
This subclass is indented under subclass 692. Subject matter wherein the contact or lead having a specified geometry comprises an electrical connection for connecting the package or housing and its contained active solid-state device to other electrical devices or circuits.

694 Axial leads:
This subclass is indented under subclass 693. Subject matter wherein the leads or contacts which form an external connection to the housing or package extend out opposite ends along an axis of symmetry of a housing or package.

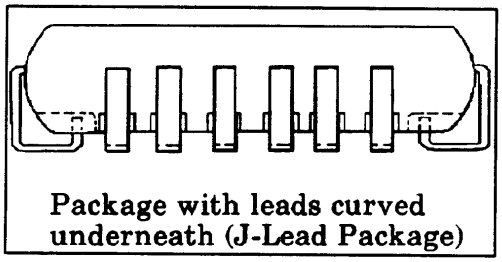
695 Fanned/radial leads:
This subclass is indented under subclass 693. Subject matter wherein the leads or contacts which form an external connection to the housing or package extend radially outward from the package.

(1) Note. See illustration, below.



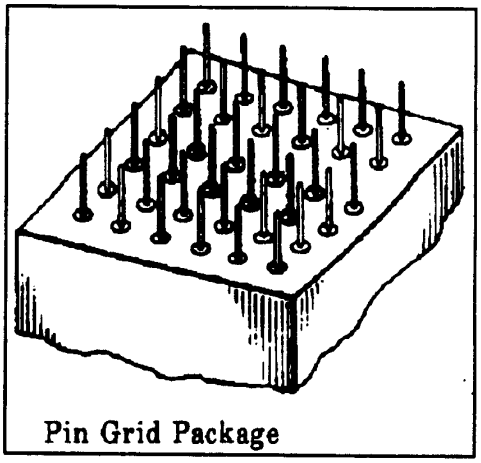
696 Bent (e.g., J-shaped) lead:
This subclass is indented under subclass 693. Subject matter wherein the leads or contacts which form an external connection to the housing or package include one or more leads which have a curved end portion (e.g., for mounting on the top surface of a printed circuit board).

(1) Note. See illustration, below.



697 Pin grid type:
This subclass is indented under subclass 693. Subject matter wherein the leads or contacts which form an external connection to the housing or package are in the form of a grid or matrix of elongated pins.

(1) Note. See illustration, below.



698 With specific electrical feedthrough structure:
This subclass is indented under subclass 690. Subject matter wherein a specific structure is provided for feeding electrical contacts or leads into or out of the housing or package.

699 Housing entirely of metal except for feedthrough structure:
Subject matter under 698 wherein the housing or package is made entirely of metal except for the portion wherein the electrical contacts or leads are fed through.

(1) Note. Typically, an insulator is placed in the feedthrough portion of a metal housing to prevent electrical short circuiting of the leads to the housing.

700 Multiple contact layers separated from each other by insulator means and forming part of a package or housing (e.g., plural ceramic layer package):
This subclass is indented under subclass 690. Subject matter wherein the housing or package combined with a contact or lead structure is in the form of a multiple layered insulating com-

posite with plural electrical connection layers located between layers of insulator material.

701 Insulating material:
This subclass is indented under subclass 678. Subject matter wherein the housing or package is made of an electrically insulating material.

702 Of insulating material other than ceramic:
Subject matter under 701 wherein the housing is made of electrically insulating material other than ceramic (e.g., the housing is made of glass or of a single crystal insulator material).

(1) Note. A ceramic is a polycrystalline, non-metallic, non-organic material, such as fired polycrystalline aluminum oxide, typically made by firing a compressed and shaped powder at high temperatures to fuse the powder together.

703 Composite ceramic, or single ceramic with metal:
This subclass is indented under subclass 701. Subject matter wherein the housing is a composite made up of at least two ceramic materials (e.g., alumina and beryllia) or of a single ceramic material with a metal.

704 Cap or lid:
This subclass is indented under subclass 701. Subject matter wherein the housing or package is provided with a cap or lid.

705 Of high thermal conductivity ceramic (e.g., BeO):
This subclass is indented under subclass 701. Subject matter wherein the housing is made of ceramic which has high thermal conductivity to promote heat dissipation from the housing.

706 With heat sink:
This subclass is indented under subclass 701. Subject matter wherein the insulating housing has a heat sink to dissipate heat.

(1) Note. The heat sink may be located in a cavity in a base member made of ceramic material.

SEE OR SEARCH CLASS:
174, Electricity: Conductors and Insulators, appropriate subclasses directed to cooling means.
361, Electricity: Electrical Systems and Devices, subclasses 688 through 723 for cooling means for electronic devices or components with housings or mounting assemblies.

707 Directly attached to semiconductor device:
This subclass is indented under subclass 706. Subject matter wherein the heat sink is attached directly to the semiconductor device.

708 Entirely of metal except for feedthrough:
This subclass is indented under subclass 678. Subject matter wherein the housing or package is made entirely of metal except for the portion wherein the electrical contacts or leads are fed through.

(1) Note. Typically, an insulator is placed in the feedthrough portion of a metal housing to prevent electrical short circuiting of the leads to the housing.

709 With specified insulator to isolate device from housing:
This subclass is indented under subclass 708. Subject matter wherein a specific insulator means is provided to electrically isolate the active solid-state device contained in the metal package or housing from the metal package or housing to prevent electrical short circuits due to the housing or package.

710 With specified means (e.g., lip) to seal base to cap:
This subclass is indented under subclass 708. Subject matter wherein specific means are provided to seal the cap to the base such as, for example, a bead or lip or boss around the periphery of the base.

711 With raised portion of base for mounting semiconductor chip:
This subclass is indented under subclass 708. Subject matter wherein a portion of the base is raised above the rest of the base and the raised portion provides a base on which to mount a semiconductor chip with an active solid-state device therein or thereon.

712 With provision for cooling the housing or its contents:
This subclass is indented under subclass 678. Subject matter wherein means for cooling the housing or its contents are provided in addition to natural cooling processes.

SEE OR SEARCH CLASS:
174, Electricity: Conductors and Insulators, appropriate subclasses directed to cooling means.
361, Electricity: Electrical Systems and Devices, subclasses 688 through 723, for cooling means for electronic devices or components with housings or mounting assemblies.

713 For integrated circuit:
This subclass is indented under subclass 712. Subject matter wherein the solid-state electronic device for which cooling means is provided is an integrated circuit, which is a semiconductor substrate which contains a plurality of active solid-state electronic devices.

714 Liquid coolant:
This subclass is indented under subclass 712. Subject matter wherein the means provided for cooling the housing or its contents is a liquid.

715 Boiling (evaporative) liquid:
This subclass is indented under subclass 714. Subject matter wherein the cooling means involves boiling a liquid to provide evaporative cooling.

SEE OR SEARCH CLASS:
174, Electricity: Conductors and Insulators, appropriate subclasses directed to liquid cooling means.
361, Electricity: Electrical Systems and Devices, subclasses 699+ for liquid cooling means for electronic devices or components with housings or mounting assemblies.

716 Cryogenic liquid coolant:
This subclass is indented under subclass 714. Subject matter wherein the cooling means uses a liquid to maintain device temperatures at or below 100 degrees Kelvin.

SEE OR SEARCH CLASS:
174, Electricity: Conductors and Insulators, appropriate subclasses directed to liquid cooling means.
361, Electricity: Electrical Systems and Devices, subclasses 699+ for liquid cooling means for electronic devices or components with housings or mounting assemblies.

717 Isolation of cooling means (e.g., heat sink) by an electrically insulating element (e.g., spacer):
This subclass is indented under subclass 712. Subject matter wherein an insulating element is used to physically separate a cooling means from an active solid-state electronic device or a housing therefor.

718 Heat dissipating element held in place by clamping or spring means:
This subclass is indented under subclass 712. Subject matter wherein an element for dissipating heat is held in place by means to clamp it to the device or vice versa, or by a spring to position the device and heat dissipating element in thermal contact with each other.

719 Pressed against semiconductor element:
This subclass is indented under subclass 718. Subject matter wherein the heat dissipating element and the active device are in press contact with each other.

720 Heat dissipating element has high thermal conductivity insert (e.g., copper slug in aluminum heat sink):
This subclass is indented under subclass 712. Subject matter wherein the heat dissipating element has a relatively high thermal conductivity vis-a-vis a larger (main) heat sink into which it is inserted (e.g., a copper slug in an aluminum heat sink).

721 With gas coolant:
This subclass is indented under subclass 712. Subject matter wherein the cooling means uses a gas to provide the cooling (e.g., by convection).

722 With fins:
This subclass is indented under subclass 721. Subject matter wherein the cooling means has fins, i.e., long, thin, blade like structures used to dissipate heat to the gas coolant.

723 For plural devices:
This subclass is indented under subclass 678. Subject matter wherein a package or housing is provided for more than one electronic device, at least one of the electronic devices being an active solid-state device.

SEE OR SEARCH CLASS:
174, Electricity: Conductors and Insulators, subclasses 50+ for housings and printed circuits.
361, Electricity: Electrical Systems and Devices, subclasses 729 and 730+ for plural housing modules.

724 With discrete components:
This subclass is indented under subclass 723. Subject matter wherein at least some of the electronic components are in the form of an individual device per semiconductor chip, as contrasted to a single integrated circuit containing plural semiconductor devices. The discrete components may be active solid-state devices or passive components such as resistors, capacitors, or inductors.

725 With electrical isolation means:
This subclass is indented under subclass 723. Subject matter wherein means are provided to electrically isolate the plural devices from each other.

726 Devices held in place by clamping:
This subclass is indented under subclass 725. Subject matter wherein the plural devices which are electrically isolated are held in place by clamp means, i.e., by means which press devices into place.

727 Device held in place by clamping:
This subclass is indented under subclass 678. Subject matter wherein at least one of the plural devices is held in place by clamp means (i.e., by means which press a device into place).

728 For high frequency (e.g., microwave) device:
This subclass is indented under subclass 678. Subject matter wherein the active solid-state device provided with a housing or package is a high frequency solid-state electronic device operating at high frequencies, such as microwave frequencies or above.

729 Portion of housing of specific materials:
This subclass is indented under subclass 678. Subject matter wherein at least a portion of the housing or package is made of specific materials.

730 Outside periphery of package having specified shape or configuration:
This subclass is indented under subclass 678. Subject matter wherein the outside periphery of a package or housing has a particular shape or configuration.

731 With housing mount:
This subclass is indented under subclass 678. Subject matter wherein the housing or package has means (e.g., a flange or threaded stud) for attaching the housing to a support.

(1) Note. Search this class, subclass 180 for housings or packages of this type which specifically contain a regenerative type switching device such as an SCR or thyristor.

732 Flanged mount:
This subclass is indented under subclass 731. Subject matter wherein the housing mount is a flange with openings therein (e.g., threaded holes) to permit the housing to be attached (e.g., by fasteners) to a support.

733 Stud mount:
This subclass is indented under subclass 731. Subject matter wherein the housing mount is a threaded element shaped like a bolt extending from the housing for fastening into a threaded hole in a support.

734 COMBINED WITH ELECTRICAL CONTACT OR LEAD:
This subclass is indented under the class definition. Subject matter wherein the active solid-state device is provided with one or more electrical contacts or leads.

SEE OR SEARCH THIS CLASS, SUBCLASS:

41, for point contact rectifiers.

44, through 47, for devices with a metal contact alloyed to elemental semiconductor type PN junction in a non-regenerative structure.

54, for Schottky barrier to amorphous semiconductor material device.

73, for Schottky barrier to polycrystalline semiconductor material device.

81, and 82, for light emitter combined with or also constituting a light responsive device and having a specific housing or contact structure.

91, for plural light emitting devices with shaped contacts or opaque masking.

99, for light emitting devices with specified housing or contact structure.

145, for a regenerative type device combined with a FET with extended latching current level and a low impedance channel contact extending below the device surface.

155, and 156, for a regenerative type device with switching speed enhancing means (e.g., a Schottky contact).

177, through 182, for a regenerative type device with housing or external electrode.

217, for a majority signal carrier charge transfer device with a conductive means in direct contact with channel (e.g., a non-insulated gate).

260, for JFET having the same channel controlled by, for example, Schottky barrier and pn junction gates.

276, for a JFET in a microwave integrated circuit with a contact or heat sink extending through a hole in the semiconductor.

280, through 284, for JFETs with a Schottky gate electrode.

316, through 322, for a variable threshold insulated electrical field effect device with additional contacted control electrode.

343, for graded channel dopant IGFET device with plural sections connected in parallel and having all contacts on the same surface.

382, through 385, for an IGFET in an integrated circuit with a refractory material contact to source or drain region.

449, through 457, for Schottky contacts in light responsive devices.

471, through 486, for Schottky contact devices.

502, for high power integrated circuit devices with electrical isolation and a backside collector contact.

503, for an integrated circuit device with electrically isolated components having a contact or metallization configuration to reduce parasitic coupling.

522, for beam-lead supported semiconductor islands in integrated circuits.

573, for Darlington configuration non-isolated bipolar transistors with resistance means connected between transistor base regions and with housing or contact structure or configuration.

576, for complementary bipolar transistors sharing a common active region (e.g., IIL, I^2L) including lateral bipolar transistor structure and having contacts of a refractory material.

584, for bipolar transistor device with enlarged emitter area and with housing or contact means.

602, for a voltage variable capacitance device with specified housing or contact.

621, for a semiconductor device with electrical contact in a hole in the semiconductor (e.g., lead extends through semiconductor body).

624, for mesa structure device having a low resistance ohmic connection along a mesa edge.

661, through 663, for superconductive contacts or leads.

664, for transmission line leads.

665, for contacts or leads including fusible link or noise suppression means.

666, through 677, for lead frames.

688, and 689, for housings with large area flexible electrodes in press contact with opposite sides of active semiconductor chip and surrounded by an insulating element.

690, through 700, for housings with specified contact or lead.

905, for plural DRAM cells sharing a common contact or common trench.
926, for a device with an elongated lead extending axially through another elongated lead.
928, for shorted pn or Schottky junction other than an emitter junction.

SEE OR SEARCH CLASS:
174, Electricity: Conductors and Insulators, subclasses 99+ for bus bar structure, per se.
361, Electricity: Electrical Systems and Devices, subclasses 772 through 776 for specific lead configurations connecting electronic systems and devices to printed circuit boards.

735 Beam leads (i.e., leads that extend beyond the ends or sides of a chip component):
This subclass is indented under subclass 734. Subject matter wherein electrical contact leads extend like beams beyond the ends of a chip component.

SEE OR SEARCH CLASS:
438, Semiconductor Device Manufacturing: Process, particularly subclass 411 for methods of forming electrically isolated semiconductor islands held in place by beam lead metallization; subclass 461 for methods of forming beam leads on a semiconductor substrate combined with dicing of the substrate into plural separate bodies; and subclass 611 for methods of forming beam lead metallization on a semiconductor substrate.

736 Layered:
This subclass is indented under subclass 735. Subject matter wherein the leads are made of at least two separate layers of the same or different material.

737 Bump leads:
This subclass is indented under subclass 734. Subject matter wherein an electrical contact is in the form of a relatively abrupt protuberance on the surface of a solid-state electronic device or chip/die containing such a device.

738 Ball shaped:
This subclass is indented under subclass 737. Subject matter wherein the bump contacts have the spherical shape of a ball.

SEE OR SEARCH THIS CLASS, SUBCLASS:
780, for ball shaped bonds, generally.

739 With textured surface:
This subclass is indented under subclass 734. Subject matter wherein the surface of the contact or lead is rough or has a characteristic of a closely interwoven fabric, rather than being smooth.

740 With means to prevent contact from penetrating shallow PN junction (e.g., prevention of aluminum "spiking"):
This subclass is indented under subclass 734. Subject matter wherein means are provided for preventing an electrical contact from penetrating into the relatively thin PN junction region.

(1) Note. This penetration is sometimes referred to as "spiking", and if the contact material is aluminum, prevention of this phenomenon is known as prevention of aluminum spiking.

741 Of specified material other than unalloyed aluminum:
This subclass is indented under subclass 734. Subject matter wherein the contact or lead is made of a specified material other than an aluminum alloy.

742 With a semiconductor conductivity substitution type dopant (e.g., germanium in the case of a gallium arsenide semiconductor) in a contact metal):
This subclass is indented under subclass 741. Subject matter wherein the contact metal is doped with atoms of an element, e.g., germanium in the case of a semiconductor of gallium arsenide, which changes the conductivity of (i.e., introduces holes or electrons into) the semiconductor material to which the contact is connected.

743 For compound semiconductor material:
This subclass is indented under subclass 742. Subject matter in which the electrical contact material contacts and contains a dopant for a semiconductor material which is a chemical compound, as contrasted to an elemental semiconductor.

744 For compound semiconductor material:
This subclass is indented under subclass 741. Subject matter in which the electrical contact material contacts a semiconductor material which is a chemical compound, as contrasted to an elemental semiconductor.

745 Contact for III-V material:
This subclass is indented under subclass 744. Subject matter in which the compound semiconductor material is a group III-V compound, i.e., one component is from periodic table group III and the other is from periodic table group V.

746 Composite material (e.g., fibers or strands embedded in solid matrix):
This subclass is indented under subclass 741. Subject matter in which the semiconductor contact material is formed as a composite of, for example, fibers or strands embedded in a solid matrix.

747 With thermal expansion matching of contact or lead material to semiconductor active device:
This subclass is indented under subclass 741. Subject matter in which the electrical contact or lead material is chosen to have a coefficient of thermal expansion which closely matches that of the semiconductor active device material.

SEE OR SEARCH THIS CLASS, SUBCLASS:
178, for regenerative device with housing and means to avoid stress (e.g., thermal matching of electrode to semiconductor).
633, for thermal expansion compensation between semiconductor and insulating coating.

748 Plural layers of specified contact or lead material:
This subclass is indented under subclass 747. Subject matter wherein the thermal expansion matching lead material is layered.

749 At least portion of which is transparent to ultraviolet, visible or infrared light:
This subclass is indented under subclass 741. Subject matter wherein at least part of the contact or lead is transparent to ultraviolet, visible, or infrared light.

SEE OR SEARCH THIS CLASS, SUBCLASS:
59, for FET devices in amorphous material with transparent electrode.
72, for FET devices in non-single crystal semiconductor material with transparent electrode.
449, for light responsive devices with transparent Schottky barrier.

750 Layered:
This subclass is indented under subclass 741. Subject matter wherein the specified contact material is layered.

751 At least one layer forms a diffusion barrier:
This subclass is indented under subclass 750. Subject matter wherein at least one layer forms a barrier to the diffusion of the contact material into the semiconductor or into another contact layer.

SEE OR SEARCH THIS CLASS, SUBCLASS:
486, for Schottky barrier layers including a diffusion barrier material.

752 Planarized to top of insulating layer:
This subclass is indented under subclass 750. Subject matter wherein a contact or lead and an insulating layer to which it is connected form a single planar surface.

753 With adhesion promoting means (e.g., layer of material) to promote adhesion of contact to an insulating layer:
This subclass is indented under subclass 750. Subject matter wherein a means, e.g., a layer of material, is provided to promote adhesion of an

electrical contact or lead to an insulating surface.

754 At least one layer of silicide or polycrystalline silicon:
This subclass is indented under subclass 750. Subject matter wherein at least one layer of material is made up of a silicide or polycrystalline silicon.

SEE OR SEARCH THIS CLASS, SUBCLASS:
381, and 538, for polycrystalline silicon resistive elements connected to active semiconductor electronic devices.
554, and 588, for bipolar transistor devices with a polycrystalline semiconductor connection electrode.

755 Polysilicon laminated with silicide:
This subclass is indented under subclass 754. Subject matter wherein the layers include a polysilicon laminated with a silicide.

(1) Note. Such laminated contacts of polysilicon and silicide are sometimes called "polycide" contacts.

756 Multiple polysilicon layers:
This subclass is indented under subclass 754. Subject matter wherein a layered electrical contact or lead includes multiple polysilicon layers.

757 Silicide of refractory or platinum group metal:
This subclass is indented under subclass 754. Subject matter wherein a layered electrical contact or lead includes a silicide of a metal found in groups IVA, VA, VIA or VIIIA (other than iron (Fe), nickel (Ni) or cobalt (Co)) of the periodic table of the elements.

758 Multiple metal levels on semiconductor, separated by insulating layer (e.g., multiple level metallization for integrated circuit):
This subclass is indented under subclass 750. Subject matter wherein there are plural layers of metal forming electrical contact material, the layers being separated by intervening layers of insulator material.

SEE OR SEARCH THIS CLASS, SUBCLASS:
211, for gate arrays with multi-level metallization.

SEE OR SEARCH CLASS:
156, Adhesive Bonding and Miscellaneous Chemical Manufacture, subclasses 60+, for processes of uniting plural bodies via an adhesive material.
438, Semiconductor Device Manufacturing: Process, particularly subclasses 118+ for methods of packaging a semiconductor device including a step of bonding utilizing an adhesive material; see the search notes therein.

759 Including organic insulating material between metal levels:
This subclass is indented under subclass 758. Subject matter wherein there is at least one layer of organic insulating material between different layers of metal. An organic compound is one which fulfills the requirements of the Class 260 definition, i.e., has a molecule characterized by two carbon atoms bonded together, one atom of carbon being bonded to at least one atom of hydrogen or a halogen, or one atom or carbon bonded to at least one atom of nitrogen by a single or double bond, certain compounds such as HCN, CN-CN, HNCO, HNCS, cyanogen halides, cyanamide, fulminic acid and metal carbides, being exceptions to this rule.

760 Separating insulating layer is laminate or composite of plural insulating materials (e.g., silicon oxide on silicon nitride, silicon oxynitride):
This subclass is indented under subclass 758. Subject matter wherein there is at least one separating insulator layer between different metal layers, which separating insulator layer is itself made up of plural sublayers, or which separating insulator layer is a composite such as a mixture of silicon oxide and silicon nitride.

761 At least one layer containing vanadium, hafnium, niobium, zirconium, or tantalum:
This subclass is indented under subclass 750. Subject matter wherein a layered electrical contact or lead has at least one layer which

contains vanadium (V), hafnium (Hf), niobium (Nb), zirconium (Zr), or tantalum (Ta).

762 At least one layer containing silver or copper:
This subclass is indented under subclass 750. Subject matter wherein a layered electrical contact or lead has at least one layer which contains copper (Cu) or silver (Ag).

763 At least one layer of molybdenum, titanium, or tungsten:
This subclass is indented under subclass 750. Subject matter wherein a layered electrical contact or lead has at least one layer of molybdenum (Mo), titanium (Ti) or tungsten (W).

764 Alloy containing molybdenum, titanium, or tungsten:
This subclass is indented under subclass 763. Subject matter wherein at least one layer containing molybdenum, titanium, or tungsten contains an alloy thereof.

765 At least one layer of an alloy containing aluminum:
This subclass is indented under subclass 750. Subject matter wherein a layered electrical contact or lead has at least one layer of an alloy containing aluminum (Al).

766 At least one layer containing chromium or nickel:
This subclass is indented under subclass 750. Subject matter wherein a layered electrical contact or lead has at least one layer containing chromium (Cr) or nickel (Ni).

767 Resistive to electromigration or diffusion of the contact or lead material:
This subclass is indented under subclass 741. Subject matter wherein an electrical contact or lead material is adapted to resist electromigration of the contact or lead material, or diffusion of the contact or lead material into the material to which the contact is attached.

768 Refractory or platinum group metal or alloy or silicide thereof:
This subclass is indented under subclass 741. Subject matter wherein the specified contact or lead material is a refractory metal or a platinum group metal, i.e., a metal found in groups IVA, VA, VIA or VIIIA (other than iron (Fe), nickel (Ni) or cobalt (Co)) of the periodic table of the elements or a silicide (i.e., a binary compound of silicon), usually with a more electropositive element or radical, thereof.

769 Platinum group metal or silicide thereof:
This subclass is indented under subclass 768. Subject matter wherein the specified contact or lead material is a platinum group metal (i.e., platinum (Pt), palladium (Pd), rhodium (Rh), ruthenium (Ru), osmium (Os) or iridium (Ir)) or a silicide i.e., a binary compound of silicon, usually with a more electropositive element or radical, thereof.

770 Molybdenum, tungsten, or titanium or their silicides:
This subclass is indented under subclass 768. Subject matter wherein the specified contact or lead material is molybdenum (Mo), tungsten (W), titanium (Ti), or their silicides, (i.e., a binary compound of one of them with silicon).

771 Alloy containing aluminum:
This subclass is indented under subclass 741. Subject matter wherein the specific contact or lead material is an alloy containing aluminum (Al).

772 Solder composition:
This subclass is indented under subclass 741. Subject matter wherein the specific contact or lead material is a solder composition (i.e., a metal or metallic alloy that melts at relatively low temperatures).

(1) Note. Solder is normally used to join metals with higher melting points than the solder composition.

773 Of specified configuration:
This subclass is indented under subclass 734. Subject matter in which an electrical contact or lead has a specific configuration or shape.

774 Via (interconnection hole) shape:
This subclass is indented under subclass 773. Subject matter wherein the shape or configuration of an electrical contact or lead is determined by the shape of a hole through an insulating layer through which the contact extends.

775 Varying width or thickness of conductor:
This subclass is indented under subclass 773. Subject matter wherein an electrical contact or lead has a width or thickness which varies over the length of the contact or lead.

776 Cross-over arrangement, component or structure:
This subclass is indented under subclass 773. Subject matter wherein means are provided for electrically insulating electrical contact elements or leads which cross each other to do so without a short circuit therebetween.

(1) Note. Electrically insulating components or structures associated with electrical contact crossovers may be referred to as bridges, tunnels, overpasses, underpasses, etc.

777 Chip mounted on chip:
This subclass is indented under subclass 734. Subject matter wherein a semiconductor substrate of an active solid-state device is electrically connected to, and positioned on, another semiconductor substrate.

SEE OR SEARCH CLASS:
361, Electricity: Electrical Systems and Devices, subclasses 760+ for plural modules or means of connection of components to a printed circuit board.

778 Flip chip:
This subclass is indented under subclass 734. Subject matter wherein a semiconductor substrate which contains an active solid-state electronic device has electric contacts on the top side thereof, the top side being that which contains an active solid-state electronic device, and which is flipped so that the contact side becomes the bottom side for connection with a substrate which has matching electrical contacts.

779 Solder wettable contact, lead, or bond:
This subclass is indented under subclass 734. Subject matter wherein an electrical contact or lead has a surface to which solder will readily adhere.

780 Ball or nail head type contact, lead, or bond:
This subclass is indented under subclass 734. Subject matter wherein a contact, lead, or bond is in the form of a wire having an end for connection to the semiconductor which is in the shape of a ball or nail head.

SEE OR SEARCH THIS CLASS, SUBCLASS:
738, for ball shaped bump contacts.

781 Layered contact, lead or bond:
This subclass is indented under subclass 780. Subject matter wherein a ball or nail head type contact is made up of a plurality of layers of the same or different material.

782 Die bond:
This subclass is indented under subclass 734. Subject matter wherein a semiconductor chip containing at least one active solid-state device and provided with a contact or lead is provided with a means for attaching the chip to a supporting member.

(1) Note. The supporting member or attachment may form part of the contacts or leads for the chip, or be separate therefrom.

783 With adhesive means:
This subclass is indented under subclass 782. Subject matter wherein adhesive means (e.g., a layer) is provided to secure a die (chip) which contains an active solid-state electronic device to a supporting member.

SEE OR SEARCH CLASS:
156, Adhesive Bonding and Miscellaneous Chemical Manufacture, subclasses 60+ for processes of uniting plural bodies via an adhesive material.
438, Semiconductor Device Manufacturing: Process, particularly subclasses 118+ for methods of packaging a semiconductor device including a step of bonding utilizing an adhesive material; see the search notes therein.

784 Wire contact, lead, or bond:
This subclass is indented under subclass 734. Subject matter wherein the contact, lead or bond is a very flexible, elongated, small diame-

ter filament made of electrically conductive material.

785 By pressure alone:
This subclass is indented under subclass 734. Subject matter wherein the electrical contact, lead or bond is held in place by pressure alone (e.g., by a spring clip).

SEE OR SEARCH THIS CLASS, SUBCLASS:
181+, and 688+, for other electrodes in press contact with an active semiconductor device.

786 Configuration or pattern of bonds:
This subclass is indented under subclass 734. Subject matter wherein the electrical contact, lead or bond, has a specific configuration or pattern.

SEE OR SEARCH THIS CLASS, SUBCLASS:
459, for light activated devices with particular bonding pad arrangement.
625, for mesa structure semiconductor device bonded to heat sink or thick electrical conductor.

787 ENCAPSULATED:
This subclass is indented under the class definition. Subject matter wherein an active solid-state electronic device, often part of a semiconductor chip, is surrounded by an electrically insulating material which forms a sealed encasement therefor.

SEE OR SEARCH THIS CLASS, SUBCLASS:
100, for encapsulated light emitter device.
433+, for light responsive devices with housing or encapsulation.
687, for a housing containing an encapsulant material.

SEE OR SEARCH CLASS:
29, Metal Working, particularly subclasses 841 and 855 for methods of assembling an electrical component to a base or lead and encapsulating the same.
65, Glass Manufacturing, appropriate subclasses for the manufacturing of glass encapsulated electronic devices or components thereof.
174, Electricity: Conductors and Insulators, subclass 251 for a printed circuit with an encapsulated wire.
264, Plastic and Nonmetallic Article Shaping or Treating: Processes, subclass 272.11 for encapsulation of electrical components.
343, Communications: Radio Wave Antennas, subclass 873 for embedded, potted, or coated radio wave antennas.
361, Electricity: Electrical Systems and Devices, subclasses 600 and 679 for enclosures, including encapsulated types, for electrical and electronic devices.
438, Semiconductor Device Manufacturing: Process, particularly subclasses 112 and 127 for methods of encapsulating; see the search notes therein.

788 With specified encapsulant:
This subclass is indented under subclass 787. Subject matter wherein the chemical composition of the material that encapsulates the active solid-state electronic device is specified.

789 With specified filler material:
This subclass is indented under subclass 788. Subject matter wherein a particular material has been added to an encapsulant material to give it desirable mechanical, thermal, electrical, or other desirable characteristics, and the material is specified.

790 Plural encapsulating layers:
This subclass is indented under subclass 788. Subject matter wherein the encapsulant is made up of more than one layer.

791 Including polysiloxane (e.g., silicone resin):
This subclass is indented under subclass 788. Subject matter wherein the encapsulant includes polysiloxane (i.e., any of various polymeric compounds which contain alternate silicon and oxygen atoms in either a linear or cyclic arrangement), often with one or two organic groups attached to each silicon atom.

792 Including polyimide:
This subclass is indented under subclass 788. Subject matter wherein the encapsulant includes polyimide i.e., a polymeric compound resulting from replacement of both atoms of hydrogen in an organic amine by organic univalent acid radicals or by an organic divalent acid radical.

(1) Note. Polyimides are copolymers (polymers formed from at least two different starting organic materials) which have a linkage, as illustrated below, between the starting materials, wherein R is typically hydrogen and Q_1 and Q_2 are the organic residues of the starting monomers.

793 Including epoxide:
This subclass is indented under subclass 788. Subject matter wherein the encapsulant includes an epoxy compound (i.e., a compound containing three membered ring consisting or one oxygen and two carbon atoms).

794 Including glass:
This subclass is indented under subclass 788. Subject matter wherein the encapsulant contains glass (i.e., an amorphous inorganic, usually transparent or translucent substance consisting of a mixture of silicates or borates or phosphates formed by fusion of silica or of oxides of boron or phosphorous with a flux and stabilizer that cools to a rigid condition without crystallization).

795 With specified filler material:
This subclass is indented under subclass 787. Subject matter wherein a particular material has been added to an encapsulant material to give it desirable mechanical, thermal, electrical, or other desirable characteristics, and the material is specified.

796 With heat sink embedded in encapsulant:
This subclass is indented under subclass 787. Subject matter wherein a heat sink is embedded in the encapsulant.

SEE OR SEARCH CLASS:
174, Electricity: Conductors and Insulators, appropriate subclasses.
361, Electricity: Electrical Systems and Devices, subclasses 704 through 723 for thermal conduction means.

797 ALIGNMENT MARKS:
This subclass is indented under the class definition. Subject matter wherein the active solid-state device is provided with one or more indicia or marks used during fabrication of the device to facilitate accurate alignment of regions in the device.

798 MISCELLANEOUS:
This subclass is indented under the class definition. Subject matter wherein the subject matter is not otherwise provided for.

E-SUBCLASSES

The E-subclasses in U.S. Classes 257 and 438 provide for active solid-state electronic devices, that is, electronic devices or components that are made primarily of solid materials, usually semiconductors, which operate by the movement of charge carriers - electrons or holes - which undergo energy level changes within the material and can modify an input voltage or electro-magnetic signal to achieve rectification, amplification, oscillating, radiation emission, or switching action, or capacitors or resistors with potential-jump or surface barrier; the E-subclasses include processes or apparatus peculiar to the manufacture or treatment of such active solid-state devices or of parts of such devices.

E21.001 PROCESSES OR APPARATUS ADAPTED FOR MANUFACTURE OR TREATMENT OF SEMICONDUCTOR OR SOLID-STATE DEVICES OR OF PARTS THEREOF (EPO):
This main group provides for processes or apparatus that are employed in the manufacture or treatment of semiconductor or solid-state devices or of parts thereof. This subclass is substantially the same in scope as ECLA classification H01L21/00.

(1) Note. This subclass will take subject matter where the manufactured or treated device/component (or part thereof) will have at least one of the following capabilities:

(a)The conduction or modification of an electrical current,

(b)The storage of electrical energy for subsequent discharge within a microelectronic integrated circuit, or

(c)The conversion of electromagnetic wave energy to electrical energy or electrical energy to electromagnetic energy.

SEE OR SEARCH THIS CLASS, SUBCLASS:

E31.001,E33.001, E39.001, E45.001, E47.001, E49.001, and E51.001, for processes or apparatus adapted for manufacture or treatment of semiconductor or solid state devices or of parts thereof.

E21.002 Manufacture or treatment of semiconductor device (EPO):

This subclass is indented under subclass E21.001. This subclass is substantially the same in scope as ECLA classification H01L21/02.

E21.003 Manufacture of two-terminal component for integrated circuit (EPO):

This subclass is indented under subclass E21.002. This subclass is substantially the same in scope as ECLA classification H01L21/02B.

SEE OR SEARCH THIS CLASS, SUBCLASS:

E21.532,for manufacture or treatment of devices consisting of a plurality of solid-state components formed in or on a common substrate or of parts thereof.

E21.004 Of resistor (EPO):

This subclass is indented under subclass E21.003. This subclass is substantially the same in scope as ECLA classification H01L21/02B2.

E21.005 Active material comprising carbon, e.g., diamond or diamond-like carbon (EPO):

This subclass is indented under subclass E21.004. This subclass is substantially the same in scope as ECLA classification H01L21/02B2D.

E21.006 Active material comprising refractory, transition, or noble metal or metal compound, e.g., alloy, silicide, oxide, nitride (EPO):

This subclass is indented under subclass E21.004. This subclass is substantially the same in scope as ECLA classification H01L21/02B2M.

E21.007 Active material comprising organic conducting material, e.g., conducting polymer (EPO):

This subclass is indented under subclass E21.004. This subclass is substantially the same in scope as ECLA classification H01L21/02B2P.

E21.008 Of capacitor (EPO):

This subclass is indented under subclass E21.003. This subclass is substantially the same in scope as ECLA classification H01L21/02B3.

E21.009 Dielectric having perovskite structure (EPO):

This subclass is indented under subclass E21.008. This subclass is substantially the same in scope as ECLA classification H01L21/02B3B.

E21.01 Dielectric comprising two or more layers, e.g., buffer layers, seed layers, gradient layers (EPO):

This subclass is indented under subclass E21.009. This subclass is substantially the same in scope as ECLA classification H01L21/02B3B2.

E21.011 Formation of electrode (EPO):

This subclass is indented under subclass E21.008. This subclass is substantially the same in scope as ECLA classification H01L21/02B3C.

E21.012 With increased surface area, e.g., by roughening, texturing (EPO):

This subclass is indented under subclass E21.011. This subclass is substantially the same in scope as ECLA classification H01L21/02B3C2.

E21.013 With rough surface, e.g., using hemispherical grains (EPO):
This subclass is indented under subclass E21.012. This subclass is substantially the same in scope as ECLA classification H01L21/02B3C2B.

E21.014 Having cylindrical, crown, or fin-type shape (EPO):
This subclass is indented under subclass E21.012. This subclass is substantially the same in scope as ECLA classification H01L21/02B3C2D.

E21.015 Having horizontal extensions (EPO):
This subclass is indented under subclass E21.012. This subclass is substantially the same in scope as ECLA classification H01L21/02B3C2H.

E21.016 Made by depositing layers, e.g., alternatingly conductive and insulating layers (EPO):
This subclass is indented under subclass E21.015. This subclass is substantially the same in scope as ECLA classification H01L21/02B3C2H2.

E21.017 Made by patterning layers, e.g., etching conductive layers (EPO):
This subclass is indented under subclass E21.015. This subclass is substantially the same in scope as ECLA classification H01L21/02B3C2H6.

E21.018 Having vertical extensions (EPO):
This subclass is indented under subclass E21.012. This subclass is substantially the same in scope as ECLA classification H01L21/02B3C2V.

E21.019 Made by depositing layers, e.g., alternatingly conductive and insulating layers (EPO):
This subclass is indented under subclass E21.018. This subclass is substantially the same in scope as ECLA classification H01L21/02B3C2V2.

E21.02 Made by patterning layers, e.g., etching conductive layers (EPO):
This subclass is indented under subclass E21.018. This subclass is substantially the same in scope as ECLA classification H01L21/02B3C2V6.

E21.021 Having multilayers, e.g., comprising barrier layer and metal layer (EPO):
This subclass is indented under subclass E21.012. This subclass is substantially the same in scope as ECLA classification H01L21/02B3C4.

E21.022 Of inductor (EPO):
This subclass is indented under subclass E21.003. This subclass is substantially the same in scope as ECLA classification H01L21/02B4.

E21.023 Making mask on semicond uctor body for further photolithographic processing (EPO):
This subclass is indented under subclass E21.002. This subclass is substantially the same in scope as ECLA classification H01L21/027.

E21.024 Comprising organic layer (EPO):
This subclass is indented under subclass E21.023. This subclass is substantially the same in scope as ECLA classification H01L21/027B.

E21.025 For lift-off process (EPO):
This subclass is indented under subclass E21.024. This subclass is substantially the same in scope as ECLA classification H01L21/027B2.

E21.026 Characterized by treatment of photoresist layer (EPO):
This subclass is indented under subclass E21.024. This subclass is substantially the same in scope as ECLA classification H01L21/027B6.

E21.027 Photolith ographic process (EPO):
This subclass is indented under subclass E21.026. This subclass is substantially the same in scope as ECLA classification H01L21/027B6B.

E21.028 Using laser (EPO):
This subclass is indented under subclass E21.027. This subclass is substantially the same in scope as ECLA classification H01L21/027B6B2.

E21.029 Using anti-reflective coating (EPO):
This subclass is indented under subclass E21.027. This subclass is substantially the same in scope as ECLA classification H01L21/027B6B4.

E21.03 Electro-lithographic process (EPO):
This subclass is indented under subclass E21.026. This subclass is substantially the same in scope as ECLA classification H01L21/027B6C.

E21.031 X-ray lithographic process (EPO):
This subclass is indented under subclass E21.026. This subclass is substantially the same in scope as ECLA classification H01L21/027B6D.

E21.032 Ion lithographic process (EPO):
This subclass is indented under subclass E21.026. This subclass is substantially the same in scope as ECLA classification H01L21/027B6E.

E21.033 Comprising inorganic layer (EPO):
This subclass is indented under subclass E21.023. This subclass is substantially the same in scope as ECLA classification H01L21/033.

E21.034 For lift-off process (EPO):
This subclass is indented under subclass E21.033. This subclass is substantially the same in scope as ECLA classification H01L21/033B.

E21.035 Characterized by their composition, e.g., multilayer masks, materials (EPO):
This subclass is indented under subclass E21.033. This subclass is substantially the same in scope as ECLA classification H01L21/033D.

E21.036 Characterized by their size, orientation, disposition, behavior, shape, in horizontal or vertical plane (EPO):
This subclass is indented under subclass E21.033. This subclass is substantially the same in scope as ECLA classification H01L21/033F.

E21.037 Characterized by their behavior during process, e.g., soluble mask, re-deposited mask (EPO):
This subclass is indented under subclass E21.036. This subclass is substantially the same in scope as ECLA classification H01L21/033F2.

E21.038 Characterized by process involved to create mask, e.g., lift-off mask, sidewalls, or to modify mask, such as pre-treatment, post-treatment (EPO):
This subclass is indented under subclass E21.036. This subclass is substantially the same in scope as ECLA classification H01L21/033F4.

E21.039 Process specially adapted to improve the resolution of the mask (EPO):
This subclass is indented under subclass E21.036. This subclass is substantially the same in scope as ECLA classification H01L21/033F6.

E21.04 Device having at least one potential-jump barrier or surface barrier, e.g., PN junction, depletion layer, carrier concentration layer (EPO):
This subclass is indented under subclass E21.002. This subclass is substantially the same in scope as ECLA classification H01L21/04.

E21.041 Device having semiconductor body comprising carbon, e.g., diamond, diamond-like carbon (EPO):
This subclass is indented under subclass E21.04. This subclass is substantially the same in scope as ECLA classification H01L21/04D.

(1) Note. This group covers passivation of the semiconductor body.

E21.042 Making n- or p-doped regions (EPO):
This subclass is indented under subclass E21.041. This subclass is substantially the same in scope as ECLA classification H01L21/04D10.

E21.043 Using ion im plantation (EPO):
This subclass is indented under subclass E21.042. This subclass is substantially the

same in scope as ECLA classification H01L21/04D10B.

E21.044 Changing their shape, e.g., forming recess (EPO):
This subclass is indented under subclass E21.041. This subclass is substantially the same in scope as ECLA classification H01L21/04D16.

E21.045 Making electrode (EPO):
This subclass is indented under subclass E21.041. This subclass is substantially the same in scope as ECLA classification H01L21/04D20.

E21.046 Ohmic electrode (EPO):
This subclass is indented under subclass E21.045. This subclass is substantially the same in scope as ECLA classification H01L21/04D20A.

E21.047 Schottky electrode (EPO):
This subclass is indented under subclass E21.045. This subclass is substantially the same in scope as ECLA classification H01L21/04D20C.

E21.048 Conductor-insulator-semiconductor electrode, e.g., MIS contacts (EPO):
This subclass is indented under subclass E21.045. This subclass is substantially the same in scope as ECLA classification H01L21/04D20E.

E21.049 Multistep processes for manufacture of device whose active layer, e.g., base, channel, comprises semiconducting carbon, e.g., diamond, diamond-like carbon (EPO):
This subclass is indented under subclass E21.041. This subclass is substantially the same in scope as ECLA classification H01L21/04D40.

E21.05 Device controllable only by electric current supplied or the electric potential applied to electrode which does not carry current to be rectified, amplified, or switched, e.g., three-terminal devices such as source, drain, and gate terminals; emitter, base, collector terminals (EPO):
This subclass is indented under subclass E21.049. This subclass is substantially the same in scope as ECLA classification H01L21/04D40B.

E21.051 Field-effect transistor (EPO):
This subclass is indented under subclass E21.05. This subclass is substantially the same in scope as ECLA classification H01L21/04D40B2.

E21.052 Device controllable only by variation of electric current supplied or the electric potential applied to electrodes carrying current to be rectified, amplified, oscillated, or switched, e.g., two-terminal device (EPO):
This subclass is indented under subclass E21.049. This subclass is substantially the same in scope as ECLA classification H01L21/04D40C.

E21.053 Diode (EPO):
This subclass is indented under subclass E21.052. This subclass is substantially the same in scope as ECLA classification H01L21/04D40C2.

E21.054 Device having semiconductor body comprising silicon carbide (SiC) (EPO):
This subclass is indented under subclass E21.04. This subclass is substantially the same in scope as ECLA classification H01L21/04H.

E21.055 Passivating silicon carbide surface (EPO):
This subclass is indented under subclass E21.054. This subclass is substantially the same in scope as ECLA classification H01L21/04H2.

E21.056 Making n- or p- doped regions or layers, e.g., using diffusion (EPO):
This subclass is indented under subclass E21.054. This subclass is substantially the same in scope as ECLA classification H01L21/04H4.

E21.057 Using ion implantation (EPO):
This subclass is indented under subclass E21.056. This subclass is substantially the same in scope as ECLA classification H01L21/04H4A.

SEE OR SEARCH THIS CLASS, SUBCLASS:

E21.054, for processes where ion implantation of boron and subsequent annealing does not produce a p-doped region.

E21.058 Using masks (EPO):
This subclass is indented under subclass E21.057. This subclass is substantially the same in scope as ECLA classification H01L21/04H4A10.

E21.059 Angled implantation (EPO):
This subclass is indented under subclass E21.057. This subclass is substantially the same in scope as ECLA classification H01L21/04H4A12.

E21.06 Changing shape of semiconductor body, e.g., forming recesses (EPO):
This subclass is indented under subclass E21.054. This subclass is substantially the same in scope as ECLA classification H01L21/04H6.

E21.061 Making electrode (EPO):
This subclass is indented under subclass E21.054. This subclass is substantially the same in scope as ECLA classification H01L21/04H10.

E21.062 Ohmic electrode (EPO):
This subclass is indented under subclass E21.061. This subclass is substantially the same in scope as ECLA classification H01L21/04H10A.

E21.063 Conductor-insulator-semiconductor electrode, e.g., MIS contact (EPO):
This subclass is indented under subclass E21.061. This subclass is substantially the same in scope as ECLA classification H01L21/04H10B.

E21.064 Schottky electrode (EPO):
This subclass is indented under subclass E21.061. This subclass is substantially the same in scope as ECLA classification H01L21/04H10C.

E21.065 Multistep processes for manufacture of device whose active layer, e.g., base, channel, comprises silicon carbide (EPO):
This subclass is indented under subclass E21.054. This subclass is substantially the same in scope as ECLA classification H01L21/04H20.

E21.066 Device controllable only by electric current supplied or the electric potential applied to electrode which does not carry current to be rectified, amplified, or switched, e.g., three-terminal device (EPO):
This subclass is indented under subclass E21.065. This subclass is substantially the same in scope as ECLA classification H01L21/04H20B.

E21.067 Device controllable only by variation of electric current supplied or electric potential applied to one or more of the electrodes carrying current to be rectified, amplified, oscillated, or switched, e.g., two-terminal device (EPO):
This subclass is indented under subclass E21.065. This subclass is substantially the same in scope as ECLA classification H01L21/04H20C.

E21.068 Device having semiconductor body comprising selenium (Se) or tellurium (Te) (EPO):
This subclass is indented under subclass E21.04. This subclass is substantially the same in scope as ECLA classification H01L21/06.

E21.069 Preparation of substrate or foundation plate for Se or Te semiconductor (EPO):
This subclass is indented under subclass E21.068. This subclass is substantially the same in scope as ECLA classification H01L21/08.

E21.07 Preliminary treatment of Se or Te, its application to substrate, or the subsequent treatment of combination (EPO):
This subclass is indented under subclass E21.068. This subclass is substantially the same in scope as ECLA classification H01L21/10.

E21.071 Application of Se or Te to substrate or foundation plate (EPO):
This subclass is indented under subclass E21.07. This subclass is substantially the same in scope as ECLA classification H01L21/10B.

E21.072 Conversion of Se or Te to conductive state (EPO):
This subclass is indented under subclass E21.07. This subclass is substantially the same in scope as ECLA classification H01L21/103.

E21.073 Treatment of surface of Se or Te layer after having been made conductive (EPO):
This subclass is indented under subclass E21.07. This subclass is substantially the same in scope as ECLA classification H01L21/105.

E21.074 Provision of discrete insulating layer, i.e., specified barrier layer material (EPO):
This subclass is indented under subclass E21.07. This subclass is substantially the same in scope as ECLA classification H01L21/108.

E21.075 Application of electrode to exposed surface of Se or Te after Se or Te has been applied to foundation plate (EPO):
This subclass is indented under subclass E21.068. This subclass is substantially the same in scope as ECLA classification H01L21/12.

E21.076 Treatment of complete device, e.g., by electroforming to form barrier (EPO):
This subclass is indented under subclass E21.068. This subclass is substantially the same in scope as ECLA classification H01L21/14.

E21.077 Heat treating (EPO):
This subclass is indented under subclass E21.076. This subclass is substantially the same in scope as ECLA classification H01L21/145.

E21.078 Device having semiconductor body comprising cuprous oxide (Cu_2O) or cuprous iodide (CuI) (EPO):
This subclass is indented under subclass E21.04. This subclass is substantially the same in scope as ECLA classification H01L21/16.

E21.079 Preparation of substrate, preliminary treatment oxidation of substrate, reduction treatment (EPO):
This subclass is indented under subclass E21.078. This subclass is substantially the same in scope as ECLA classification H01L21/16B.

E21.08 Preliminary treatment of foundation plate (EPO):
This subclass is indented under subclass E21.079. This subclass is substantially the same in scope as ECLA classification H01L21/16B2.

E21.081 Reduction of copper oxide, treatment of oxide layer (EPO):
This subclass is indented under subclass E21.079. This subclass is substantially the same in scope as ECLA classification H01L21/16B4.

E21.082 Oxidation and subsequent heat treatment of substrate (EPO):
This subclass is indented under subclass E21.079. This subclass is substantially the same in scope as ECLA classification H01L21/16B3.

E21.083 Application of specified conductive layer (EPO):
This subclass is indented under subclass E21.079. This subclass is substantially the same in scope as ECLA classification H01L21/16B5.

E21.084 Treatment of complete device, e.g., electroforming, heat treating (EPO):
This subclass is indented under subclass E21.078. This subclass is substantially the same in scope as ECLA classification H01L21/16C.

E21.085 Device having semiconductor body comprising Group IV elements or Group III-V compounds with or without impurities, e.g., doping materials (EPO):
This subclass is indented under subclass E21.04. This subclass is substantially the same in scope as ECLA classification H01L21/18.

(1) Note. This group covers also processes which, by using the appropriate technol-

ogy, are clearly suitable for manufacture or treatment of devices whose bodies comprise Group IV elements or III-V compounds, even if the material used is not explicitly specified.

E21.086 Intermixing or interdiffusion or disordering of Group III-V heterostructures, e.g., IILD (EPO):
This subclass is indented under subclass E21.085. This subclass is substantially the same in scope as ECLA classification H01L21/18A.

E21.087 Joining of semiconductor body for junction formation (EPO):
This subclass is indented under subclass E21.085. This subclass is substantially the same in scope as ECLA classification H01L21/18B.

E21.088 By direct bonding (EPO):
This subclass is indented under subclass E21.087. This subclass is substantially the same in scope as ECLA classification H01L21/18B2.

E21.089 Multistep processes for manufacture of device using quantum interference effect, e.g., electrostatic Aharonov-Bohm effect (EPO):
This subclass is indented under subclass E21.085. This subclass is substantially the same in scope as ECLA classification H01L21/18Q.

E21.09 Deposition of semiconductor material on substrate, e.g., epitaxial growth, solid phase epitaxy (EPO):
This subclass is indented under subclass E21.085. This subclass is substantially the same in scope as ECLA classification H01L21/20.

E21.091 Using physical deposition, e.g., vacuum deposition, sputtering (EPO):
This subclass is indented under subclass E21.09. This subclass is substantially the same in scope as ECLA classification H01L21/203.

E21.092 Epitaxial deposition of Group IV element, e.g., Si, Ge (EPO):
This subclass is indented under subclass E21.091. This subclass is substantially the same in scope as ECLA classification H01L21/203B.

E21.093 Deposition on semiconductor substrate being different from deposited semiconductor material; i.e., formation of heterojunctions (EPO):
This subclass is indented under subclass E21.092. This subclass is substantially the same in scope as ECLA classification H01L21/203B2.

E21.094 Deposition on insulating or meta llic substrate (EPO):
This subclass is indented under subclass E21.092. This subclass is substantially the same in scope as ECLA classification H01L21/203B3.

E21.095 Epitaxial deposition of diamond (EPO):
This subclass is indented under subclass E21.092. This subclass is substantially the same in scope as ECLA classification H01L21/203B4.

E21.096 Deposition of diamond (EPO):
This subclass is indented under subclass E21.091. This subclass is substantially the same in scope as ECLA classification H01L21/203A.

E21.097 Epitaxial deposition of Group III-V compound (EPO):
This subclass is indented under subclass E21.091. This subclass is substantially the same in scope as ECLA classification H01L21/203C.

E21.098 Deposition on semiconductor substrate not being an Group III-V compound (EPO):
This subclass is indented under subclass E21.097. This subclass is substantially the same in scope as ECLA classification H01L21/203C2.

E21.099 Deposition on insulating or metallic substrate (EPO):
This subclass is indented under subclass E21.097. This subclass is substantially the same in scope as ECLA classification H01L21/203C3.

E21.1 Doping during epitaxial deposition (EPO):
This subclass is indented under subclass E21.097. This subclass is substantially the same in scope as ECLA classification H01L21/203C6.

E21.101 Using reduction or decomposition of gaseous compound yielding solid condensate, i.e., chemical deposition (EPO):
This subclass is indented under subclass E21.09. This subclass is substantially the same in scope as ECLA classification H01L21/205.

E21.102 Epitaxial deposition of Group IV elements, e.g., Si, Ge, C (EPO):
This subclass is indented under subclass E21.101. This subclass is substantially the same in scope as ECLA classification H01L21/205B.

E21.103 Deposition on a semiconductor substrate which is different from the semiconductor material being deposited, i.e., formation of heterojunctions (EPO):
This subclass is indented under subclass E21.102. This subclass is substantially the same in scope as ECLA classification H01L21/205B2.

E21.104 Deposition on an insulating or a metallic substrate (EPO):
This subclass is indented under subclass E21.102. This subclass is substantially the same in scope as ECLA classification H01L21/205B3.

E21.105 Epitaxial deposition of diamond (EPO):
This subclass is indented under subclass E21.102. This subclass is substantially the same in scope as ECLA classification H01L21/205B4.

E21.106 Doping during the epitaxial deposition (EPO):
This subclass is indented under subclass E21.102. This subclass is substantially the same in scope as ECLA classification H01L21/205B6.

E21.107 Deposition of diamond (EPO):
This subclass is indented under subclass E21.101. This subclass is substantially the same in scope as ECLA classification H01L21/205A.

E21.108 Epitaxial deposition of Group III-V compound (EPO):
This subclass is indented under subclass E21.101. This subclass is substantially the same in scope as ECLA classification H01L21/205C.

E21.109 Using molecular beam technique (EPO):
This subclass is indented under subclass E21.108. This subclass is substantially the same in scope as ECLA classification H01L21/205C4.

E21.11 Doping the epitaxial deposit (EPO):
This subclass is indented under subclass E21.108. This subclass is substantially the same in scope as ECLA classification H01L21/205C6.

E21.111 Doping with transition metals to form semi-insulating layers (EPO):
This subclass is indented under subclass E21.11. This subclass is substantially the same in scope as ECLA classification H01L21/205C6B.

E21.112 Deposition on a semiconductor substrate not being Group III-V compound (EPO):
This subclass is indented under subclass E21.108. This subclass is substantially the same in scope as ECLA classification H01L21/205C2.

E21.113 Deposition on an insulating or a metallic substrate (EPO):
This subclass is indented under subclass E21.108. This subclass is substantially the same in scope as ECLA classification H01L21/205C3.

E21.114 Using liquid deposition (EPO):
This subclass is indented under subclass E21.09. This subclass is substantially the same in scope as ECLA classification H01L21/208.

E21.115 Epitaxial deposition of Group IV elements, e.g., Si, Ge, C (EPO):
This subclass is indented under subclass E21.114. This subclass is substantially the same in scope as ECLA classification H01L21/208B.

E21.116 Deposition on a semiconductor substrate which is different from the semiconductor material being deposited, i.e., formation of heterojunction (EPO):
This subclass is indented under subclass E21.115. This subclass is substantially the same in scope as ECLA classification H01L21/208B2.

E21.117 Epitaxial deposition of Group III-V compound (EPO):
This subclass is indented under subclass E21.114. This subclass is substantially the same in scope as ECLA classification H01L21/208C.

E21.118 Deposition on a semiconductor substrate not being an Group III-V compound (EPO):
This subclass is indented under subclass E21.117. This subclass is substantially the same in scope as ECLA classification H01L21/208C2.

E21.119 Characterized by the substrate (EPO):
This subclass is indented under subclass E21.09. This subclass is substantially the same in scope as ECLA classification H01L21/20B.

E21.12 Characterized by the post-treatment used to control the interface betw een substrate and epitaxial layer, e.g., ion implantation followed by annealing (EPO):
This subclass is indented under subclass E21.119. This subclass is substantially the same in scope as ECLA classification H01L21/20B20.

E21.121 Substrate is crystalline insulating material, e.g., sapphire (EPO):
This subclass is indented under subclass E21.119. This subclass is substantially the same in scope as ECLA classification H01L21/20B4.

E21.122 Bonding of semiconductor wafer to insulating substrate or to semic onducting substrate using an intermediate insulating layer (EPO):
This subclass is indented under subclass E21.119. This subclass is substantially the same in scope as ECLA classification H01L21/20B2.

SEE OR SEARCH THIS CLASS, SUBCLASS:
E21.088, for bonding of semiconductor wafer to semiconductor wafer for junction formation.

E21.123 Substrate is crystalline semiconductor material, e.g., lattice adaptation, heteroepitaxy (EPO):
This subclass is indented under subclass E21.119. This subclass is substantially the same in scope as ECLA classification H01L21/20B6.

E21.124 Heteroepitaxy (EPO):
This subclass is indented under subclass E21.123. This subclass is substantially the same in scope as ECLA classification H01L21/20B6B.

E21.125 Defect and dislocati on suppression due to lattice mismatch, e.g., lattice adaptation (EPO):
This subclass is indented under subclass E21.124. This subclass is substantially the same in scope as ECLA classification H01L21/20B6B2.

E21.126 Group III-V compound on dissimilar Group III-V compound (EPO):
This subclass is indented under subclass E21.124. This subclass is substantially the same in scope as ECLA classification H01L21/20B6B4.

E21.127 Group III-V compound on Si or Ge (EPO):
This subclass is indented under subclass E21.124. This subclass is substantially the same in scope as ECLA classification H01L21/20B6B6.

E21.128 Carbon on a noncarbon semiconductor substrate (EPO):
This subclass is indented under subclass E21.124. This subclass is substantially the same in scope as ECLA classification H01L21/20B6B10.

E21.129 Group IVA, e.g., Si, C, Ge on Group IVB, e.g., Ti, Zr (EPO):
This subclass is indented under subclass E21.124. This subclass is substantially the

same in scope as ECLA classification H01L21/20B6B8.

E21.13 The substrate is crystalline conducting material, e.g., metallic silicide (EPO):
This subclass is indented under subclass E21.119. This subclass is substantially the same in scope as ECLA classification H01L21/20B8.

E21.131 Selective epilaxial growth, e.g., simultaneous deposition of mono- and non-mono semiconductor material (EPO):
This subclass is indented under subclass E21.09. This subclass is substantially the same in scope as ECLA classification H01L21/20C.

E21.132 Preparation of substrate for selective epitaxy (EPO) :
This subclass is indented under subclass E21.131. This subclass is substantially the same in scope as ECLA classification H01L21/20C2.

E21.133 Epitaxial re-growth of non-monocrystalline semiconductor material, e.g., lateral epitaxy by seeded solidific ation, solid-state crystallization, solid-state graphoepitaxy, explosive crystallization, grain growth in polycrystalline material (EPO):
This subclass is indented under subclass E21.09. This subclass is substantially the same in scope as ECLA classification H01L21/20D.

E21.134 Using a coherent energy beam, e.g., laser or electron beam (EPO):
This subclass is indented under subclass E21.133. This subclass is substantially the same in scope as ECLA classification H01L21/20D2.

E21.135 Diffusion of impurity material, e.g., doping material, electrode material, into or out of a semiconductor body, or between semiconductor regions; interactions between two or more impurities; redistribution of impurities (EPO):
This subclass is indented under subclass E21.085. This subclass is substantially the same in scope as ECLA classification H01L21/22.

E21.136 From the substrate during epitaxy, e.g., autodoping; preventing or using autodoping (EPO):
This subclass is indented under subclass E21.135. This subclass is substantially the same in scope as ECLA classification H01L21/22C.

E21.137 To control carrier lifetime, i.e., deep level dopant (EPO):
This subclass is indented under subclass E21.135. This subclass is substantially the same in scope as ECLA classification H01L21/22D.

E21.138 In Group III-V compound (EPO):
This subclass is indented under subclass E21.137. This subclass is substantially the same in scope as ECLA classification H01L21/22D2.

E21.139 Lithium-drift (EPO):
This subclass is indented under subclass E21.135. This subclass is substantially the same in scope as ECLA classification H01L21/22L.

E21.14 Diffusion source (EPO):
This subclass is indented under subclass E21.135. This subclass is substantially the same in scope as ECLA classification H01L21/22N.

E21.141 Using diffusion into or out of a solid from or into a gaseous phase (EPO):
This subclass is indented under subclass E21.135. This subclass is substantially the same in scope as ECLA classification H01L21/223.

SEE OR SEARCH THIS CLASS, SUBCLASS:
E21.144,for diffusion into or out of a solid from or into a solid phase, e.g., a doped oxide layer.

E21.142 Diffusion into or out of Group III-V compound (EPO):
This subclass is indented under subclass E21.141. This subclass is substantially the same in scope as ECLA classification H01L21/223B.

E21.143 From or into plasma phase (EPO):
This subclass is indented under subclass E21.141. This subclass is substantially the same in scope as ECLA classification H01L21/223E.

E21.144 Using diffusion into or out of a solid from or into a solid phase, e.g., a doped oxide layer (EPO):
This subclass is indented under subclass E21.135. This subclass is substantially the same in scope as ECLA classification H01L21/225.

E21.145 Diffusion into or out of Group IV semiconductor (EPO):
This subclass is indented under subclass E21.144. This subclass is substantially the same in scope as ECLA classification H01L21/225A.

E21.146 Using predeposition of impurities into the semiconductor surface, e.g., from gaseous phase (EPO):
This subclass is indented under subclass E21.145. This subclass is substantially the same in scope as ECLA classification H01L21/225A2.

E21.147 By ion implantation (EPO):
This subclass is indented under subclass E21.146. This subclass is substantially the same in scope as ECLA classification H01L21/225A2D.

E21.148 From or through or into an applied layer, e.g., photoresist, nitride (EPO):
This subclass is indented under subclass E21.145. This subclass is substantially the same in scope as ECLA classification H01L21/225A4.

E21.149 Applied layer is oxide, e.g., P2O5, PSG, H3 BO3, doped oxide (EPO):
This subclass is indented under subclass E21.148. This subclass is substantially the same in scope as ECLA classification H01L21/225A4D.

E21.15 Through the applied layer (EPO):
This subclass is indented under subclass E21.149. This subclass is substantially the same in scope as ECLA classification H01L21/225A4D2.

E21.151 Applied layer being silicon or silicide or SIPOS, e.g., polysilicon, porous silicon (EPO):
This subclass is indented under subclass E21.148. This subclass is substantially the same in scope as ECLA classification H01L21/225A4F.

E21.152 Diffusion into or out of Group III-V compound (EPO):
This subclass is indented under subclass E21.144. This subclass is substantially the same in scope as ECLA classification H01L21/225B.

E21.153 Using diffusion into or out of a solid from or into a liquid phase, e.g., alloy diffusion process (EPO):
This subclass is indented under subclass E21.135. This subclass is substantially the same in scope as ECLA classification H01L21/228.

E21.154 Alloying of impurity material, e.g., doping material, electrode material, with a semiconductor body (EPO):
This subclass is indented under subclass E21.085. This subclass is substantially the same in scope as ECLA classification H01L21/24.

E21.155 Alloying of doping material with Group III-V compound (EPO):
This subclass is indented under subclass E21.154. This subclass is substantially the same in scope as ECLA classification H01L21/24B.

E21.156 Alloying of electrode material (EPO):
This subclass is indented under subclass E21.154. This subclass is substantially the same in scope as ECLA classification H01L21/24C.

E21.157 With Group III-V compound (EPO):
This subclass is indented under subclass E21.156. This subclass is substantially the same in scope as ECLA classification H01L21/24C2.

E21.158 Manufacture of electrode on semiconductor body using process other than by epitaxial growth, diffusion of impurities, alloying of impurity materials, or radiation bombardment (EPO):

This subclass is indented under subclass E21.085. This subclass is substantially the same in scope as ECLA classification H01L21/28.

SEE OR SEARCH THIS CLASS, SUBCLASS:

E21.090 through E21.134, for epitaxial growth.

E21.135 through E21.153, for diffusion of impurities.

E21.154 through E21 -157, for alloying of impurity materials.

E21.328 through E21.349, for radiation bombardment.

E21.249 through E21.257 and E21.305-E21.314, for etching and patterning the electrodes.

E21.159 Deposition of conductive or insulating material for electrode conducting electric current (EPO):

This subclass is indented under subclass E21.158. This subclass is substantially the same in scope as ECLA classification H01L21/283.

E21.16 From a gas or vapor, e.g., condensation (EPO):

This subclass is indented under subclass E21.159. This subclass is substantially the same in scope as ECLA classification H01L21/285.

E21.161 Of conductive layer (EPO):

This subclass is indented under subclass E21.16. This subclass is substantially the same in scope as ECLA classification H01L21/285B.

E21.162 On semiconductor body comprising Group IV element (EPO):

This subclass is indented under subclass E21.161. This subclass is substantially the same in scope as ECLA classification H01L21/285B4.

E21.163 Deposition of Schottky electrode (EPO):

This subclass is indented under subclass E21.162. This subclass is substantially the same in scope as ECLA classification H01L21/285B4C.

E21.164 O layer comprising silicide (EPO):

This subclass is indented under subclass E21.162. This subclass is substantially the same in scope as ECLA classification H01L21/285B4D.

E21.165 Conductive layer comprising silicide (EPO):

This subclass is indented under subclass E21.162. This subclass is substantially the same in scope as ECLA classification H01L21/285B4A.

E21.166 Conductive layer comprising semiconducting material (EPO):

This subclass is indented under subclass E21.162. This subclass is substantially the same in scope as ECLA classification H01L21/285B4B.

E21.167 Making of side-wall contact (EPO):

This subclass is indented under subclass E21.166. This subclass is substantially the same in scope as ECLA classification H01L21/285B4B2.

E21.168 Conductive layer comprising transition metal, e.g., Ti, W, Mo (EPO):

This subclass is indented under subclass E21.162. This subclass is substantially the same in scope as ECLA classification H01L21/285B4L.

E21.169 By physical means, e.g., sputtering, evaporation (EPO):

This subclass is indented under subclass E21.162. This subclass is substantially the same in scope as ECLA classification H01L21/285B4F.

E21.17 By chemical means, e.g., CVD, LPCVD, PECVD, laser CVD (EPO):

This subclass is indented under subclass E21.162. This subclass is substantially the same in scope as ECLA classification H01L21/285B4H.

E21.171 Selective deposition (EPO):
This subclass is indented under subclass E21.17. This subclass is substantially the same in scope as ECLA classification H01L21/285B4H2.

E21.172 On semiconductor body comprising Group III-V compound (EPO):
This subclass is indented under subclass E21.161. This subclass is substantially the same in scope as ECLA classification H01L21/285B6.

E21.173 Deposition of Schottky electrode (EPO):
This subclass is indented under subclass E21.172. This subclass is substantially the same in scope as ECLA classification H01L21/285B6B.

E21.174 From a liquid, e.g., electrolytic deposition (EPO):
This subclass is indented under subclass E21.159. This subclass is substantially the same in scope as ECLA classification H01L21/288.

E21.175 Using an external electrical current, i.e., electro-deposition (EPO):
This subclass is indented under subclass E21.174. This subclass is substantially the same in scope as ECLA classification H01L21/288E.

E21.176 Manufacture or post-treatment of electrode having a capacitive structure, i.e., gate structure for field-effect device (EPO):
This subclass is indented under subclass E21.158. This subclass is substantially the same in scope as ECLA classification H01L21/28B.

E21.177 MOS-gate structure (EPO):
This subclass is indented under subclass E21.176. This subclass is substantially the same in scope as ECLA classification H01L21/28B2.

E21.178 Joint-gate structure (EPO):
This subclass is indented under subclass E21.177. This subclass is substantially the same in scope as ECLA classification H01L21/28B2C.

E21.179 Floating or plural gate structure (EPO):
This subclass is indented under subclass E21.177. This subclass is substantially the same in scope as ECLA classification H01L21/28B2D.

E21.18 Gate structure with charge-trapping insulator (EPO):
This subclass is indented under subclass E21.177. This subclass is substantially the same in scope as ECLA classification H01L21/28B2E.

E21.181 On semiconductor body not comprising Group IV element, e.g., Group III-V compound (EPO):
This subclass is indented under subclass E21.177. This subclass is substantially the same in scope as ECLA classification H01L21/28B2F.

E21.182 On semiconductor body comprising Group IV element excluding non-elemental Si, e.g., Ge, C, diamond, silicon compound or compound, such as SiC or SiGe (EPO):
This subclass is indented under subclass E21.177. This subclass is substantially the same in scope as ECLA classification H01L21/28B2G.

E21.183 For charge-coupled device (EPO):
This subclass is indented under subclass E21.177. This subclass is substantially the same in scope as ECLA classification H01L21/28B2K.

E21.184 PN-homojunction gate structure (EPO):
This subclass is indented under subclass E21.176. This subclass is substantially the same in scope as ECLA classification H01L21/28B3.

E21.185 For charge-coupled device (EPO):
This subclass is indented under subclass E21.184. This subclass is substantially the same in scope as ECLA classification H01L21/28B3K.

E21.186 Schottky gate structure (EPO):
This subclass is indented under subclass E21.176. This subclass is substantially the same in scope as ECLA classification H01L21/28B4.

E21.187 For charge-coupled device (EPO):
This subclass is indented under subclass E21.186. This subclass is substantially the same in scope as ECLA classification H01L21/28B4K.

E21.188 Heterojunction gate structure (EPO):
This subclass is indented under subclass E21.176. This subclass is substantially the same in scope as ECLA classification H01L21/28B5.

E21.189 For charge-coupled device (EPO):
This subclass is indented under subclass E21.188. This subclass is substantially the same in scope as ECLA classification H01L21/28B5K.

E21.19 Making electrode structure comprising conductor-insulator-semiconductor, e.g., MIS gate (EPO):
This subclass is indented under subclass E21.158. This subclass is substantially the same in scope as ECLA classification H01L21/28E.

E21.191 Insulator formed on silicon semiconductor body (EPO):
This subclass is indented under subclass E21.19. This subclass is substantially the same in scope as ECLA classification H01L21/28E2.

E21.192 Characterized by insulator (EPO):
This subclass is indented under subclass E21.191. This subclass is substantially the same in scope as ECLA classification H01L21/28E2C.

E21.193 On single crystalline silicon (EPO):
This subclass is indented under subclass E21.192. This subclass is substantially the same in scope as ECLA classification H01L21/28E2C2.

E21.194 Characterized by treatment after formation of definitive gate conductor (EPO):
This subclass is indented under subclass E21.193. This subclass is substantially the same in scope as ECLA classification H01L21/28E2C2B.

E21.195 Characterized by conductor (EPO):
This subclass is indented under subclass E21.191. This subclass is substantially the same in scope as ECLA classification H01L21/28E2B.

(1) Note. This subclass includes the final conductor comprising a superconductor.

E21.196 Final conductor next to insulator having lateral composition or doping variation, or being formed laterally by more than one deposition step (EPO):
This subclass is indented under subclass E21.195. This subclass is substantially the same in scope as ECLA classification H01L21/28E2B8.

E21.197 Final conductor layer next to insulator being silicon e.g., polysilicon, with or without impurities (EPO):
This subclass is indented under subclass E21.195. This subclass is substantially the same in scope as ECLA classification H01L21/28E2B2.

(1) Note. A very thin layer, e.g., silicon, adhesion or seed layer is not considered as the one next to the insulator.

E21.198 Conductor comprising at least another non-silicon conductive layer (EPO):
This subclass is indented under subclass E21.197. This subclass is substantially the same in scope as ECLA classification H01L21/28E2B2P.

E21.199 Conductor comprising silicide layer formed by silicidation reaction of silicon with metal layer (EPO):
This subclass is indented under subclass E21.198. This subclass is substantially the same in scope as ECLA classification H01L21/28E2B2P3.

SEE OR SEARCH THIS CLASS, SUBCLASS:
E21.198,for conductor comprising a silicide layer formed by metal ion implantation.

E21.2 Conductor comprising metal or metallic silicide formed by deposition e.g., sputter depo-

sition, i.e., without silicidation reaction (EPO):
This subclass is indented under subclass E21.198. This subclass is substantially the same in scope as ECLA classification H01L21/28E2B2P4.

E21.201 Conductor layer next to insulator is Si or Ge or C and their non-Si alloys (EPO):
This subclass is indented under subclass E21.195. This subclass is substantially the same in scope as ECLA classification H01L21/28E2B4.

E21.202 Conductor layer next to the insulator is single metal, e.g., Ta, W, Mo, Al (EPO):
This subclass is indented under subclass E21.195. This subclass is substantially the same in scope as ECLA classification H01L21/28E2B5.

E21.203 Conductor layer next to insulator is metallic silicide (Me Si) (EPO):
This subclass is indented under subclass E21.195. This subclass is substantially the same in scope as ECLA classification H01L21/28E2B7.

E21.204 Conductor layer next to insulator is non-Me Si composite or compound, e.g., TiN (EPO):
This subclass is indented under subclass E21.195. This subclass is substantially the same in scope as ECLA classification H01L21/28E2B6.

E21.205 Characterized by sectional shape, e.g., T-shape, inverted T, spacer (EPO):
This subclass is indented under subclass E21.195. This subclass is substantially the same in scope as ECLA classification H01L21/28E2B20.

E21.206 Lithography, isolation, or planarization-related aspects of making conductor-insulator-semiconductor structure, e.g., sub-lithography lengths; to solve problems arising at crossing with side of device isolation (EPO):
This subclass is indented under subclass E21.195. This subclass is substantially the same in scope as ECLA classification H01L21/28E2B30.

(1) Note. When the conductor, or part of it, is a spacer, documents are also classified in E21.205.

E21.207 Insulator formed on nonelemental silicon semiconductor body, e.g., Ge, SiGe, SiGeC (EPO):
This subclass is indented under subclass E21.19. This subclass is substantially the same in scope as ECLA classification H01L21/28E3.

E21.208 Comprising layer having ferroelectric properties (EPO):
This subclass is indented under subclass E21.158. This subclass is substantially the same in scope as ECLA classification H01L21/28K.

E21.209 Making electrode structure comprising conductor-insulator-conductor-insulator-semiconductor, e.g., gate stack for non-volatile memory (EPO):
This subclass is indented under subclass E21.158. This subclass is substantially the same in scope as ECLA classification H01L21/28F.

E21.21 Comprising charge trapping insulator (EPO):
This subclass is indented under subclass E21.158. This subclass is substantially the same in scope as ECLA classification H01L21/28G.

E21.211 Treatment of semiconductor body using process other than deposition of semiconductor material on a substrate, diffusion or alloying of impurity material, or radiation treatment (EPO):
This subclass is indented under subclass E21.085. This subclass is substantially the same in scope as ECLA classification H01L21/30.

E21.212 Hydrogenation or deuterization, e.g., using atomic hydrogen or deuterium from a plasma (EPO):
This subclass is indented under subclass E21.211. This subclass is substantially the same in scope as ECLA classification H01L21/30H.

E21.213 Of Group III-V compound (EPO):
This subclass is indented under subclass E21.212. This subclass is substantially the same in scope as ECLA classification H01L21/30H8.

E21.214 To change their surface-physical characteristics or shape, e.g., etching, polishing, cutting (EPO):
This subclass is indented under subclass E21.211. This subclass is substantially the same in scope as ECLA classification H01L21/302.

E21.215 Chemical or electrical treatment, e.g., electrolytic etching (EPO):
This subclass is indented under subclass E21.214. This subclass is substantially the same in scope as ECLA classification H01L21/306.

SEE OR SEARCH THIS CLASS, SUBCLASS:
E21.240, for forming insulating layers by masking or using photolithographic technique.

E21.216 Electrolytic etching (EPO):
This subclass is indented under subclass E21.215. This subclass is substantially the same in scope as ECLA classification H01L21/3063.

E21.217 Of Group III-V compound (EPO):
This subclass is indented under subclass E21.216. This subclass is substantially the same in scope as ECLA classification H01L21/3063B.

E21.218 Plasma etching; reactive-ion etching (EPO):
This subclass is indented under subclass E21.215. This subclass is substantially the same in scope as ECLA classification H01L21/3065.

E21.219 Chemical etching (EPO):
This subclass is indented under subclass E21.215. This subclass is substantially the same in scope as ECLA classification H01L21/306B.

E21.22 Etching of Group III-V compound (EPO):
This subclass is indented under subclass E21.219. This subclass is substantially the same in scope as ECLA classification H01L21/306B4.

E21.221 Anisotropic liquid etching (EPO):
This subclass is indented under subclass E21.22. This subclass is substantially the same in scope as ECLA classification H01L21/306B4B.

E21.222 Vapor phase etching (EPO):
This subclass is indented under subclass E21.22. This subclass is substantially the same in scope as ECLA classification H01L21/306B4C.

E21.223 Anisotropic liquid etching (EPO):
This subclass is indented under subclass E21.219. This subclass is substantially the same in scope as ECLA classification H01L21/306B3.

E21.224 Chemical cleaning (EPO):
This subclass is indented under subclass E21.215. This subclass is substantially the same in scope as ECLA classification H01L21/306N.

E21.225 Cleaning diamond or graphite (EPO):
This subclass is indented under subclass E21.224. This subclass is substantially the same in scope as ECLA classification H01L21/306N8.

E21.226 Dry cleaning (EPO):
This subclass is indented under subclass E21.224. This subclass is substantially the same in scope as ECLA classification H01L21/306N2.

E21.227 With gaseous hydrogen fluoride (HF) (EPO):
This subclass is indented under subclass E21.226. This subclass is substantially the same in scope as ECLA classification H01L21/306N2B.

E21.228 Wet cleaning only (EPO):
This subclass is indented under subclass E21.224. This subclass is substantially the

same in scope as ECLA classification H01L21/306N4.

E21.229 Combining dry and wet cleaning steps (EPO):
This subclass is indented under subclass E21.224. This subclass is substantially the same in scope as ECLA classification H01L21/306N6.

E21.23 With simultaneous mechanical treatment, e.g., chemical-mechanical polishing (EPO):
This subclass is indented under subclass E21.215. This subclass is substantially the same in scope as ECLA classification H01L21/306P.

E21.231 Using mask (EPO):
This subclass is indented under subclass E21.215. This subclass is substantially the same in scope as ECLA classification H01L21/308.

E21.232 Characterized by their composition, e.g., multilayer masks, materials (EPO):
This subclass is indented under subclass E21.231. This subclass is substantially the same in scope as ECLA classification H01L21/308B.

E21.233 Characterized by their size, orientation, disposition, behavior, shape, in horizontal or vertical plane (EPO):
This subclass is indented under subclass E21.231. This subclass is substantially the same in scope as ECLA classification H01L21/308D.

E21.234 Characterized by their behavior during process, e.g., soluble mask, redeposited mask (EPO):
This subclass is indented under subclass E21.233. This subclass is substantially the same in scope as ECLA classification H01L21/308D2.

E21.235 Characterized by process involved to create mask, e.g., lift-off mask, sidewall, or to modify the mask, e.g., pre-treatment, post-treatment (EPO):
This subclass is indented under subclass E21.233. This subclass is substantially the same in scope as ECLA classification H01L21/308D4.

E21.236 Process specially adapted to improve resolution of mask (EPO):
This subclass is indented under subclass E21.233. This subclass is substantially the same in scope as ECLA classification H01L21/308D6.

E21.237 Mechanical treatment, e.g., grinding, polishing, cutting (EPO):
This subclass is indented under subclass E21.214. This subclass is substantially the same in scope as ECLA classification H01L21/304.

E21.238 Making grooves, e.g., cutting (EPO):
This subclass is indented under subclass E21.237. This subclass is substantially the same in scope as ECLA classification H01L21/304B.

E21.239 Using abrasion, e.g., sand-blasting (EPO):
This subclass is indented under subclass E21.237. This subclass is substantially the same in scope as ECLA classification H01L21/304D.

E21.24 To form insulating layer thereon, e.g., for masking or by using photolithographic technique (EPO):
This subclass is indented under subclass E21.214. This subclass is substantially the same in scope as ECLA classification H01L21/31.

SEE OR SEARCH THIS CLASS, SUBCLASS:
E21.158,for manufacture of electrodes.
E21.502,for encapsulating layers.

E21.241 Post-treatment (EPO):
This subclass is indented under subclass E21.24. This subclass is substantially the same in scope as ECLA classification H01L21/3105.

E21.242 Of organic layer (EPO):
This subclass is indented under subclass E21.241. This subclass is substantially the same in scope as ECLA classification H01L21/3105P.

E21.243 Planarization of insulating layer (EPO):
This subclass is indented under subclass E21.241. This subclass is substantially the

same in scope as ECLA classification H01L21/3105B.

E21.244 Involving dielectric removal step (EPO):
This subclass is indented under subclass E21.243. This subclass is substantially the same in scope as ECLA classification H01L21/3105B2.

E21.245 Removal by chemical etching, e.g., dry etching (EPO):
This subclass is indented under subclass E21.244. This subclass is substantially the same in scope as ECLA classification H01L21/3105B2B.

SEE OR SEARCH THIS CLASS, SUBCLASS:
E21.249,for etching, per se.

E21.246 Removal by selective chemical etching, e.g., selective dry etching through mask (EPO):
This subclass is indented under subclass E21.245. This subclass is substantially the same in scope as ECLA classification H01L21/3105B2B2.

E21.247 Doping insulating layer (EPO):
This subclass is indented under subclass E21.241. This subclass is substantially the same in scope as ECLA classification H01L21/3115.

E21.248 By ion implantation (EPO):
This subclass is indented under subclass E21.247. This subclass is substantially the same in scope as ECLA classification H01L21/3115B.

E21.249 Etching insulating layer by chemical or physical means (EPO):
This subclass is indented under subclass E21.241. This subclass is substantially the same in scope as ECLA classification H01L21/311.

E21.25 Etching inorganic layer (EPO):
This subclass is indented under subclass E21.249. This subclass is substantially the same in scope as ECLA classification H01L21/311B.

E21.251 By chemical means (EPO):
This subclass is indented under subclass E21.25. This subclass is substantially the same in scope as ECLA classification H01L21/311B2.

E21.252 By dry-etching (EPO):
This subclass is indented under subclass E21.251. This subclass is substantially the same in scope as ECLA classification H01L21/311B2B.

E21.253 Of layers not containing Si, e.g., PZT, Al_2O_3 (EPO):
This subclass is indented under subclass E21.252. This subclass is substantially the same in scope as ECLA classification H01L21/311B2B2.

E21.254 Etching organic layer (EPO):
This subclass is indented under subclass E21.249. This subclass is substantially the same in scope as ECLA classification H01L21/311C.

E21.255 By chemical means (EPO):
This subclass is indented under subclass E21.254. This subclass is substantially the same in scope as ECLA classification H01L21/311C2.

E21.256 By dry-etching (EPO):
This subclass is indented under subclass E21.255. This subclass is substantially the same in scope as ECLA classification H01L21/311C2B.

E21.257 Using mask (EPO):
This subclass is indented under subclass E21.249. This subclass is substantially the same in scope as ECLA classification H01L21/311D.

E21.258 Using masks (EPO):
This subclass is indented under subclass E21.24. This subclass is substantially the same in scope as ECLA classification H01L21/32.

E21.259 Organic layers, e.g., photoresist (EPO):
This subclass is indented under subclass E21.24. This subclass is substantially the same in scope as ECLA classification H01L21/312.

E21.26 Layer comprising organo-silicon compound (EPO):
This subclass is indented under subclass E21.259. This subclass is substantially the same in scope as ECLA classification H01L21/312B.

E21.261 Layer comprising polysiloxane compound (EPO):
This subclass is indented under subclass E21.26. This subclass is substantially the same in scope as ECLA classification H01L21/312B2.

E21.262 Layer comprising hydrogen silsesquioxane (EPO):
This subclass is indented under subclass E21.261. This subclass is substantially the same in scope as ECLA classification H01L21/312B2B.

E21.263 Layer comprising silazane compounds (EPO):
This subclass is indented under subclass E21.261. This subclass is substantially the same in scope as ECLA classification H01L21/312B4.

E21.264 Layers comprising fluoro hydrocarbon compounds, e.g., polytetrafluoroethylene (EPO):
This subclass is indented under subclass E21.259. This subclass is substantially the same in scope as ECLA classification H01L21/312F.

E21.265 By Langmuir-Blodgett technique (EPO):
This subclass is indented under subclass E21.259. This subclass is substantially the same in scope as ECLA classification H01L21/312L.

E21.266 Inorganic layer (EPO):
This subclass is indented under subclass E21.24. This subclass is substantially the same in scope as ECLA classification H01L21/314.

E21.267 Composed of alternated layers or of mixtures of nitrides and oxides or of oxynitrides, e.g., formation of oxynitride by oxidation of nitride layer (EPO):
This subclass is indented under subclass E21.266. This subclass is substantially the same in scope as ECLA classification H01L21/314B.

E21.268 Of silicon (EPO):
This subclass is indented under subclass E21.266. This subclass is substantially the same in scope as ECLA classification H01L21/314B1.

E21.269 Formed by deposition from a gas or vapor (EPO):
This subclass is indented under subclass E21.268. This subclass is substantially the same in scope as ECLA classification H01L21/314B2.

E21.27 Carbon layer, e.g., diamond-like layer (EPO):
This subclass is indented under subclass E21.266. This subclass is substantially the same in scope as ECLA classification H01L21/314C.

E21.271 Composed of oxide or glassy oxide or oxide based glass (EPO):
This subclass is indented under subclass E21.266. This subclass is substantially the same in scope as ECLA classification H01L21/316.

E21.272 With perovskite structure (EPO):
This subclass is indented under subclass E21.271. This subclass is substantially the same in scope as ECLA classification H01L21/316D.

E21.273 Deposition of porous oxide or porous glassy oxide or oxide based porous glass (EPO):
This subclass is indented under subclass E21.271. This subclass is substantially the same in scope as ECLA classification H01L21/316P.

E21.274 Deposition from gas or vapor (EPO):
This subclass is indented under subclass E21.271. This subclass is substantially the same in scope as ECLA classification H01L21/316B.

E21.275 Deposition of boron or phosphorus doped silicon oxide, e.g., BSG, PSG, BPSG (EPO):
This subclass is indented under subclass E21.274. This subclass is substantially the

same in scope as ECLA classification H01L21/316B4.

E21.276 Deposition of halogen doped silicon oxide, e.g., fluorine doped silicon oxide (EPO):
This subclass is indented under subclass E21.274. This subclass is substantially the same in scope as ECLA classification H01L21/316B6.

E21.277 Deposition of carbon doped silicon oxide, e.g., SiOC (EPO):
This subclass is indented under subclass E21.274. This subclass is substantially the same in scope as ECLA classification H01L21/316B8.

E21.278 Deposition of silicon oxide (EPO):
This subclass is indented under subclass E21.274. This subclass is substantially the same in scope as ECLA classification H01L21/316B2.

E21.279 On silicon body (EPO):
This subclass is indented under subclass E21.278. This subclass is substantially the same in scope as ECLA classification H01L21/316B2B.

E21.28 Deposition of aluminum oxide (EPO):
This subclass is indented under subclass E21.274. This subclass is substantially the same in scope as ECLA classification H01L21/316B3.

E21.281 On a silicon body (EPO):
This subclass is indented under subclass E21.28. This subclass is substantially the same in scope as ECLA classification H01L21/316B3B.

E21.282 Formed by oxidation (EPO):
This subclass is indented under subclass E21.271. This subclass is substantially the same in scope as ECLA classification H01L21/316C.

E21.283 Of semiconductor material, e.g., by oxidation of semiconductor body itself (EPO):
This subclass is indented under subclass E21.282. This subclass is substantially the same in scope as ECLA classification H01L21/316C2.

E21.284 By thermal oxidation (EPO):
This subclass is indented under subclass E21.283. This subclass is substantially the same in scope as ECLA classification H01L21/316C2B.

E21.285 Of silicon (EPO):
This subclass is indented under subclass E21.284. This subclass is substantially the same in scope as ECLA classification H01L21/316C2B2.

E21.286 Of Group III-V compound (EPO):
This subclass is indented under subclass E21.284. This subclass is substantially the same in scope as ECLA classification H01L21/316C2B3.

E21.287 By anodic oxidation (EPO):
This subclass is indented under subclass E21.283. This subclass is substantially the same in scope as ECLA classification H01L21/316C2C.

E21.288 Of silicon (EPO):
This subclass is indented under subclass E21.287. This subclass is substantially the same in scope as ECLA classification H01L21/316C2C2.

E21.289 Of Group III-V compound (EPO) :
This subclass is indented under subclass E21.287. This subclass is substantially the same in scope as ECLA classification H01L21/316C2C3.

E21.29 Of metallic layer, e.g., Al deposited on body, e.g., formation of multi-layer insulating structures (EPO):
This subclass is indented under subclass E21.282. This subclass is substantially the same in scope as ECLA classification H01L21/316C3.

E21.291 By anodic oxidation (EPO):
This subclass is indented under subclass E21.29. This subclass is substantially the same in scope as ECLA classification H01L21/316C3B.

E21.292 Inorganic layer composed of nitride (EPO):
This subclass is indented under subclass E21.266. This subclass is substantially the

same in scope as ECLA classification H01L21/318.

E21.293 Of silicon nitride (EPO):
This subclass is indented under subclass E21.292. This subclass is substantially the same in scope as ECLA classification H01L21/318B.

E21.294 Deposition/post-treatment of noninsulating, e.g., conductive - or resistive - layers on insulating layers (EPO):
This subclass is indented under subclass E21.214. This subclass is substantially the same in scope as ECLA classification H01L21/3205.

SEE OR SEARCH THIS CLASS, SUBCLASS:
E21.158,for manufacture of electrodes.

E21.295 Deposition of layer comprising metal, e.g., metal, alloys, metal compounds (EPO):
This subclass is indented under subclass E21.294. This subclass is substantially the same in scope as ECLA classification H01L21/3205M.

E21.296 Of metal-silicide layer (EPO):
This subclass is indented under subclass E21.295. This subclass is substantially the same in scope as ECLA classification H01L21/3205M2.

E21.297 Deposition of semiconductive layer, e.g., poly - or amorphous silicon layer (EPO):
This subclass is indented under subclass E21.294. This subclass is substantially the same in scope as ECLA classification H01L21/3205N.

E21.298 Deposition of superconductive layer (EPO):
This subclass is indented under subclass E21.294. This subclass is substantially the same in scope as ECLA classification H01L21/3205Q.

E21.299 Deposition of conductive or semi-conductive organic layer (EPO):
This subclass is indented under subclass E21.294. This subclass is substantially the same in scope as ECLA classification H01L21/3205P.

E21.3 Post treatment (EPO):
This subclass is indented under subclass E21.294. This subclass is substantially the same in scope as ECLA classification H01L21/321.

E21.301 Oxidation of silicon-containing layer (EPO):
This subclass is indented under subclass E21.3. This subclass is substantially the same in scope as ECLA classification H01L21/321C.

E21.302 Nitriding of silicon-containing layer (EPO):
This subclass is indented under subclass E21.3. This subclass is substantially the same in scope as ECLA classification H01L21/321D.

E21.303 Planarization (EPO):
This subclass is indented under subclass E21.3. This subclass is substantially the same in scope as ECLA classification H01L21/321P.

E21.304 By chemical mechanical polishing (CMP) (EPO):
This subclass is indented under subclass E21.303. This subclass is substantially the same in scope as ECLA classification H01L21/321P2.

E21.305 Physical or chemical etching of layer, e.g., to produce a patterned layer from pre-deposited extensive layer (EPO):
This subclass is indented under subclass E21.3 This subclass is substantially the same in scope as ECLA classification H01L21/3213.

E21.306 By physical means only (EPO):
This subclass is indented under subclass E21.305. This subclass is substantially the same in scope as ECLA classification H01L21/3213B.

E21.307 Of silicon-containing layer (EPO):
This subclass is indented under subclass E21.306. This subclass is substantially the same in scope as ECLA classification H01L21/3213B2.

E21.308 By chemical means only (EPO):
This subclass is indented under subclass E21.305. This subclass is substantially the same in scope as ECLA classification H01L21/3213C.

E21.309 By liquid etching only (EPO):
This subclass is indented under subclass E21.308. This subclass is substantially the same in scope as ECLA classification H01L21/3213C2.

E21.31 By vapor etching only (EPO):
This subclass is indented under subclass E21.308. This subclass is substantially the same in scope as ECLA classification H01L21/3213C4.

E21.311 Using plasma (EPO):
This subclass is indented under subclass E21.31. This subclass is substantially the same in scope as ECLA classification H01L21/3213C4B.

E21.312 Of silicon-containing layer (EPO):
This subclass is indented under subclass E21.311. This subclass is substantially the same in scope as ECLA classification H01L21/3213C4B2.

E21.313 Pre- or post-treatment, e.g., anti-corrosion process (EPO):
This subclass is indented under subclass E21.31. This subclass is substantially the same in scope as ECLA classification H01L21/3213C4D.

E21.314 Using mask (EPO):
This subclass is indented under subclass E21.305. This subclass is substantially the same in scope as ECLA classification H01L21/3213D.

E21.315 Doping layer (EPO):
This subclass is indented under subclass E21.3. This subclass is substantially the same in scope as ECLA classification H01L21/3215.

E21.316 Doping polycrystalline or amorphous silicon layer (EPO):
This subclass is indented under subclass E21.315. This subclass is substantially the same in scope as ECLA classification H01L21/3215B.

E21.317 To modify their internal properties, e.g., to produce internal imperfections (EPO):
This subclass is indented under subclass E21.211. This subclass is substantially the same in scope as ECLA classification H01L21/322.

E21.318 Of silicon body, e.g., for gettering (EPO):
This subclass is indented under subclass E21.317. This subclass is substantially the same in scope as ECLA classification H01L21/322B.

E21.319 Using cavities formed by inert gas ion implantation, e.g., hydrogen, noble gas (EPO):
This subclass is indented under subclass E21.318. This subclass is substantially the same in scope as ECLA classification H01L21/322B2.

E21.32 Of silicon on insulator (SOI) (EPO):
This subclass is indented under subclass E21.318. This subclass is substantially the same in scope as ECLA classification H01L21/322B10.

E21.321 Thermally inducing defects using oxygen present in silicon body for intrinsic gettering (EPO):
This subclass is indented under subclass E21.318. This subclass is substantially the same in scope as ECLA classification H01L21/322B8.

(1) Note. Gettering using both extrinsic and intrinsic gettering processes is classified in both E21.318 and E21.321.

E21.322 Of Group III-V compound, e.g., to make them semi-insulating (EPO):
This subclass is indented under subclass E21.317. This subclass is substantially the same in scope as ECLA classification H01L21/322C.

E21.323 Of diamond body (EPO):
This subclass is indented under subclass E21.317. This subclass is substantially the same in scope as ECLA classification H01L21/322D.

E21.324 Thermal treatment for modifying properties of semiconductor body, e.g., annealing, sintering (EPO):
This subclass is indented under subclass E21.211. This subclass is substantially the

same in scope as ECLA classification H01L21/324.

E21.325 For the formation of PN junction without addition of impurities (EPO):
This subclass is indented under subclass E21.324. This subclass is substantially the same in scope as ECLA classification H01L21/324B.

E21.326 Of Group III-V compound (EPO):
This subclass is indented under subclass E21.324. This subclass is substantially the same in scope as ECLA classification H01L21/324P.

E21.327 Application of electric current or field, e.g., for electroforming (EPO):
This subclass is indented under subclass E21.211. This subclass is substantially the same in scope as ECLA classification H01L21/326.

E21.328 Radiation treatment (EPO):
This subclass is indented under subclass E21.085. This subclass is substantially the same in scope as ECLA classification H01L21/26.

E21.329 Using natural radiation, e.g., alpha , beta or gamma radiation (EPO):
This subclass is indented under subclass E21.328. This subclass is substantially the same in scope as ECLA classification H01L21/26C.

E21.33 To produce chemical element by transmutation (EPO):
This subclass is indented under subclass E21.328. This subclass is substantially the same in scope as ECLA classification H01L21/261.

E21.331 With high-energy radiation (EPO):
This subclass is indented under subclass E21.328. This subclass is substantially the same in scope as ECLA classification H01L21/263.

E21.332 For etching, e.g., sputter etching (EPO):
This subclass is indented under subclass E21331. This subclass is substantially the same in scope as ECLA classification H01L21/263B.

E21.333 For heating, e.g., electron beam heating (EPO):
This subclass is indented under subclass E21.331. This subclass is substantially the same in scope as ECLA classification H01L21/263C.

E21.334 Producing ions for implantation (EPO):
This subclass is indented under subclass E21.331. This subclass is substantially the same in scope as ECLA classification H01L21/265.

E21.335 In Group IV semiconductor (EPO):
This subclass is indented under subclass E21.334. This subclass is substantially the same in scope as ECLA classification H01L21/265A.

E21.336 Of electrically active species (EPO):
This subclass is indented under subclass E21.335. This subclass is substantially the same in scope as ECLA classification H01L21/265A2.

E21.337 Through-implantation (EPO):
This subclass is indented under subclass E21.336. This subclass is substantially the same in scope as ECLA classification H01L21/265A2B.

E21.338 Recoil-implantation (EPO):
This subclass is indented under subclass E21.335. This subclass is substantially the same in scope as ECLA classification H01L21/265A3.

E21.339 Of electrically inactive species in silicon to make buried insulating layer (EPO):
This subclass is indented under subclass E21.335. This subclass is substantially the same in scope as ECLA classification H01L21/265A4.

E21.34 In Group III-V compound (EPO):
This subclass is indented under subclass E21.334. This subclass is substantially the same in scope as ECLA classification H01L21/265B.

E21.341 Of electrically active species (EPO):
This subclass is indented under subclass E21.34. This subclass is substantially the same

in scope as ECLA classification H01L21/265B2.

E21.342 Through-implantation (EPO):
This subclass is indented under subclass E21.341. This subclass is substantially the same in scope as ECLA classification H01L21/265B2B.

E21.343 Characterized by the implantation of both electrically active and inactive species in the same semiconductor region to be doped (EPO):
This subclass is indented under subclass E21.34. This subclass is substantially the same in scope as ECLA classification H01L21/265B3.

E21.344 In diamond (EPO):
This subclass is indented under subclass E21.334. This subclass is substantially the same in scope as ECLA classification H01L21/265D.

E21.345 Characterized by the angle between the ion beam and the crystal planes or the main crystal surface (EPO):
This subclass is indented under subclass E21.334. This subclass is substantially the same in scope as ECLA classification H01L21/265F.

E21.346 Using mask (EPO):
This subclass is indented under subclass E21.334. This subclass is substantially the same in scope as ECLA classification H01L21/266.

E21.347 Using electromagnetic radiation, e.g., laser radiation (EPO):
This subclass is indented under subclass E21.331. This subclass is substantially the same in scope as ECLA classification H01L21/268.

E21.348 Using X-ray laser (EPO):
This subclass is indented under subclass E21.347. This subclass is substantially the same in scope as ECLA classification H01L21/268B.

E21.349 Using incoherent radiation (EPO):
This subclass is indented under subclass E21.347. This subclass is substantially the same in scope as ECLA classification H01L21/268C.

E21.35 Multi-step process for manufacture of device of bipolar type, e.g., diodes, transistors, thyristors, resistors, capacitors) (EPO):
This subclass is indented under subclass E21.085. This subclass is substantially the same in scope as ECLA classification H01L21/328.

E21.351 Device comprising one or two electrodes, e.g., diode, resistor or capacitor with PN or Schottky junctions (EPO):
This subclass is indented under subclass E21.35. This subclass is substantially the same in scope as ECLA classification H01L21/329.

E21.352 Diode (EPO):
This subclass is indented under subclass E21.351. This subclass is substantially the same in scope as ECLA classification H01L21/329B.

E21.353 Tunnel diode (EPO):
This subclass is indented under subclass E21.352. This subclass is substantially the same in scope as ECLA classification H01L21/329B2.

E21.354 Transit time diode, e.g., IMPATT, TRAPATT diode (EPO):
This subclass is indented under subclass E21.352. This subclass is substantially the same in scope as ECLA classification H01L21/329B3.

E21.355 Break-down diode, e.g., Zener diode, avalanche diode (EPO):
This subclass is indented under subclass E21.352. This subclass is substantially the same in scope as ECLA classification H01L21/329B4.

E21.356 Zener diode (EPO):
This subclass is indented under subclass E21.355. This subclass is substantially the same in scope as ECLA classification H01L21/329B4B.

E21.357 Avalanche diode (EPO):
This subclass is indented under subclass E21.355. This subclass is substantially the

same in scope as ECLA classification H01L21/329B4C.

E21.358 Rectifier diode (EPO):
This subclass is indented under subclass E21.352. This subclass is substantially the same in scope as ECLA classification H01L21/329B5.

E21.359 Schottky diode (EPO):
This subclass is indented under subclass E21.352. This subclass is substantially the same in scope as ECLA classification H01L21/329B6.

E21.36 Planar diode (EPO):
This subclass is indented under subclass E21.352. This subclass is substantially the same in scope as ECLA classification H01L21/329B7.

E21.361 Multi-layer diode, e.g., PNPN or NPNP diode (EPO):
This subclass is indented under subclass E21.352. This subclass is substantially the same in scope as ECLA classification H01L21/329B8.

E21.362 Gated-diode structure, e.g., SITh, FCTh, FCD (EPO):
This subclass is indented under subclass E21.352. This subclass is substantially the same in scope as ECLA classification H01L21/329B9.

E21.363 Resistor with PN junction (EPO):
This subclass is indented under subclass E21.351. This subclass is substantially the same in scope as ECLA classification H01L21/329C.

E21.364 Capacitor with PN - or Schottky junction, e.g., varactor (EPO):
This subclass is indented under subclass E21.351. This subclass is substantially the same in scope as ECLA classification H01L21/329D.

SEE OR SEARCH THIS CLASS, SUBCLASS:
E21.397, for hybrid capacitor with PN junction combined with MOS control.

E21.365 Active layer is Group III-V compound (EPO):
This subclass is indented under subclass E21.351. This subclass is substantially the same in scope as ECLA classification H01L21/329P.

E21.366 Diode (EPO):
This subclass is indented under subclass E21.365. This subclass is substantially the same in scope as ECLA classification H01L21/329P4.

E21.367 With an heterojunction, e.g., resonant tunneling diodes (RTD) (EPO):
This subclass is indented under subclass E21.366. This subclass is substantially the same in scope as ECLA classification H01L21/329P4D.

E21.368 Schottky diode (EPO):
This subclass is indented under subclass E21.366. This subclass is substantially the same in scope as ECLA classification H01L21/329P4C.

E21.369 Device comprising three or more electrodes (EPO):
This subclass is indented under subclass E21.35. This subclass is substantially the same in scope as ECLA classification H01L21/33.

E21.37 Transistor (EPO):
This subclass is indented under subclass E21.369. This subclass is substantially the same in scope as ECLA classification H01L21/331.

E21.371 Heterojunction transistor (EPO):
This subclass is indented under subclass E21.37. This subclass is substantially the same in scope as ECLA classification H01L21/331B.

(1) Note: for multi-step processes, a junction between two regions of the same material but in different crystalline state, e.g., amorphous Si or poly Si emitters on a single crystalline Si, is not considered an heterojunction.

E21.372 Bipolar thin film transistor (EPO):
This subclass is indented under subclass E21.37. This subclass is substantially the same in scope as ECLA classification H01L21/331E.

E21.373 Lateral transistor (EPO):
This subclass is indented under subclass E21.37. This subclass is substantially the same in scope as ECLA classification H01L21/331C.

E21.374 Schottky transistor (EPO):
This subclass is indented under subclass E21.037. This subclass is substantially the same in scope as ECLA classification H01L21/331D.

E21.375 Silicon vertical transistor (EPO):
This subclass is indented under subclass E21.037. This subclass is substantially the same in scope as ECLA classification H01L21/331F.

E21.376 Planar transistor (EPO):
This subclass is indented under subclass E21.375. This subclass is substantially the same in scope as ECLA classification H01L21/331F2.

E21.377 Mesa-planar transistor (EPO):
This subclass is indented under subclass E21.375. This subclass is substantially the same in scope as ECLA classification H01L21/331F3.

E21.378 Inverse transistor (EPO):
This subclass is indented under subclass E21.375. This subclass is substantially the same in scope as ECLA classification H01L21/331F4.

E21.379 With single crystalline emitter, collector or base including extrinsic, link or graft base formed on silicon substrate, e.g., by epitaxy, recrystallization, after insulating device isolation (EPO):
This subclass is indented under subclass E21.375. This subclass is substantially the same in scope as ECLA classification H01L21/331F8.

E21.38 Where main current goes through whole of silicon substrate, e.g., power bipolar transistor (EPO):
This subclass is indented under subclass E21.375. This subclass is substantially the same in scope as ECLA classification H01L21/331F10.

E21.381 With a multi- emitter, e.g., interdigitated, multicellular, distributed (EPO):
This subclass is indented under subclass E21.38. This subclass is substantially the same in scope as ECLA classification H01L21/331F10E.

E21.382 Field-effect controlled bipolar-type transistor, e.g., insulated gate bipolar transistor (IGBT) (EPO):
This subclass is indented under subclass E21.37. This subclass is substantially the same in scope as ECLA classification H01L21/331G.

E21.383 Vertical insulated gate bipolar transistor (EPO):
This subclass is indented under subclass E21.382. This subclass is substantially the same in scope as ECLA classification H01L21/331G2.

E21.384 With recessed gate (EPO):
This subclass is indented under subclass E21.383. This subclass is substantially the same in scope as ECLA classification H01L21/331G2R.

E21.385 With recess formed by etching in source/emitter contact region (EPO):
This subclass is indented under subclass E21.383. This subclass is substantially the same in scope as ECLA classification H01L21/331G2B.

E21.386 Active layer, e.g., base, is Group III-V compound (EPO):
This subclass is indented under subclass E21.37. This subclass is substantially the same in scope as ECLA classification H01L21/331P.

E21.387 Heterojunction transistor (EPO):
This subclass is indented under subclass E21.386. This subclass is substantially the same in scope as ECLA classification H01L21/331P2.

E21.388 Thyristor (EPO):
This subclass is indented under subclass E21.369. This subclass is substantially the same in scope as ECLA classification H01L21/332.

SEE OR SEARCH THIS CLASS, SUBCLASS:
E21.362, for gated diode structure, e.g., FCTh, SITh, and FCD.

E21.389 Lateral or planar thyristor (EPO):
This subclass is indented under subclass E21.388. This subclass is substantially the same in scope as ECLA classification H01L21/332B.

E21.39 Structurally associated with other devices (EPO):
This subclass is indented under subclass E21.388. This subclass is substantially the same in scope as ECLA classification H01L21/332M.

SEE OR SEARCH THIS CLASS, SUBCLASS:
E21.602, for manufacturing of integrated circuits.

E21.391 Other device being a controlling device of the field-effect-type (EPO):
This subclass is indented under subclass E21.39. This subclass is substantially the same in scope as ECLA classification H01L21/332M2.

E21.392 Bi-directional thyristor (EPO):
This subclass is indented under subclass E21.388. This subclass is substantially the same in scope as ECLA classification H01L21/332P.

E21.393 Active layer is Group III-V compound (EPO):
This subclass is indented under subclass E21.388. This subclass is substantially the same in scope as ECLA classification H01L21/332Q.

E21.394 Multi-step process for the manufacture of unipolar device (EPO):
This subclass is indented under subclass E21.085. This subclass is substantially the same in scope as ECLA classification H01L21/334.

E21.395 Transistor-like structure, e.g., hot electron transistor (HET); metal base transistor (MBT); resonant tunneling HET (RHET); resonant tunneling transistor (RTT); bulk barrier transistor (BBT); planar doped barrier transistor (PDBT); charge injection transistor (CHINT); ballistic transistor (EPO):
This subclass is indented under subclass E21.394. This subclass is substantially the same in scope as ECLA classification H01L21/334B.

E21.396 Metal-insulator-semiconductor capacitor, e.g., trench capacitor (EPO):
This subclass is indented under subclass E21.394. This subclass is substantially the same in scope as ECLA classification H01L21/334C.

E21.397 Comprising PN junction, e.g., hybrid capacitor (EPO):
This subclass is indented under subclass E21.396. This subclass is substantially the same in scope as ECLA classification H01L21/334C2.

E21.398 Active layer is Group III-V compound (EPO):
This subclass is indented under subclass E21.394. This subclass is substantially the same in scope as ECLA classification H01L21/334P.

E21.399 Transistor-like structure, e.g., hot electron transistor (HET), metal base transistor (MBT), resonant tunneling hot electron transistor (RHET), resonant tunneling transistor (RTT), bulk barrier transistor (BBT), planar doped barrier transistor (PDBT), charge injection transistor (CHINT) (EPO):
This subclass is indented under subclass E21.398. This subclass is substantially the same in scope as ECLA classification H01L21/334P2.

E21.4 Field-effect transistor (EPO):
This subclass is indented under subclass E21.394. This subclass is substantially the same in scope as ECLA classification H01L21/335.

E21.401 Using static field induced region, e.g., SIT, PBT (EPO):
This subclass is indented under subclass E21.4. This subclass is substantially the same in scope as ECLA classification H01L21/335B.

E21.402 Permeable base transistor (PBT) (EPO):
This subclass is indented under subclass E21.401. This subclass is substantially the same in scope as ECLA classification H01L21/335B2.

E21.403 With heterojunction interface channel or gate, e.g., HFET, HIGFET, SISFET, HJFET, HEMT (EPO):
This subclass is indented under subclass E21.4. This subclass is substantially the same in scope as ECLA classification H01L21/335C.

E21.404 With one or zero or quasi-one or quasi-zero dimensional charge carrier gas channel, e.g., quantum wire FET; single electron transistor (SET); striped channel transistor; coulomb blockade device (EPO):
This subclass is indented under subclass E21.4. This subclass is substantially the same in scope as ECLA classification H01L21/335D.

E21.405 Active layer is Group III-V compound, e.g., III-V velocity modulation transistor (VMT), NERFET (EPO):
This subclass is indented under subclass E21.4. This subclass is substantially the same in scope as ECLA classification H01L21/335P.

E21.406 Using static field induced region, e.g., SIT, PBT (EPO):
This subclass is indented under subclass E21.405. This subclass is substantially the same in scope as ECLA classification H01L21/335P2.

E21.407 With an heterojunction interface channel or gate, e.g., HFET, HIGFET, SI SFET, HJFET, HEMT (EPO):
This subclass is indented under subclass E21.405. This subclass is substantially the same in scope as ECLA classification H01L21/335P3.

E21.408 With one or zero or quasi-one or quasi-zero dimensional channel, e.g., in plane gate transistor (IPG), single electron transistor (SET), striped channel transistor, coulomb blockade device (EPO):
This subclass is indented under subclass E21.405. This subclass is substantially the same in scope as ECLA classification H01L21/335P4.

E21.409 With an insulated gate (EPO):
This subclass is indented under subclass E21.4. This subclass is substantially the same in scope as ECLA classification H01L21/336.

E21.41 Vertical transistor (EPO):
This subclass is indented under subclass E21.409. This subclass is substantially the same in scope as ECLA classification H01L21/336A.

SEE OR SEARCH THIS CLASS, SUBCLASS:
E21.411 through E21.416, for vertical thin film transistor, with the exception of monocrystalline vertical thin film transistor.

E21.411 Thin film unipolar transistor (EPO):
This subclass is indented under subclass E21.409. This subclass is substantially the same in scope as ECLA classification H01L21/336D.

E21.412 Amorphous silicon or polysilicon transistor (EPO):
This subclass is indented under subclass E21.411. This subclass is substantially the same in scope as ECLA classification H01L21/336D2.

(1) Note: This subclass includes amorphous silicon or polysilicon transistor with Gate All Around.

E21.413 Lateral single gate single channel transistor with noninverted structure, i.e., channel layer is formed before gate (EPO):
This subclass is indented under subclass E21.412. This subclass is substantially the same in scope as ECLA classification H01L21/336D2B.

E21.414 Lateral single gate single channel transistor with inverted structure, i.e., channel layer is formed after gate (EPO):
This subclass is indented under subclass E21.412. This subclass is substantially the same in scope as ECLA classification H01L21/336D2C.

E21.415 Monocrystalline silicon transistor on insulating substrate, e.g., quartz substrate (EPO):
This subclass is indented under subclass E21.411. This subclass is substantially the same in scope as ECLA classification H01L21/336D3.

E21.416 On sapphire substrate, e.g., silicon on sapphire (SOS) transistor (EPO):
This subclass is indented under subclass E21.415. This subclass is substantially the same in scope as ECLA classification H01L21/336D3B.

E21.417 With channel containing layer, e.g., p-base, formed in or on drain region, e.g., DMOS transistor (EPO):
This subclass is indented under subclass E21.409. This subclass is substantially the same in scope as ECLA classification H01L21/336B.

E21.418 Vertical power DMOS transistor (EPO):
This subclass is indented under subclass E21.417. This subclass is substantially the same in scope as ECLA classification H01L21/336B2.

E21.419 With recessed gate (EPO):
This subclass is indented under subclass E21.418. This subclass is substantially the same in scope as ECLA classification H01L21/336B2R.

E21.42 With recess formed by etching in source/base contact region (EPO):
This subclass is indented under subclass E21.418. This subclass is substantially the same in scope as ECLA classification H01L21/336B2B.

E21.421 With multiple gate, one gate having MOS structure and others having same or a different structure, i.e., non MOS, e.g., JFET gate (EPO):
This subclass is indented under subclass E21.409. This subclass is substantially the same in scope as ECLA classification H01L21/336E.

E21.422 With floating gate (EPO):
This subclass is indented under subclass E21.409. This subclass is substantially the same in scope as ECLA classification H01L21/336F.

E21.423 With charge trapping gate insulator, e.g., MNOS transistor (EPO):
This subclass is indented under subclass E21.409. This subclass is substantially the same in scope as ECLA classification H01L21/336G.

E21.424 Lateral single gate silicon transistor (EPO):
This subclass is indented under subclass E21.409. This subclass is substantially the same in scope as ECLA classification H01L21/336H.

SEE OR SEARCH THIS CLASS, SUBCLASS:
E21.435, for lateral single gate silicon transistor with LDD.

E21.425 With source or drain region formed by Schottky barrier or conductor-insulator-semiconductor structure (EPO):
This subclass is indented under subclass E21.424. This subclass is substantially the same in scope as ECLA classification H01L21/336H18.

E21.426 With single crystalline channel formed on the silicon substrate after insulating device isolation (EPO):
This subclass is indented under subclass E21.424. This subclass is substantially the same in scope as ECLA classification H01L21/336H20.

E21.427 With asymmetry in channel direction, e.g., high-voltage lateral transistor with channel containing layer, e.g., p-base (EPO):
This subclass is indented under subclass E21.424. This subclass is substantially the same in scope as ECLA classification H01L21/336H4.

SEE OR SEARCH THIS CLASS, SUBCLASS:
E21.417, for lateral single gate silicon transistor with p-base formed in or on the drain region.

E21.428 With a recessed gate, e.g., lateral U-MOS (EPO):
This subclass is indented under subclass E21.424. This subclass is substantially the same in scope as ECLA classification H01L21/336H6.

E21.429 Using etching to form recess at gate location (EPO):
This subclass is indented under subclass E21.428. This subclass is substantially the same in scope as ECLA classification H01L21/336H6B.

E21.43 Recessing gate by adding semiconductor material at source (S) or drain (D) location, e.g., transist or with elevated single crystal S and D (EPO):
This subclass is indented under subclass E21.428. This subclass is substantially the same in scope as ECLA classification H01L21/336H6C.

E21.431 With source and drain recessed by etching or recessed and refilled (EPO):
This subclass is indented under subclass E21.424. This subclass is substantially the same in scope as ECLA classification H01L21/336H8.

E21.432 With source and drain contacts formation strictly before final gate formation, e.g., contact first technology (EPO):
This subclass is indented under subclass E21.424. This subclass is substantially the same in scope as ECLA classification H01L21/336H2.

E21.433 Where the source and drain or source and drain extensions are self-aligned to sides of gate (EPO):
This subclass is indented under subclass E21.424. This subclass is substantially the same in scope as ECLA classification H01L21/336H1.

E21.434 With initial gate mask or masking layer complementary to prospective gate location, e.g., with dummy source and drain contacts (EPO):
This subclass is indented under subclass E21.433. This subclass is substantially the same in scope as ECLA classification H01L21/336H1C.

E21.435 Lateral single gate single channel silicon transistor with both lightly doped source and drain extensions and source and drain self-aligned to sides of gate, e.g., LDD MOSFET, DDD MOSFET (EPO):
This subclass is indented under subclass E21.409. This subclass is substantially the same in scope as ECLA classification H01L21/336C.

E21.436 Gate comprising layer with ferroelectric properties (EPO):
This subclass is indented under subclass E21.409. This subclass is substantially the same in scope as ECLA classification H01L21/336K.

E21.437 With lightly doped drain selectively formed at side of gate (EPO):
This subclass is indented under subclass E21.409. This subclass is substantially the same in scope as ECLA classification H01L21/336L.

SEE OR SEARCH THIS CLASS, SUBCLASS:
E21.435,and E21.427, for LDD, per se.

E21.438 Using self-aligned silicidation, i.e., salicide (EPO):
This subclass is indented under subclass E21.409. This subclass is substantially the same in scope as ECLA classification H01L21/336M.

(1) Note: documents are classified in this subclass when they are directed to avoiding short circuit between source/drain and gate.

SEE OR SEARCH THIS CLASS, SUBCLASS:
E21.165, for improving the source or drain contact.

E21.199, for improving the gate.

E21.439 Providing different silicide thicknesses on gate and on source or drain (EPO):
This subclass is indented under subclass E21.438. This subclass is substantially the same in scope as ECLA classification H01L21/336M2.

E21.44 Using self-aligned selective metal deposition simultaneously on gate and on source or drain (EPO):
This subclass is indented under subclass E21.409. This subclass is substantially the same in scope as ECLA classification H01L21/336N.

E21.441 Active layer is Group III-V compound (EPO):
This subclass is indented under subclass E21.409. This subclass is substantially the same in scope as ECLA classification H01L21/336P.

E21.442 With gate at side of channel (EPO):
This subclass is indented under subclass E21.409. This subclass is substantially the same in scope as ECLA classification H01L21/336S.

E21.443 Using self-aligned punchthrough stopper or threshold implant under gate region (EPO):
This subclass is indented under subclass E21.409. This subclass is substantially the same in scope as ECLA classification H01L21/336T.

E21.444 Using dummy gate wherein at least part of final gate is self-aligned to dummy gate (EPO):
This subclass is indented under subclass E21.409. This subclass is substantially the same in scope as ECLA classification H01L21/336U.

(1) Note: this subclass also includes processes where only a part of the gate is a dummy layer, e.g., part of a silicide stemming from the silicidation of polymer.

E21.445 With PN junction or heterojunction gate (EPO):
This subclass is indented under subclass E21.4. This subclass is substantially the same in scope as ECLA classification H01L21/337.

E21.446 With PN homojunction gate (EPO):
This subclass is indented under subclass E21.445. This subclass is substantially the same in scope as ECLA classification H01L21/337B.

E21.447 Vertical transistor, e.g., tecnetrons (EPO):
This subclass is indented under subclass E21.446. This subclass is substantially the same in scope as ECLA classification H01L21/337B2.

E21.448 With heterojunction gate (EPO):
This subclass is indented under subclass E21.445. This subclass is substantially the same in scope as ECLA classification H01L21/337C.

E21.449 Active layer is Group III-V compound (EPO):
This subclass is indented under subclass E21.445. This subclass is substantially the same in scope as ECLA classification H01L21/337P.

E21.45 With Schottky gate, e.g., MESFET (EPO):
This subclass is indented under subclass E21.4. This subclass is substantially the same in scope as ECLA classification H01L21/338.

E21.451 Active layer being Group III-V compound (EPO):
This subclass is indented under subclass E21.45. This subclass is substantially the same in scope as ECLA classification H01L21/338P.

E21.452 Lateral single-gate transistors (EPO):
This subclass is indented under subclass E21.451. This subclass is substantially the same in scope as ECLA classification H01L21/338P2.

E21.453 Process wherein final gate is made after formation of source and drain regions in

active layer, e.g., dummy-gate process (EPO):
This subclass is indented under subclass E21.452. This subclass is substantially the same in scope as ECLA classification H01L21/338P2B.

E21.454 Process wherein final gate is made before formation, e.g., activation anneal, of source and drain regions in active layer (EPO):
This subclass is indented under subclass E21.452. This subclass is substantially the same in scope as ECLA classification H01L21/338P2C.

(1) Note: This subclass covers processes wherein the drain is formed before the final gate but wherein a LDD or the like is formed after.

E21.455 Lateral transistor with two or more independent gates (EPO):
This subclass is indented under subclass E21.452. This subclass is substantially the same in scope as ECLA classification H01L21/338P2M.

E21.456 Charge transfer device (EPO):
This subclass is indented under subclass E21.394. This subclass is substantially the same in scope as ECLA classification H01L21/339.

E21.457 With insulated gate (EPO):
This subclass is indented under subclass E21.456. This subclass is substantially the same in scope as ECLA classification H01L21/339B.

E21.458 With Schottky gate (EPO):
This subclass is indented under subclass E21.456. This subclass is substantially the same in scope as ECLA classification H01L21/339C.

E21.459 Device having semiconductor body other than carbon, Si, Ge, SiC, Se, Te, Cu_2O, CuI, and Group III-V compounds with or without impurities, e.g., doping materials (EPO):
This subclass is indented under subclass E21.04 This subclass is substantially the same in scope as ECLA classification H01L21/34.

E21.46 Multistep process (EPO):
This subclass is indented under subclass E21.459. This subclass is substantially the same in scope as ECLA classification H01L21/34B.

E21.461 Deposition of semiconductor material on substrate, e.g., epitaxial growth (EPO):
This subclass is indented under subclass E21.459. This subclass is substantially the same in scope as ECLA classification H01L21/36.

E21.462 Using physical deposition, e.g., vacuum deposition, sputtering (EPO):
This subclass is indented under subclass E21.461. This subclass is substantially the same in scope as ECLA classification H01L21/363.

E21.463 Using reduction or decomposition of gaseous compound yielding solid condensate, i.e., chemical deposition (EPO):
This subclass is indented under subclass E21.461. This subclass is substantially the same in scope as ECLA classification H01L21/365.

E21.464 Using liquid deposition (EPO):
This subclass is indented under subclass E21.461. This subclass is substantially the same in scope as ECLA classification H01L21/368.

E21.465 From molten solution of compound or alloy, e.g., liquid phase epitaxy (EPO):
This subclass is indented under subclass E21.464. This subclass is substantially the same in scope as ECLA classification H01L21/368B.

E21.466 Diffusion of impurity material, e.g., dopant, electrode material, into or out of semiconductor body, or between semiconductor regions (EPO):
This subclass is indented under subclass E21.459. This subclass is substantially the same in scope as ECLA classification H01L21/38.

E21.467 Using diffusion into or out of solid from or into gaseous phase (EPO):
This subclass is indented under subclass E21.466. This subclass is substantially the same in scope as ECLA classification H01L21/383.

E21.468 Using diffusion into or out of solid from or into solid phase, e.g., doped oxide layer (EPO):
This subclass is indented under subclass E21.466. This subclass is substantially the same in scope as ECLA classification H01L21/385.

E21.469 Using diffusion into or out of solid from or into liquid phase, e.g., alloy diffusion process (EPO):
This subclass is indented under subclass E21.466. This subclass is substantially the same in scope as ECLA classification H01L21/388.

E21.47 Alloying of impurity material, e.g., dopant, electrode material, with semiconductor body (EPO):
This subclass is indented under subclass E21.459. This subclass is substantially the same in scope as ECLA classification H01L21/40.

E21.471 Radiation treatment (EPO):
This subclass is indented under subclass E21.459. This subclass is substantially the same in scope as ECLA classification H01L21/42.

E21.472 With high-energy radiation (EPO):
This subclass is indented under subclass E21.471. This subclass is substantially the same in scope as ECLA classification H01L21/423.

E21.473 Producing ion implantation (EPO):
This subclass is indented under subclass E21.472. This subclass is substantially the same in scope as ECLA classification H01L21/425.

E21.474 Using mask (EPO):
This subclass is indented under subclass E21.473. This subclass is substantially the same in scope as ECLA classification H01L21/426.

E21.475 Using electromagnetic radiation, e.g., laser radiation (EPO):
This subclass is indented under subclass E21.472. This subclass is substantially the same in scope as ECLA classification H01L21/428.

E21.476 Manufacture of electrodes on semiconductor bodies using processes or apparatus other than epitaxial growth, e.g., coating, diffusion, or alloying, or radiation treatment (EPO):
This subclass is indented under subclass E21.459. This subclass is substantially the same in scope as ECLA classification H01L21/44.

SEE OR SEARCH THIS CLASS, SUBCLASS:
E21.461 through E21.475, for manufacture of electrodes on semiconductor bodies or apparatus not provided for in this subclass.

E21.477 Deposition of conductive or insulating materials for electrode (EPO):
This subclass is indented under subclass E21.476. This subclass is substantially the same in scope as ECLA classification H01L21/441.

E21.478 From gas or vapor, e.g., condensation (EPO):
This subclass is indented under subclass E21.477. This subclass is substantially the same in scope as ECLA classification H01L21/443.

E21.479 From liquid, e.g., electrolytic deposition (EPO):
This subclass is indented under subclass E21.477. This subclass is substantially the same in scope as ECLA classification H01L21/445.

E21.48 Involving application of pressure, e.g., thermocompression bonding (EPO):
This subclass is indented under subclass E21.476. This subclass is substantially the same in scope as ECLA classification H01L21/447.

E21.481 Including application of mechanical vibration, e.g., ultrasonic vibration (EPO):
This subclass is indented under subclass E21.476. This subclass is substantially the same in scope as ECLA classification H01L21/449.

E21.482 Treatment of semiconductor body using process other than electromagnetic radiation (EPO):
This subclass is indented under subclass E21.459. This subclass is substantially the same in scope as ECLA classification H01L21/46.

SEE OR SEARCH THIS CLASS, SUBCLASS:
E21.475, for treatment of semiconductor body using electromagnetic radiation, e.g., laser.
E21.476, for manufacture of electrodes.

E21.483 To change their surface-physical characteristics or shape, e.g., etching, polishing, cutting (EPO):
This subclass is indented under subclass E21.482. This subclass is substantially the same in scope as ECLA classification H01L21/461.

E21.484 Mechanical treatment, e.g., grinding, ultrasonic treatment (EPO):
This subclass is indented under subclass E21.483. This subclass is substantially the same in scope as ECLA classification H01L21/463.

E21.485 Chemical or electrical treatment, e.g., electrolytic etching (EPO):
This subclass is indented under subclass E21.483. This subclass is substantially the same in scope as ECLA classification H01L21/465.

SEE OR SEARCH THIS CLASS, SUBCLASS:
E21.487, for chemical or electrical treatment to form insulating layer.

E21.486 Using mask (EPO):
This subclass is indented under subclass E21.485. This subclass is substantially the same in scope as ECLA classification H01L21/467.

E21.487 To form insulating layer thereon, e.g., for masking or by using photolithographic techniques; posttreatment of these layers (EPO):
This subclass is indented under subclass E21.483. This subclass is substantially the same in scope as ECLA classification H01L21/469.

SEE OR SEARCH THIS CLASS, SUBCLASS:
E21.476, for manufacture of electrodes.
E21.502, for encapsulating layer.

E21.488 Using mask (EPO):
This subclass is indented under subclass E21.487. This subclass is substantially the same in scope as ECLA classification H01L21/475.

E21.489 Posttreatment of insulating layer (EPO):
This subclass is indented under subclass E21.487. This subclass is substantially the same in scope as ECLA classification H01L21/4757.

E21.49 Etching layer (EPO):
This subclass is indented under subclass E21.489. This subclass is substantially the same in scope as ECLA classification H01L21/4757B.

E21.491 Doping layer (EPO):
This subclass is indented under subclass E21.489. This subclass is substantially the same in scope as ECLA classification H01L21/4757C.

E21.492 Organic layer, e.g., photoresist (EPO):
This subclass is indented under subclass E21.487. This subclass is substantially the same in scope as ECLA classification H01L21/47.

E21.493 Inorganic layer (EPO):
This subclass is indented under subclass E21.487. This subclass is substantially the same in scope as ECLA classification H01L21/471.

E21.494 Composed of oxide or glassy oxide or oxide-based glass (EPO):
This subclass is indented under subclass E21.493. This subclass is substantially the same in scope as ECLA classification H01L21/473.

E21.495 Deposition of noninsulating, e.g., conductive-, resistive-, layer on insulating layer (EPO):
This subclass is indented under subclass E21.483. This subclass is substantially the same in scope as ECLA classification H01L21/4763.

SEE OR SEARCH THIS CLASS, SUBCLASS:
E21.476, for manufacture of electrodes.

E21.496 Posttreatment of layer (EPO):
This subclass is indented under subclass E21.495. This subclass is substantially the same in scope as ECLA classification H01L21/4763B.

E21.497 Thermal treatment for modifying property of semiconductor body, e.g., annealing, sintering (EPO):
This subclass is indented under subclass E21.482. This subclass is substantially the same in scope as ECLA classification H01L21/477.

E21.498 Application of electric current or fields, e.g., for electroforming (EPO):
This subclass is indented under subclass E21.482. This subclass is substantially the same in scope as ECLA classification H01L21/479.

E21.499 Assembling semiconductor devices, e.g., packaging, including mounting, encapsulating, or treatment of packaged semiconductor (EPO):
This subclass is indented under subclass E21.04. This subclass is substantially the same in scope as ECLA classification H01L21/50.

E21.5 Mounting semiconductor bodies in container (EPO):
This subclass is indented under subclass E21.499. This subclass is substantially the same in scope as ECLA classification H01L21/52.

E21.501 Providing fillings in container, e.g., gas fillings (EPO):
This subclass is indented under subclass E21.499. This subclass is substantially the same in scope as ECLA classification H01L21/54.

E21.502 Encapsulation, e.g., encapsulation layer, coating (EPO):
This subclass is indented under subclass E21.499. This subclass is substantially the same in scope as ECLA classification H01L21/56.

E21.503 Encapsulation of active face of flip-chip device, e.g., under filling or under encapsulation of flip-chip, encapsulation perform on chip or mounting substrate (EPO):
This subclass is indented under subclass E21.502. This subclass is substantially the same in scope as ECLA classification H01L21/56F.

E21.504 Moulds (EPO):
This subclass is indented under subclass E21.502. This subclass is substantially the same in scope as ECLA classification H01L21/56M.

E21.505 Insulative mounting semiconductor device on support (EPO):
This subclass is indented under subclass E21.499. This subclass is substantially the same in scope as ECLA classification H01L21/58.

E21.506 Attaching or detaching leads or other conductive members, to be used for carrying current to or from device in operation (EPO):
This subclass is indented under subclass E21.499. This subclass is substantially the same in scope as ECLA classification H01L21/60.

E21.507 Formation of contacts to semiconductor by use of metal layers separated by insulating layers, e.g., self-aligned contacts to source/drain or emitter/base (EPO):
This subclass is indented under subclass E21.506. This subclass is substantially the

same in scope as ECLA classification H01L21/60B.

E21.508 Forming solder bumps (EPO):
This subclass is indented under subclass E21.507. This subclass is substantially the same in scope as ECLA classification H01L21/60B2.

E21.509 Involving soldering or alloying process, e.g., soldering wires (EPO):
This subclass is indented under subclass E21.506. This subclass is substantially the same in scope as ECLA classification H01L21/60C.

E21.51 Mounting on metallic conductive member (EPO):
This subclass is indented under subclass E21.509. This subclass is substantially the same in scope as ECLA classification H01L21/60C2.

E21.511 Mounting on insulating member provided with metallic leads, e.g., flip-chip mounting, conductive die mounting (EPO):
This subclass is indented under subclass E21.509. This subclass is substantially the same in scope as ECLA classification H01L21/60C4.

E21.512 Right-up bonding (EPO):
This subclass is indented under subclass E21.511. This subclass is substantially the same in scope as ECLA classification H01L21/60C4B.

E21.513 Mounting on semiconductor conductive member (EPO):
This subclass is indented under subclass E21.509. This subclass is substantially the same in scope as ECLA classification H01L21/60C6.

E21.514 Involving use of conductive adhesive (EPO):
This subclass is indented under subclass E21.506. This subclass is substantially the same in scope as ECLA classification H01L21/60D.

E21.515 Involving use of mechanical auxiliary part without use of alloying or soldering process, e.g., pressure contacts (EPO):
This subclass is indented under subclass E21.506. This subclass is substantially the same in scope as ECLA classification H01L21/60E.

E21.516 Involving automation techniques using film carriers (EPO):
This subclass is indented under subclass E21.506. This subclass is substantially the same in scope as ECLA classification H01L21/60F.

E21.517 Involving use of electron or laser beam (EPO):
This subclass is indented under subclass E21.506. This subclass is substantially the same in scope as ECLA classification H01L21/60G.

E21.518 Involving application of mechanical vibration, e.g., ultrasonic vibration (EPO):
This subclass is indented under subclass E21.506. This subclass is substantially the same in scope as ECLA classification H01L21/607.

E21.519 Involving application of pressure, e.g., thermo-compression bonding (EPO):
This subclass is indented under subclass E21.506. This subclass is substantially the same in scope as ECLA classification H01L21/603.

E21.52 Devices having no potential-jump barrier or surface barrier (EPO):
This subclass is indented under subclass E21.002. This subclass is substantially the same in scope as ECLA classification H01L21/62.

E21.521 Testing or measuring during manufacture or treatment or reliability measurement, i.e., testing of parts followed by no processing which modifies parts as such (EPO):
This subclass is indented under subclass E21.001. This subclass is substantially the same in scope as ECLA classification H01L21/66.

SEE OR SEARCH THIS CLASS, SUBCLASS:
E23.179, for marks, test patterns.

E21.522 Structural arrangement (EPO):
This subclass is indented under subclass E21.521. This subclass is substantially the same in scope as ECLA classification H01L21/66A.

E21.523 Additional lead-in metallization on device, e.g., additional pads or lands, lines in scribe line, sacrificed conductors, sacrificed frames (EPO):
This subclass is indented under subclass E21.522. This subclass is substantially the same in scope as ECLA classification H01L21/66A2.

E21.524 Circuit for characterizing or monitoring manufacturing process, e.g., whole test die, wafer filled with test structures, onboard devices incorporated on each die, process/product control monitors or PCM, devices in scribe-line/kerf, drop-in devices (EPO):
This subclass is indented under subclass E21.522. This subclass is substantially the same in scope as ECLA classification H01L21/66A4.

E21.525 Procedures, i.e., sequence of activities consisting of plurality of measurement and correction, marking or sorting steps (EPO):
This subclass is indented under subclass E21.521. This subclass is substantially the same in scope as ECLA classification H01L21/66P.

E21.526 Connection or disconnection of subentities or redundant parts of device in response to measurement, e.g., wafer scale, memory devices (EPO):
This subclass is indented under subclass E21.525. This subclass is substantially the same in scope as ECLA classification H01L21/66P2.

E21.527 Optical enhancement of defects or not directly visible states, e.g., selective electrolytic deposition, bubbles in liquids, light emission, color change (EPO):
This subclass is indented under subclass E21.525. This subclass is substantially the same in scope as ECLA classification H01L21/66P4.

E21.528 Acting in response to ongoing measurement without interruption of processing, e.g., end-point detection, in-situ thickness measurement (EPO):
This subclass is indented under subclass E21.525. This subclass is substantially the same in scope as ECLA classification H01L21/66P6.

E21.529 Measuring as part of manufacturing process (EPO):
This subclass is indented under subclass E21.521. This subclass is substantially the same in scope as ECLA classification H01L21/66M.

E21.53 For structural parameters, e.g., thickness, line width, refractive index, temperature, warp, bond strength, defects, optical inspection, electrical measurement of structural dimensions, metallurgic measurement of diffusions (EPO):
This subclass is indented under subclass E21.529. This subclass is substantially the same in scope as ECLA classification H01L21/66M2.

E21.531 For electrical parameters, e.g., resistance, deep levels, CV, diffusions by electrical means (EPO):
This subclass is indented under subclass E21.529. This subclass is substantially the same in scope as ECLA classification H01L21/66M4.

E21.532 Manufacture or treatment of devices consisting of plurality of solid-state components formed in or on common substrate or of parts thereof; manufacture of integrated circuit devices or of parts thereof (EPO):
This subclass is indented under subclass E21.001. This subclass is substantially the same in scope as ECLA classification H01L21/70.

E21.533 Of thick- or thin-film circuits or parts thereof (EPO):
This subclass is indented under subclass E21.532. This subclass is substantially the same in scope as ECLA classification H01L21/70B.

E21.534 Of thick-film circuits or parts thereof (EPO):
This subclass is indented under subclass E21.533. This subclass is substantially the same in scope as ECLA classification H01L21/70B2.

E21.535 Of thin-film circuits or parts thereof (EPO):
This subclass is indented under subclass E21.533. This subclass is substantially the same in scope as ECLA classification H01L21/70B3.

E21.536 Manufacture of specific parts of devices (EPO):
This subclass is indented under subclass E21.532. This subclass is substantially the same in scope as ECLA classification H01L21/71.

E21.537 Making of localized buried regions, e.g., buried collector layer, internal connection, substrate contacts (EPO):
This subclass is indented under subclass E21.536. This subclass is substantially the same in scope as ECLA classification H01L21/74.

E21.538 Making of internal connections, substrate contacts (EPO):
This subclass is indented under subclass E21.537. This subclass is substantially the same in scope as ECLA classification H01L21/74B.

E21.539 For Group III-V compound semiconductor integrated circuits (EPO):
This subclass is indented under subclass E21.537. This subclass is substantially the same in scope as ECLA classification H01L21/74F.

E21.54 Making of isolation regions between components (EPO):
This subclass is indented under subclass E21.536. This subclass is substantially the same in scope as ECLA classification H01L21/76.

E21.541 Between components manufactured in active substrate comprising SiC compound semiconductor (EPO):
This subclass is indented under subclass E21.54. This subclass is substantially the same in scope as ECLA classification H01L21/76H.

E21.542 Between components manufactured in active substrate comprising Group III-V compound semiconductor (EPO):
This subclass is indented under subclass E21.54. This subclass is substantially the same in scope as ECLA classification H01L21/76P.

E21.543 Between components manufactured in active substrate comprising Group II-VI compound semiconductor (EPO):
This subclass is indented under subclass E21.54. This subclass is substantially the same in scope as ECLA classification H01L21/76R.

E21.544 PN junction isolation (EPO):
This subclass is indented under subclass E21.54. This subclass is substantially the same in scope as ECLA classification H01L21/761.

E21.545 Dielectric regions, e.g., EPIC dielectric isolation, LOCOS; trench refilling techniques, SOI technology, use of channel stoppers (EPO):
This subclass is indented under subclass E21.54. This subclass is substantially the same in scope as ECLA classification H01L21/762.

E21.546 Using trench refilling with dielectric materials (EPO):
This subclass is indented under subclass E21.545. This subclass is substantially the same in scope as ECLA classification H01L21/762C.

SEE OR SEARCH THIS CLASS, SUBCLASS:
E21.572, for trench filling with polycrystalline silicon.

E21.547 Dielectric material being obtained by full chemical transformation of nondielectric materials, such as polycrystalline silicon, metals (EPO):
This subclass is indented under subclass E21.546. This subclass is substantially the

same in scope as ECLA classification H01L21/762C2.

E21.548 Concurrent filling of plurality of trenches having different trench shape or dimension, e.g., rectangular and V-shaped trenches, wide and narrow trenches, shallow and deep trenches (EPO):
This subclass is indented under subclass E21.546. This subclass is substantially the same in scope as ECLA classification H01L21/762C4.

E21.549 Of trenches having shape other than rectangular or V shape, e.g., rounded corners, oblique or rounded trench walls (EPO):
This subclass is indented under subclass E21.546. This subclass is substantially the same in scope as ECLA classification H01L21/762C6.

E21.55 Trench shape altered by local oxidation of silicon process step, e.g., trench corner rounding by LOCOS (EPO):
This subclass is indented under subclass E21.549. This subclass is substantially the same in scope as ECLA classification H01L21/762C6A.

E21.551 Introducing impurities in trench side or bottom walls, e.g., for forming channel stoppers or alter isolation behavior (EPO):
This subclass is indented under subclass E21.546. This subclass is substantially the same in scope as ECLA classification H01L21/762C8.

E21.552 Using local oxidation of silicon, e.g., LOCOS, SWAMI, SILO (EPO):
This subclass is indented under subclass E21.545. This subclass is substantially the same in scope as ECLA classification H01L21/762B.

E21.553 In region recessed from surface, e.g., in recess, groove, tub or trench region (EPO):
This subclass is indented under subclass E21.552. This subclass is substantially the same in scope as ECLA classification H01L21/762B2.

E21.554 Using auxiliary pillars in recessed region, e.g., to form LOCOS over extended areas (EPO):
This subclass is indented under subclass E21.553. This subclass is substantially the same in scope as ECLA classification H01L21/762B2B.

E21.555 Recessed region having shape other than rectangular, e.g., rounded or oblique shape (EPO):
This subclass is indented under subclass E21.553. This subclass is substantially the same in scope as ECLA classification H01L21/762B2C.

E21.556 Introducing electrical inactive or active impurities in local oxidation region, e.g., to alter LOCOS oxide growth characteristics or for additional isolation purpose (EPO):
This subclass is indented under subclass E21.552. This subclass is substantially the same in scope as ECLA classification H01L21/762B4.

E21.557 Introducing electrical active impurities in local oxidation region solely for forming channel stoppers (EPO):
This subclass is indented under subclass E21.556. This subclass is substantially the same in scope as ECLA classification H01L21/762B4B.

E21.558 Introducing both types of electrical active impurities in local oxidation region solely for forming channel stoppers, e.g., for isolation of complementary doped regions (EPO):
This subclass is indented under subclass E21.557. This subclass is substantially the same in scope as ECLA classification H01L21/762B4B2.

E21.559 With plurality of successive local oxidation steps (EPO):
This subclass is indented under subclass E21.552. This subclass is substantially the same in scope as ECLA classification H01L21/762B6.

E21.56 Dielectric isolation using EPIC technique, i.e., epitaxial passivated integrated circuit (EPO):
This subclass is indented under subclass E21.545. This subclass is substantially the same in scope as ECLA classification H01L21/762F.

E21.561 Using semiconductor or insulator technology, i.e., SOI technology (EPO):
This subclass is indented under subclass E21.545. This subclass is substantially the same in scope as ECLA classification H01L21/762D.

E21.562 Using selective deposition of single crystal silicon, e.g., Selective Epitaxial Growth (SEG) (EPO):
This subclass is indented under subclass E21.561. This subclass is substantially the same in scope as ECLA classification H01L21/762D10.

SEE OR SEARCH THIS CLASS, SUBCLASS:
E21.703, for manufacture of integrated circuits on insulating substrates.
E21.704, for silicon on sapphire technology (SOS).

E21.563 Using silicon implanted buried insulating layers, e.g., oxide layers, i.e., SIMOX technique (EPO):
This subclass is indented under subclass E21.561. This subclass is substantially the same in scope as ECLA classification H01L21/762D2.

E21.564 SOI together with lateral isolation, e.g., using local oxidation of silicon, or dielectric or polycrystalline material refilled trench or air gap isolation regions, e.g., completely isolated semiconductor islands (EPO):
This subclass is indented under subclass E21.561. This subclass is substantially the same in scope as ECLA classification H01L21/762D20.

E21.565 Using full isolation by porous oxide silicon, i.e., FIPOS technique (EPO):
This subclass is indented under subclass E21.561. This subclass is substantially the same in scope as ECLA classification H01L21/762D4.

E21.566 Using lateral overgrowth technique, i.e., ELO techniques (EPO):
This subclass is indented under subclass E21.561. This subclass is substantially the same in scope as ECLA classification H01L21/762D6.

E21.567 Using bonding technique (EPO):
This subclass is indented under subclass E21.561. This subclass is substantially the same in scope as ECLA classification H01L21/762D8.

E21.568 With separation/delamination along ion implanted layer, e.g., "Smart-cut", "Unibond" (EPO):
This subclass is indented under subclass E21.567. This subclass is substantially the same in scope as ECLA classification H01L21/762D8B.

E21.569 Using silicon etch back technique, e.g., BESOI, ELTRAN (EPO):
This subclass is indented under subclass E21.567. This subclass is substantially the same in scope as ECLA classification H01L21/762D8D.

E21.57 With separation/delamination along porous layer (EPO):
This subclass is indented under subclass E21.567. This subclass is substantially the same in scope as ECLA classification H01L21/762D8F.

E21.571 Using selective deposition of single crystal silicon, i.e., SEG technique (EPO):
This subclass is indented under subclass E21.545. This subclass is substantially the same in scope as ECLA classification H01L21/762E.

E21.572 Polycrystalline semiconductor regions (EPO):
This subclass is indented under subclass E21.54. This subclass is substantially the same in scope as ECLA classification H01L21/763.

E21.573 Air gaps (EPO):
This subclass is indented under subclass E21.54. This subclass is substantially the same in scope as ECLA classification H01L21/764.

E21.574 Isolation by field effect (EPO):
This subclass is indented under subclass E21.54. This subclass is substantially the same in scope as ECLA classification H01L21/765.

E21.575 Interconnections, comprising conductors and dielectrics, for carrying current between separate components within device (EPO):
This subclass is indented under subclass E21.536. This subclass is substantially the same in scope as ECLA classification H01L21/768.

E21.576 Characterized by formation and posttreatment of dielectrics, e.g., planarizing (EPO):
This subclass is indented under subclass E21.575. This subclass is substantially the same in scope as ECLA classification H01L21/768B.

E21.577 By forming via holes (EPO):
This subclass is indented under subclass E21.576. This subclass is substantially the same in scope as ECLA classification H01L21/768B2.

E21.578 Tapered via holes (EPO):
This subclass is indented under subclass E21.577. This subclass is substantially the same in scope as ECLA classification H01L21/768B2B.

E21.579 For "dual damascene" type structures (EPO):
This subclass is indented under subclass E21.577. This subclass is substantially the same in scope as ECLA classification H01L21/768B2D.

E21.58 Planarizing dielectric (EPO):
This subclass is indented under subclass E21.576. This subclass is substantially the same in scope as ECLA classification H01L21/768B4.

E21.581 Dielectric comprising air gaps (EPO):
This subclass is indented under subclass E21.576. This subclass is substantially the same in scope as ECLA classification H01L21/768B6.

SEE OR SEARCH THIS CLASS, SUBCLASS:
E21.243, for planarization of insulating materials, per se.

E21.582 Characterized by formation and posttreatment of conductors, e.g., patterning (EPO):
This subclass is indented under subclass E21.575. This subclass is substantially the same in scope as ECLA classification H01L21/768C.

E21.583 Planarization; smoothing (EPO):
This subclass is indented under subclass E21.582. This subclass is substantially the same in scope as ECLA classification H01L21/768C2.

SEE OR SEARCH THIS CLASS, SUBCLASS:
E21.195, for electrode structure characterized by conductor.

E21.584 Barrier, adhesion or liner layer (EPO):
This subclass is indented under subclass E21.582. This subclass is substantially the same in scope as ECLA classification H01L21/768C3.

E21.585 Filling of holes, grooves, vias or trenches with conductive material (EPO):
This subclass is indented under subclass E21.582. This subclass is substantially the same in scope as ECLA classification H01L21/768C4.

E21.586 By selective deposition of conductive material in vias, e.g., selective chemical vapor deposition on semiconductor material, plating (EPO):
This subclass is indented under subclass E21.585. This subclass is substantially the same in scope as ECLA classification H01L21/768C4B.

E21.587 By deposition over sacrificial masking layer, e.g., lift-off (EPO):
This subclass is indented under subclass E21.585. This subclass is substantially the same in scope as ECLA classification H01L21/768C4C.

SEE OR SEARCH THIS CLASS, SUBCLASS:
E21.174, for electrolytic deposition.

E21.588 Reflowing or applying pressure to fill contact hole, e.g., to remove voids (EPO):
This subclass is indented under subclass E21.585. This subclass is substantially the same in scope as ECLA classification H01L21/768C4E.

E21.589 By forming conductive members before deposition of protective insulating material, e.g., pillars, studs (EPO):
This subclass is indented under subclass E21.582. This subclass is substantially the same in scope as ECLA classification H01L21/768C6.

E21.59 Local interconnects; local pads (EPO):
This subclass is indented under subclass E21.582. This subclass is substantially the same in scope as ECLA classification H01L21/768C10.

E21.591 Modifying pattern or conductivity of conductive members, e.g., formation of alloys, reduction of contact resistances (EPO):
This subclass is indented under subclass E21.582. This subclass is substantially the same in scope as ECLA classification H01L21/768C8.

E21.592 By altering solid-state characteristics of conductive members, e.g., fuses, in situ oxidation, laser melting (EPO):
This subclass is indented under subclass E21.591. This subclass is substantially the same in scope as ECLA classification H01L21/768C8B.

(1) Note: This subclass includes permanent or temporary modification.

E21.593 By forming silicide of refractory metal (EPO):
This subclass is indented under subclass E21.591. This subclass is substantially the same in scope as ECLA classification H01L21/768C8C.

E21.594 By using super-conducting material (EPO):
This subclass is indented under subclass E21.591. This subclass is substantially the same in scope as ECLA classification H01L21/768C8D.

E21.595 Modifying pattern (EPO):
This subclass is indented under subclass E21.591. This subclass is substantially the same in scope as ECLA classification H01L21/768C8L.

E21.596 Using laser, e.g., laser cutting, laser direct writing, laser repair (EPO):
This subclass is indented under subclass E21.595. This subclass is substantially the same in scope as ECLA classification H01L21/768C8L2.

E21.597 Formed through semiconductor substrate (EPO):
This subclass is indented under subclass E21.575. This subclass is substantially the same in scope as ECLA classification H01L21/768T.

E21.598 Manufacture or treatment of devices consisting of plurality of solid-state components or integrated circuits formed in, or on, common substrate (EPO):
This subclass is indented under subclass E21.532. This subclass is substantially the same in scope as ECLA classification H01L21/77.

E21.599 With subsequent division of substrate into plural individual devices (EPO):
This subclass is indented under subclass E21.598. This subclass is substantially the same in scope as ECLA classification H01L21/78.

E21.6 Involving separation of active layers from substrate (EPO):
This subclass is indented under subclass E21.599. This subclass is substantially the

same in scope as ECLA classification H01L21/78B.

E21.601 Leaving reusable substrate, e.g., epitaxial lift-off process (EPO):
This subclass is indented under subclass E21.6. This subclass is substantially the same in scope as ECLA classification H01L21/78B2.

E21.602 To produce devices each consisting of plurality of components, e.g., integrated circuits (EPO):
This subclass is indented under subclass E21.599. This subclass is substantially the same in scope as ECLA classification H01L21/82.

E21.603 Substrate is semiconductor, using combination of semiconductor substrates, e.g., diamond, SiC, Si, Group III-V compound, and/or Group II-VI compound semiconductor substrates (EPO):
This subclass is indented under subclass E21.602. This subclass is substantially the same in scope as ECLA classification H01L21/8258.

E21.604 Substrate is semiconductor, using diamond technology (EPO):
This subclass is indented under subclass E21.602. This subclass is substantially the same in scope as ECLA classification H01L21/82D.

SEE OR SEARCH THIS CLASS, SUBCLASS:
E21.604, for diamond.
E21.605, for silicon carbide.
E21.606, for silicon.
E21.697, for Group III-V compound semiconductors.
E21.698, for Group II-VI compound semiconductors.

E21.605 Substrate is semiconductor, using SiC technology (EPO):
This subclass is indented under subclass E21.602. This subclass is substantially the same in scope as ECLA classification H01L21/82H.

E21.606 Substrate being semiconductor, using silicon technology (EPO):
This subclass is indented under subclass E21.602. This subclass is substantially the same in scope as ECLA classification H01L21/822.

E21.607 Three-dimensional integrated circuits stacked in different levels (EPO):
This subclass is indented under subclass E21.606. This subclass is substantially the same in scope as ECLA classification H01L21/822B.

E21.608 Bipolar technology (EPO):
This subclass is indented under subclass E21.606. This subclass is substantially the same in scope as ECLA classification H01L21/8222.

E21.609 Comprising combination of vertical and lateral transistors (EPO):
This subclass is indented under subclass E21.608. This subclass is substantially the same in scope as ECLA classification H01L21/8224.

E21.61 Comprising merged transistor logic or integrated injection logic (EPO):
This subclass is indented under subclass E21.608. This subclass is substantially the same in scope as ECLA classification H01L21/8226.

E21.611 Complementary devices, e.g., complementary transistors (EPO):
This subclass is indented under subclass E21.608. This subclass is substantially the same in scope as ECLA classification H01L21/8228.

E21.612 Complementary vertical transistors (EPO):
This subclass is indented under subclass E21.611. This subclass is substantially the same in scope as ECLA classification H01L21/8228B.

E21.613 Memory structures (EPO):
This subclass is indented under subclass E21.608. This subclass is substantially the same in scope as ECLA classification H01L21/8229.

E21.614 Three-dimensional integrated circuits stacked in different levels (EPO):
This subclass is indented under subclass E21.606. This subclass is substantially the same in scope as ECLA classification H01L21/822B.

E21.615 Field-effect technology (EPO):
This subclass is indented under subclass E21.606. This subclass is substantially the same in scope as ECLA classification H01L21/8232.

E21.616 MIS technology (EPO):
This subclass is indented under subclass E21.615. This subclass is substantially the same in scope as ECLA classification H01L21/8234.

E21.617 Combination of charge coupled devices, i.e., CCD or BBD (EPO):
This subclass is indented under subclass E21.616. This subclass is substantially the same in scope as ECLA classification H01L21/8234B.

E21.618 With particular manufacturing method of channel, e.g., channel implants, halo or pocket implants, or channel materials (EPO):
This subclass is indented under subclass E21.616. This subclass is substantially the same in scope as ECLA classification H01L21/8234C.

E21.619 With particular manufacturing method of source or drain, e.g., specific S or D implants or silicided S or D structures or raised S or D structures (EPO):
This subclass is indented under subclass E21.616. This subclass is substantially the same in scope as ECLA classification H01L21/8234D.

E21.62 Manufacturing common source or drain regions between plurality of conductor-insulator-semiconductor structures (EPO):
This subclass is indented under subclass E21.619. This subclass is substantially the same in scope as ECLA classification H01L21/8234D2.

E21.621 With particular manufacturing method of gate conductor, e.g., particular materials, shapes (EPO):
This subclass is indented under subclass E21.616. This subclass is substantially the same in scope as ECLA classification H01L21/8234G.

E21.622 Silicided or salicided gate conductors (EPO):
This subclass is indented under subclass E21.621. This subclass is substantially the same in scope as ECLA classification H01L21/8234G2.

E21.623 Gate conductors with different gate conductor materials or different gate conductor implants, e.g., dual gate structures (EPO):
This subclass is indented under subclass E21.621. This subclass is substantially the same in scope as ECLA classification H01L21/8234G4.

E21.624 Gate conductors with different shapes, lengths or dimensions (EPO):
This subclass is indented under subclass E21.621. This subclass is substantially the same in scope as ECLA classification H01L21/8234G6.

E21.625 With particular manufacturing method of gate insulating layer, e.g., different gate insulating layer thicknesses, particular gate insulator materials or particular gate insulator implants (EPO):
This subclass is indented under subclass E21.616. This subclass is substantially the same in scope as ECLA classification H01L21/8234J.

E21.626 With particular manufacturing method of gate sidewall spacers, e.g., double spacers, particular spacer material or shape (EPO):
This subclass is indented under subclass E21.616. This subclass is substantially the same in scope as ECLA classification H01L21/8234S.

E21.627 Interconnection or wiring or contact manufacturing related aspects (EPO):
This subclass is indented under subclass E21.616. This subclass is substantially the

same in scope as ECLA classification H01L21/8234T.

E21.628 Isolation region manufacturing related aspects, e.g., to avoid interaction of isolation region with adjacent structure (EPO):
This subclass is indented under subclass E21.616. This subclass is substantially the same in scope as ECLA classification H01L21/8234U.

E21.629 With particular manufacturing method of vertical transistor structures, i.e., with channel vertical to substrate surface (EPO):
This subclass is indented under subclass E21.616. This subclass is substantially the same in scope as ECLA classification H01L21/8234V.

E21.63 With particular manufacturing method of wells or tubs, e.g., twin tubs, high energy well implants, buried implanted layers for lateral isolation (BILLI) (EPO):
This subclass is indented under subclass E21.616. This subclass is substantially the same in scope as ECLA classification H01L21/8234W.

E21.631 Combination of enhancement and depletion transistors (EPO):
This subclass is indented under subclass E21.616. This subclass is substantially the same in scope as ECLA classification H01L21/8236.

E21.632 Complementary field-effect transistors, e.g., CMOS (EPO):
This subclass is indented under subclass E21.616. This subclass is substantially the same in scope as ECLA classification H01L21/8238.

E21.633 With particular manufacturing method of channel, e.g., channel implants, halo or pocket implants, or channel materials (EPO):
This subclass is indented under subclass E21.632. This subclass is substantially the same in scope as ECLA classification H01L21/8238C.

E21.634 With particular manufacturing method of source or drain, e.g., specific S or D implants or silicided S or D structures or raised S or D structures (EPO):
This subclass is indented under subclass E21.632. This subclass is substantially the same in scope as ECLA classification H01L21/8238D.

E21.635 With particular manufacturing method of gate conductor, e.g., particular materials, shapes (EPO):
This subclass is indented under subclass E21.632. This subclass is substantially the same in scope as ECLA classification H01L21/8238G.

E21.636 Silicided or salicided gate conductors (EPO):
This subclass is indented under subclass E21.635. This subclass is substantially the same in scope as ECLA classification H01L21/8238G2.

E21.637 Gate conductors with different gate conductor materials or different gate conductor implants, e.g., dual gate structures (EPO):
This subclass is indented under subclass E21.635. This subclass is substantially the same in scope as ECLA classification H01L21/8238G4.

E21.638 Gate conductors with different shapes, lengths or dimensions (EPO):
This subclass is indented under subclass E21.635. This subclass is substantially the same in scope as ECLA classification H01L21/8238G6.

E21.639 With particular manufacturing method of gate insulating layer, e.g., different gate insulating layer thicknesses, particular gate insulator materials or particular gate insulator implants (EPO):
This subclass is indented under subclass E21.632. This subclass is substantially the same in scope as ECLA classification H01L21/8238J.

E21.64 With particular manufacturing method of gate sidewall spacers, e.g., double spacers, particular spacer material or shape (EPO):
This subclass is indented under subclass E21.632. This subclass is substantially the same in scope as ECLA classification H01L21/8238S.

E21.641 Interconnection or wiring or contact manufacturing related aspects (EPO):
This subclass is indented under subclass E21.632. This subclass is substantially the same in scope as ECLA classification H01L21/8238T.

E21.642 Isolation region manufacturing related aspects, e.g., to avoid interaction of isolation region with adjacent structure (EPO):
This subclass is indented under subclass E21.632. This subclass is substantially the same in scope as ECLA classification H01L21/8238U.

E21.643 With particular manufacturing method of vertical transistor structures, i.e., with channel vertical to substrate surface (EPO):
This subclass is indented under subclass E21.632. This subclass is substantially the same in scope as ECLA classification H01L21/8238V.

E21.644 With particular manufacturing method of wells or tubs, e.g., twin tubs, high energy well implants, buried implanted layers for lateral isolation (BILLI) (EPO):
This subclass is indented under subclass E21.616. This subclass is substantially the same in scope as ECLA classification H01L21/8238W.

E21.645 Memory structures (EPO):
This subclass is indented under subclass E21.616. This subclass is substantially the same in scope as ECLA classification H01L21/8239.

E21.646 Dynamic random access memory structures (DRAM) (EPO):
This subclass is indented under subclass E21.645. This subclass is substantially the same in scope as ECLA classification H01L21/8242.

E21.647 Characterized by type of capacitor (EPO):
This subclass is indented under subclass E21.646. This subclass is substantially the same in scope as ECLA classification H01L21/8242B.

E21.648 Capacitor stacked over transfer transistor (EPO):
This subclass is indented under subclass E21.647. This subclass is substantially the same in scope as ECLA classification H01L21/8242B2.

SEE OR SEARCH THIS CLASS, SUBCLASS:
E21.008,and E21.396, for manufacturing of the capacitor, per se.

E21.649 Making connection between transistor and capacitor, e.g., plug (EPO):
This subclass is indented under subclass E21.648. This subclass is substantially the same in scope as ECLA classification H01L21/8242B2C.

E21.65 Capacitor extending under transfer transistor area (EPO):
This subclass is indented under subclass E21.647. This subclass is substantially the same in scope as ECLA classification H01L21/8242B4.

E21.651 Capacitor in U- or V-shaped trench in substrate (EPO):
This subclass is indented under subclass E21.647. This subclass is substantially the same in scope as ECLA classification H01L21/8242B6.

E21.652 In combination with vertical transistor (EPO):
This subclass is indented under subclass E21.651. This subclass is substantially the same in scope as ECLA classification H01L21/8242B6B.

E21.653 Making connection between transistor and capacitor, e.g., buried strap (EPO):
This subclass is indented under subclass E21.651. This subclass is substantially the same in scope as ECLA classification H01L21/8242B6C.

E21.654 Characterized by type of transistor; manufacturing of transistor (EPO):
This subclass is indented under subclass E21.646. This subclass is substantially the same in scope as ECLA classification H01L21/8242C.

E21.655 Transistor in U- or V-shaped trench in substrate (EPO):
This subclass is indented under subclass E21.654. This subclass is substantially the same in scope as ECLA classification H01L21/8242C2.

E21.656 Characterized by data lines (EPO):
This subclass is indented under subclass E21.646. This subclass is substantially the same in scope as ECLA classification H01L21/8242D.

E21.657 Making bit line (EPO):
This subclass is indented under subclass E21.656. This subclass is substantially the same in scope as ECLA classification H01L21/8242D2.

E21.658 Making bit line contact (EPO):
This subclass is indented under subclass E21.656. This subclass is substantially the same in scope as ECLA classification H01L21/8242D4.

E21.659 Making word line (EPO):
This subclass is indented under subclass E21.656. This subclass is substantially the same in scope as ECLA classification H01L21/8242D6.

E21.66 Simultaneous fabrication of periphery and memory cells (EPO):
This subclass is indented under subclass E21.646. This subclass is substantially the same in scope as ECLA classification H01L21/8242P.

E21.661 Static random access memory structures (SRAM) (EPO):
This subclass is indented under subclass E21.645. This subclass is substantially the same in scope as ECLA classification H01L21/8244.

E21.662 Read-only memory structures (ROM), i.e., nonvolatile memory structures (EPO):
This subclass is indented under subclass E21.645. This subclass is substantially the same in scope as ECLA classification H01L21/8246.

SEE OR SEARCH THIS CLASS, SUBCLASS:
E21.004,for manufacture of the resistor, per se.

E21.663 Ferroelectric nonvolatile memory structures (EPO):
This subclass is indented under subclass E21.662. This subclass is substantially the same in scope as ECLA classification H01L21/8246F.

E21.664 With ferroelectric capacitor (EPO):
This subclass is indented under subclass E21.663. This subclass is substantially the same in scope as ECLA classification H01L21/8246F6.

E21.665 Magnetic nonvolatile memory structures, e.g., MRAM (EPO):
This subclass is indented under subclass E21.662. This subclass is substantially the same in scope as ECLA classification H01L21/8246M.

E21.666 PROM (EPO):
This subclass is indented under subclass E21.662. This subclass is substantially the same in scope as ECLA classification H01L21/8246P.

E21.667 ROM only (EPO):
This subclass is indented under subclass E21.662. This subclass is substantially the same in scope as ECLA classification H01L21/8246R.

E21.668 With source and drain on same level, e.g., lateral channel (EPO):
This subclass is indented under subclass E21.667. This subclass is substantially the same in scope as ECLA classification H01L21/8246R2.

E21.669 Source or drain contact programmed (EPO):
This subclass is indented under subclass E21.668. This subclass is substantially the same in scope as ECLA classification H01L21/8246R2B.

E21.67 Gate contact programmed (EPO):
This subclass is indented under subclass E21.668. This subclass is substantially the

same in scope as ECLA classification H01L21/8246R2C.

E21.671 Doping programmed, e.g., mask ROM (EPO):
This subclass is indented under subclass E21.668. This subclass is substantially the same in scope as ECLA classification H01L21/8246R2D.

E21.672 Entire channel doping programmed (EPO):
This subclass is indented under subclass E21.671. This subclass is substantially the same in scope as ECLA classification H01L21/8246R2D4.

E21.673 Source or drain doping programmed (EPO):
This subclass is indented under subclass E21.671. This subclass is substantially the same in scope as ECLA classification H01L21/8246R2D6.

E21.674 Gate programmed, e.g., different gate material or no gate (EPO):
This subclass is indented under subclass E21.668. This subclass is substantially the same in scope as ECLA classification H01L21/8246R2G.

E21.675 Gate dielectric programmed, e.g., different thickness (EPO):
This subclass is indented under subclass E21.668. This subclass is substantially the same in scope as ECLA classification H01L21/8246R2T.

E21.676 With source and drain on different levels, e.g., vertical channel (EPO):
This subclass is indented under subclass E21.667. This subclass is substantially the same in scope as ECLA classification H01L21/8246R4.

E21.677 With FETs on different levels, e.g., 3D ROM (EPO):
This subclass is indented under subclass E21.667. This subclass is substantially the same in scope as ECLA classification H01L21/8246R6.

E21.678 Simultaneous fabrication of periphery and memory cells (EPO):
This subclass is indented under subclass E21.667. This subclass is substantially the same in scope as ECLA classification H01L21/8246R8.

E21.679 Charge trapping insulator nonvolatile memory structures (EPO):
This subclass is indented under subclass E21.662. This subclass is substantially the same in scope as ECLA classification H01L21/8246T.

E21.68 Electrically programmable (EPROM), i.e., floating gate memory structures (EPO):
This subclass is indented under subclass E21.662. This subclass is substantially the same in scope as ECLA classification H01L21/8247.

E21.681 With conductive layer as control gate (EPO):
This subclass is indented under subclass E21.68. This subclass is substantially the same in scope as ECLA classification H01L21/8247M.

E21.682 With source and drain on same level and without cell select transistor (EPO):
This subclass is indented under subclass E21.681. This subclass is substantially the same in scope as ECLA classification H01L21/8247M2.

E21.683 Simultaneous fabrication of periphery and memory cells (EPO):
This subclass is indented under subclass E21.682. This subclass is substantially the same in scope as ECLA classification H01L21/8247M2P.

E21.684 Including one type of peripheral FET (EPO):
This subclass is indented under subclass E21.683. This subclass is substantially the same in scope as ECLA classification H01L21/8247M2P1.

E21.685 Control gate layer used for peripheral FET (EPO):
This subclass is indented under subclass E21.684. This subclass is substantially the

same in scope as ECLA classification H01L21/8247M2P1C.

E21.686 Intergate dielectric layer used for peripheral FET (EPO):
This subclass is indented under subclass E21.684. This subclass is substantially the same in scope as ECLA classification H01L21/8247M2P1D.

E21.687 Floating gate layer used for peripheral FET (EPO):
This subclass is indented under subclass E21.684. This subclass is substantially the same in scope as ECLA classification H01L21/8247M2P1F.

E21.688 Floating gate dielectric layer used for peripheral FET (EPO):
This subclass is indented under subclass E21.684. This subclass is substantially the same in scope as ECLA classification H01L21/8247M2P1G.

E21.689 Including different types of peripheral FETs (EPO):
This subclass is indented under subclass E21.683. This subclass is substantially the same in scope as ECLA classification H01L21/8247M2P2.

E21.69 With source and drain on same level and with cell select transistor (EPO):
This subclass is indented under subclass E21.681. This subclass is substantially the same in scope as ECLA classification H01L21/8247M4.

E21.691 Simultaneous fabrication of periphery and memory cells (EPO):
This subclass is indented under subclass E21.69. This subclass is substantially the same in scope as ECLA classification H01L21/8247M4P.

E21.692 With source and drain on different levels, e.g., sloping channel (EPO):
This subclass is indented under subclass E21.681. This subclass is substantially the same in scope as ECLA classification H01L21/8247M8.

E21.693 For vertical channel (EPO):
This subclass is indented under subclass E21.692. This subclass is substantially the same in scope as ECLA classification H01L21/8247M8V.

E21.694 With doped region as control gate (EPO):
This subclass is indented under subclass E21.68. This subclass is substantially the same in scope as ECLA classification H01L21/8247S.

E21.695 Combination of bipolar and field-effect technologies (EPO):
This subclass is indented under subclass E21.606. This subclass is substantially the same in scope as ECLA classification H01L21/8248.

E21.696 Bipolar and MOS technologies (EPO):
This subclass is indented under subclass E21.695. This subclass is substantially the same in scope as ECLA classification H01L21/8249.

E21.697 Substrate is Group III-V semiconductor (EPO):
This subclass is indented under subclass E21.602. This subclass is substantially the same in scope as ECLA classification H01L21/8252.

E21.698 Substrate is Group II-VI semiconductor (EPO):
This subclass is indented under subclass E21.602. This subclass is substantially the same in scope as ECLA classification H01L21/8254.

E21.699 Substrate is semiconductor other than diamond, SiC, Si, Group III-V compound, or Group II-VI compound (EPO):
This subclass is indented under subclass E21.602. This subclass is substantially the same in scope as ECLA classification H01L21/8256.

E21.7 Substrate is nonsemiconductor body, e.g., insulating body (EPO):
This subclass is indented under subclass E21.695. This subclass is substantially the same in scope as ECLA classification H01L21/782.

SEE OR SEARCH THIS CLASS, SUBCLASS:
E21.604, for diamond.
E21.605, for silicon carbide.
E21.606, for silicon.
E21.697, for III-V compound semiconductors.
E21.698, for III-V compound semiconductors.

E21.701 Substrate is sapphire, e.g., silicon on sapphire structure (SOS) (EPO):
This subclass is indented under subclass E21.7. This subclass is substantially the same in scope as ECLA classification H01L21/784.

E21.702 To produce devices, each consisting of single circuit element (EPO):
This subclass is indented under subclass E21.599. This subclass is substantially the same in scope as ECLA classification H01L21/786.

E21.703 Substrate is semiconductor body (EPO):
This subclass is indented under subclass E21.702. This subclass is substantially the same in scope as ECLA classification H01L21/84.

E21.704 Substrate is nonsemiconductor body, e.g., insulating body (EPO):
This subclass is indented under subclass E21.702. This subclass is substantially the same in scope as ECLA classification H01L21/86.

E21.705 Assembly of devices consisting of solid-state components formed in or on common substrate; assembly of integrated circuit devices (EPO):
This subclass is indented under subclass E21.532. This subclass is substantially the same in scope as ECLA classification H01L21/98.

E23.001 PACKAGING, INTERCONNECTS, AND MARKINGS FOR SEMICONDUCTOR OR OTHER SOLID-STATE DEVICES (EPO):
This main group provides for preformed physical means to cover or protect semiconductor or other solid state devices, electrical interconnection of such devices and lead elements for facilitating electrical interconnection of the chips or dies via intermediate (e.g., jumper) connections to other devices or components, and marks applied to chips or dies such as test patterns or alignment marks. This subclass is substantially the same in scope as ECLA classification H01L23/00.

E23.002 Details not otherwise provided for, e.g., protection against moisture (EPO):
This subclass is indented under subclass E23.001. This subclass is substantially the same in scope as ECLA classification H01L23/00V.

SEE OR SEARCH THIS CLASS, SUBCLASS:
E23.137, for getters.

E23.003 Mountings, e.g., nondetachable insulating substrates (EPO):
This subclass is indented under subclass E23.001. This subclass is substantially the same in scope as ECLA classification H01L23/12.

E23.004 Characterized by shape (EPO):
This subclass is indented under subclass E23.003. This subclass is substantially the same in scope as ECLA classification H01L23/13.

E23.005 Characterized by material or its electrical properties (EPO):
This subclass is indented under subclass E23.003. This subclass is substantially the same in scope as ECLA classification H01L23/14.

E23.006 Metallic substrates having insulating layers (EPO):
This subclass is indented under subclass E23.005. This subclass is substantially the same in scope as ECLA classification H01L23/14M.

E23.007 Organic substrates, e.g., plastic (EPO):
This subclass is indented under subclass E23.005. This subclass is substantially the same in scope as ECLA classification H01L23/14P.

E23.008 Semiconductor insulating substrates (EPO):
This subclass is indented under subclass E23.005. This subclass is substantially the

same in scope as ECLA classification H01L23/14S.

SEE OR SEARCH THIS CLASS, SUBCLASS:
E23.029,for semiconductor conductive substrates.

E23.009 Ceramic or glass substrates (EPO):
This subclass is indented under subclass E23.005. This subclass is substantially the same in scope as ECLA classification H01L23/15.

E23.01 Arrangements for conducting electric current to or from solid-state body in operation, e.g., leads, terminal arrangements (EPO):
This subclass is indented under subclass E23.001. This subclass is substantially the same in scope as ECLA classification H01L23/48.

E23.011 Internal lead connections, e.g., via connections, feedthrough structures (EPO):
This subclass is indented under subclass E23.01. This subclass is substantially the same in scope as ECLA classification H01L23/48J.

E23.012 Consisting of lead-in layers inseparably applied to semiconductor body (EPO):
This subclass is indented under subclass E23.01. This subclass is substantially the same in scope as ECLA classification H01L23/482.

E23.013 Bridge structure with air gap (EPO):
This subclass is indented under subclass E23.012. This subclass is substantially the same in scope as ECLA classification H01L23/482A.

E23.014 Beam leads (EPO):
This subclass is indented under subclass E23.012. This subclass is substantially the same in scope as ECLA classification H01L23/482B.

E23.015 Pads with extended contours, e.g., grid structure, branch structure, finger structure (EPO):
This subclass is indented under subclass E23.012. This subclass is substantially the same in scope as ECLA classification H01L23/482E.

E23.016 For devices consisting of semiconductor layers on insulating or semi-insulating substrates, e.g., silicon on sapphire devices, i.e., SOS (EPO):
This subclass is indented under subclass E23.012. This subclass is substantially the same in scope as ECLA classification H01L23/482J.

E23.017 Materials (EPO):
This subclass is indented under subclass E23.012. This subclass is substantially the same in scope as ECLA classification H01L23/482M.

E23.018 Conductive organic material or pastes, e.g., conductive adhesives, inks (EPO):
This subclass is indented under subclass E23.017. This subclass is substantially the same in scope as ECLA classification H01L23/482M4.

E23.019 Consisting of layered constructions comprising conductive layers and insulating layers, e.g., planar contacts (EPO):
This subclass is indented under subclass E23.012. This subclass is substantially the same in scope as ECLA classification H01L23/485.

E23.02 Bonding areas, e.g., pads (EPO):
This subclass is indented under subclass E23.019. This subclass is substantially the same in scope as ECLA classification H01L23/485A.

E23.021 Bump or ball contacts (EPO):
This subclass is indented under subclass E23.019. This subclass is substantially the same in scope as ECLA classification H01L23/485B.

E23.022 Overhang structure (EPO):
This subclass is indented under subclass E23.019. This subclass is substantially the same in scope as ECLA classification H01L23/485H.

E23.023 Consisting of soldered or bonded constructions (EPO):
This subclass is indented under subclass E23.01. This subclass is substantially the same in scope as ECLA classification H01L23/488.

E23.024 Wire-like arrangements or pins or rods (EPO):
This subclass is indented under subclass E23.023. This subclass is substantially the same in scope as ECLA classification H01L23/49.

E23.025 Characterized by materials of wires or their coatings (EPO):
This subclass is indented under subclass E23.024. This subclass is substantially the same in scope as ECLA classification H01L23/49M.

E23.026 Bases or plates or solder therefor (EPO):
This subclass is indented under subclass E23.023. This subclass is substantially the same in scope as ECLA classification H01L23/492.

E23.027 Having heterogeneous or anisotropic structure (EPO):
This subclass is indented under subclass E26.026. This subclass is substantially the same in scope as ECLA classification H01L23/492H.

E23.028 Characterized by material (EPO):
This subclass is indented under subclass E23.026. This subclass is substantially the same in scope as ECLA classification H01L23/492M.

E23.029 Semiconductor (EPO):
This subclass is indented under subclass E23.028. This subclass is substantially the same in scope as ECLA classification H01L23/492M2.

E23.03 Carbon (EPO):
This subclass is indented under subclass E23.028. This subclass is substantially the same in scope as ECLA classification H01L23/492M3.

E23.031 Lead frames or other flat leads (EPO):
This subclass is indented under subclass E23.023. This subclass is substantially the same in scope as ECLA classification H01L23/495.

SEE OR SEARCH THIS CLASS, SUBCLASS:
E23.141,for lead frame interconnections between components.

E23.032 Additional leads (EPO):
This subclass is indented under subclass E23.031. This subclass is substantially the same in scope as ECLA classification H01L23/495C.

E23.033 Additional leads being bump or wire (EPO):
This subclass is indented under subclass E23.032. This subclass is substantially the same in scope as ECLA classification H01L23/495C2.

E23.034 Additional leads being tape carrier or flat leads (EPO):
This subclass is indented under subclass E23.032. This subclass is substantially the same in scope as ECLA classification H01L23/495C4.

E23.035 Additional leads being multilayer (EPO):
This subclass is indented under subclass E23.032. This subclass is substantially the same in scope as ECLA classification H01L23/495C6.

E23.036 Additional leads being wiring board (EPO):
This subclass is indented under subclass E23.032. This subclass is substantially the same in scope as ECLA classification H01L23/495C8.

E23.037 Characterized by die pad (EPO):
This subclass is indented under subclass E23.031. This subclass is substantially the same in scope as ECLA classification H01L23/495A.

E23.038 Insulative substrate being used as die pad, e.g., ceramic, plastic (EPO):
This subclass is indented under subclass E23.037. This subclass is substantially the same in scope as ECLA classification H01L23/495A2.

E23.039 Chip-on-leads or leads-on-chip techniques, i.e., inner lead fingers being used as die pad (EPO):
This subclass is indented under subclass E23.037. This subclass is substantially the same in scope as ECLA classification H01L23/495A4.

E23.04 Having bonding material between chip and die pad (EPO):
This subclass is indented under subclass E23.037. This subclass is substantially the same in scope as ECLA classification H01L23/495A6.

E23.041 Multi layer (EPO):
This subclass is indented under subclass E23.031. This subclass is substantially the same in scope as ECLA classification H01L23/495D.

E23.042 Plurality of lead frames mounted in one device (EPO):
This subclass is indented under subclass E23.031. This subclass is substantially the same in scope as ECLA classification H01L23/495F.

E23.043 Geometry of lead frame (EPO):
This subclass is indented under subclass E23.031. This subclass is substantially the same in scope as ECLA classification H01L23/495G.

E23.044 For devices adapted for rectifying, amplifying, oscillating, or switching, capacitors, or resistors with at least one potential-jump barrier or surface barrier (EPO):
This subclass is indented under subclass E23.043. This subclass is substantially the same in scope as ECLA classification H01L23/495G8.

E23.045 Deformation absorbing parts in lead frame plane, e.g., meanderline shape (EPO):
This subclass is indented under subclass E23.043. This subclass is substantially the same in scope as ECLA classification H01L23/495G2.

E23.046 Cross-section geometry (EPO):
This subclass is indented under subclass E23.043. This subclass is substantially the same in scope as ECLA classification H01L23/495G4.

E23.047 Characterized by bent parts (EPO):
This subclass is indented under subclass E23.046. This subclass is substantially the same in scope as ECLA classification H01L23/495G4B.

E23.048 Bent parts being outer leads (EPO):
This subclass is indented under subclass E23.047. This subclass is substantially the same in scope as ECLA classification H01L23/495G4B6.

E23.049 Insulating layers on lead frame, e.g., bridging members (EPO):
This subclass is indented under subclass E23.043. This subclass is substantially the same in scope as ECLA classification H01L23/495G6.

E23.05 Side rails of lead frame, e.g., with perforations, sprocket holes (EPO):
This subclass is indented under subclass E23.043. This subclass is substantially the same in scope as ECLA classification H01L23/495G9.

E23.051 Specifically adapted to facilitate heat dissipation (EPO):
This subclass is indented under subclass E21.031. This subclass is substantially the same in scope as ECLA classification H01L23/495H.

E23.052 Assembly of semiconductor devices on lead frame (EPO):
This subclass is indented under subclass E21.031. This subclass is substantially the same in scope as ECLA classification H01L23/495L.

E23.053 Characterized by materials of lead frames or layers thereon (EPO):
This subclass is indented under subclass E21.031. This subclass is substantially the same in scope as ECLA classification H01L23/495M.

E23.054 Metallic layers on lead frames (EPO):
This subclass is indented under subclass E23.053. This subclass is substantially the

same in scope as ECLA classification H01L23/495M1.

E23.055 Consisting of thin flexible metallic tape with or without film carrier (EPO):
This subclass is indented under subclass E23.031. This subclass is substantially the same in scope as ECLA classification H01L23/495J.

E23.056 Insulating layers on lead frames (EPO):
This subclass is indented under subclass E23.031. This subclass is substantially the same in scope as ECLA classification H01L23/495M8.

E23.057 Capacitor integral with or on lead frame (EPO):
This subclass is indented under subclass E23.031. This subclass is substantially the same in scope as ECLA classification H01L23/495Q.

E23.058 Battery in combination with lead frame (EPO):
This subclass is indented under subclass E23.031. This subclass is substantially the same in scope as ECLA classification H01L23/495R.

E23.059 Oscillators in combination with lead frame (EPO):
This subclass is indented under subclass E23.031. This subclass is substantially the same in scope as ECLA classification H01L23/495S.

E23.06 Leads, i.e., metallizations or lead frames on insulating substrates, e.g., chip carriers (EPO):
This subclass is indented under subclass E23.023. This subclass is substantially the same in scope as ECLA classification H01L23/498.

E23.061 Leads being also applied on sidewalls or bottom of substrate, e.g., leadless packages for surface mounting (EPO):
This subclass is indented under subclass E23.06. This subclass is substantially the same in scope as ECLA classification H01L23/498A.

E23.062 Multilayer substrates (EPO):
This subclass is indented under subclass E23.06. This subclass is substantially the same in scope as ECLA classification H01L23/498D.

E23.063 Chip support structure consisting of plurality of insulating substrates (EPO):
This subclass is indented under subclass E23.06. This subclass is substantially the same in scope as ECLA classification H01L23/498F.

E23.064 For flat cards, e.g., credit cards (EPO):
This subclass is indented under subclass E23.06. This subclass is substantially the same in scope as ECLA classification H01L23/498K.

E23.065 Flexible insulating substrates (EPO):
This subclass is indented under subclass E23.06. This subclass is substantially the same in scope as ECLA classification H01L23/498J.

E23.066 Lead frames fixed on or encapsulated in insulating substrates (EPO):
This subclass is indented under subclass E23.06. This subclass is substantially the same in scope as ECLA classification H01L23/498L.

E23.067 Via connections through substrates, e.g., pins going through substrate, coaxial cables (EPO):
This subclass is indented under subclass E23.06. This subclass is substantially the same in scope as ECLA classification H01L23/498E.

E23.068 Additional leads joined to metallizations on insulating substrate, e.g., pins, bumps, wires, flat leads (EPO):
This subclass is indented under subclass E23.06. This subclass is substantially the same in scope as ECLA classification H01L23/498C.

E23.069 Spherical bumps on substrate for external connection, e.g., ball grid arrays (BGA) (EPO):
This subclass is indented under subclass E23.068. This subclass is substantially the same in scope as ECLA classification H01L23/498C4.

E23.07 Geometry or layout (EPO):
This subclass is indented under subclass E23.06. This subclass is substantially the same in scope as ECLA classification H01L23/498G.

E23.071 For devices adapted for rectifying, amplifying, oscillating, or switching, capacitors, or resistors with at least one potential-jump barrier or surface barrier (EPO):
This subclass is indented under subclass E23.07. This subclass is substantially the same in scope as ECLA classification H01L23/498G8.

E23.072 Characterized by materials (EPO):
This subclass is indented under subclass E23.06. This subclass is substantially the same in scope as ECLA classification H01L23/498M.

SEE OR SEARCH THIS CLASS, SUBCLASS:
E23.005, for materials of the substrates.
E23.053, for materials of the lead-frames.

E23.073 Conductive materials containing semiconductor material (EPO):
This subclass is indented under subclass E23.072. This subclass is substantially the same in scope as ECLA classification H01L23/498M2.

E23.074 Carbon, e.g., fullerenes (EPO):
This subclass is indented under subclass E23.072. This subclass is substantially the same in scope as ECLA classification H01L23/498M3.

SEE OR SEARCH THIS CLASS, SUBCLASS:
E39.008,for superconducting fullerenes.

E23.075 Conductive materials containing organic materials or pastes, e.g., for thick films (EPO):
This subclass is indented under subclass E23.072. This subclass is substantially the same in scope as ECLA classification H01L23/498M4.

E23.076 Conductive materials containing superconducting material (EPO):
This subclass is indented under subclass E23.072. This subclass is substantially the same in scope as ECLA classification H01L23/498M6.

E23.077 Materials of insulating layers or coatings (EPO):
This subclass is indented under subclass E23.072. This subclass is substantially the same in scope as ECLA classification H01L23/498M8.

E23.078 Flexible arrangements, e.g., pressure contacts without soldering (EPO):
This subclass is indented under subclass E23.01. This subclass is substantially the same in scope as ECLA classification H01L23/48F.

E23.079 For integrated circuit devices, e.g., power bus, number of leads (EPO):
This subclass is indented under subclass E23.01. This subclass is substantially the same in scope as ECLA classification H01L23/50.

E23.08 Arrangements for cooling, heating, ventilating or temperature compensation; temperature-sensing arrangements (EPO):
This subclass is indented under subclass E23.001. This subclass is substantially the same in scope as ECLA classification H01L23/34.

E23.081 Arrangements for heating (EPO):
This subclass is indented under subclass E23.08. This subclass is substantially the same in scope as ECLA classification H01L23/34H.

E23.082 Cooling arrangements using Peltier effect (EPO):
This subclass is indented under subclass E23.08. This subclass is substantially the same in scope as ECLA classification H01L23/38.

E23.083 Mountings or securing means for detachable cooling or heating arrangements; fixed by friction, plugs or springs (EPO):
This subclass is indented under subclass E23.08. This subclass is substantially the same in scope as ECLA classification H01L23/40.

E23.084 With bolts or screws (EPO):
This subclass is indented under subclass E23.083. This subclass is substantially the same in scope as ECLA classification H01L23/40B.

E23.085 For stacked arrangements of plurality of semiconductor devices (EPO):
This subclass is indented under subclass E23.084. This subclass is substantially the same in scope as ECLA classification H01L23/40B8.

E23.086 Snap-on arrangements, e.g., clips (EPO):
This subclass is indented under subclass E23.083. This subclass is substantially the same in scope as ECLA classification H01L23/40S.

E23.087 Fillings or auxiliary members in containers or encapsulations selected or arranged to facilitate heating or cooling (EPO):
This subclass is indented under subclass E23.08. This subclass is substantially the same in scope as ECLA classification H01L23/42.

E23.088 Cooling by change of state, e.g., use of heat pipes (EPO):
This subclass is indented under subclass E23.087. This subclass is substantially the same in scope as ECLA classification H01L23/427.

E23.089 By melting or evaporation of solids (EPO):
This subclass is indented under subclass E23.088. This subclass is substantially the same in scope as ECLA classification H01L23/427S.

E23.09 Auxiliary members in containers characterized by their shape, e.g., pistons (EPO):
This subclass is indented under subclass E23.087. This subclass is substantially the same in scope as ECLA classification H01L23/433.

E23.091 Bellows (EPO):
This subclass is indented under subclass E23.09. This subclass is substantially the same in scope as ECLA classification H01L23/433B.

E23.092 Auxiliary members in encapsulations (EPO):
This subclass is indented under subclass E23.09. This subclass is substantially the same in scope as ECLA classification H01L23/433E.

E23.093 In combination with jet impingement (EPO):
This subclass is indented under subclass E23.09. This subclass is substantially the same in scope as ECLA classification H01L23/433J.

E23.094 Pistons, e.g., spring-loaded members (EPO):
This subclass is indented under subclass E23.09. This subclass is substantially the same in scope as ECLA classification H01L23/433P.

E23.095 Complete device being wholly immersed in fluid other than air (EPO):
This subclass is indented under subclass E23.08. This subclass is substantially the same in scope as ECLA classification H01L23/44.

E23.096 Fluid being liquefied gas, e.g., in cryogenic vessel (EPO):
This subclass is indented under subclass E23.095. This subclass is substantially the same in scope as ECLA classification H01L23/44C.

E23.097 Involving transfer of heat by flowing fluids (EPO):
This subclass is indented under subclass E23.08. This subclass is substantially the same in scope as ECLA classification H01L23/46.

E23.098 By flowing liquids (EPO):
This subclass is indented under subclass E23.097. This subclass is substantially the same in scope as ECLA classification H01L23/473.

E23.099 By flowing gases, e.g., air (EPO):
This subclass is indented under subclass E23.097. This subclass is substantially the same in scope as ECLA classification H01L23/467.

E23.1 Jet impingement (EPO):
This subclass is indented under subclassE23.099. This subclass is substantially

the same in scope as ECLA classification H01L23/473J.

E23.101 Selection of materials, or shaping, to facilitate cooling or heating, e.g., heat sinks (EPO):
This subclass is indented under subclass E23.08. This subclass is substantially the same in scope as ECLA classification H01L23/36.

SEE OR SEARCH THIS CLASS, SUBCLASS:
E23.081, for heating.

E23.102 Cooling facilitated by shape of device (EPO):
This subclass is indented under subclass E23.101. This subclass is substantially the same in scope as ECLA classification H01L23/367.

E23.103 Foil-like cooling fins or heat sinks (EPO):
This subclass is indented under subclass E23.102. This subclass is substantially the same in scope as ECLA classification H01L23/367F.

SEE OR SEARCH THIS CLASS, SUBCLASS:
E23.051,for foil-like cooling fins or heat sinks being part of lead-frames.

E23.104 Characterized by shape of housing (EPO):
This subclass is indented under subclass E23.102. This subclass is substantially the same in scope as ECLA classification H01L23/367H.

E23.105 Wire-like or pin-like cooling fins or heat sinks (EPO):
This subclass is indented under subclass E23.102. This subclass is substantially the same in scope as ECLA classification H01L23/367W.

E23.106 Laminates or multilayers, e.g., direct bond copper ceramic substrates (EPO):
This subclass is indented under subclass E23.101. This subclass is substantially the same in scope as ECLA classification H01L23/373L.

E23.107 Organic materials with or without thermoconductive filler (EPO):
This subclass is indented under subclass E23.106. This subclass is substantially the same in scope as ECLA classification H01L23/373P.

E23.108 Semiconductor materials (EPO):
This subclass is indented under subclass E23.106. This subclass is substantially the same in scope as ECLA classification H01L23/373S.

E23.109 Metallic materials (EPO):
This subclass is indented under subclass E23.106. This subclass is substantially the same in scope as ECLA classification H01L23/373M.

E23.11 Cooling facilitated by selection of materials for device (or materials for thermal expansion adaptation, e.g., carbon) (EPO):
This subclass is indented under subclass E23.101. This subclass is substantially the same in scope as ECLA classification H01L23/373.

E23.111 Diamond (EPO):
This subclass is indented under subclass E23.11. This subclass is substantially the same in scope as ECLA classification H01L23/373D.

E23.112 Having heterogeneous or anisotropic structure, e.g., powder or fibers in matrix, wire mesh, porous structures (EPO):
This subclass is indented under subclass E23.11. This subclass is substantially the same in scope as ECLA classification H01L23/373H.

E23.113 Ceramic materials or glass (EPO):
This subclass is indented under subclass E23.11. This subclass is substantially the same in scope as ECLA classification H01L23/373C.

E23.114 Protection against radiation, e.g., light, electromagnetic waves (EPO):
This subclass is indented under subclass E23.001. This subclass is substantially the same in scope as ECLA classification H01L23/552.

E23.115 Against alpha rays (EPO):
This subclass is indented under subclass E23.114. This subclass is substantially the same in scope as ECLA classification H01L23/556.

E23.116 Encapsulations, e.g., encapsulating layers, coatings, e.g., for protection (EPO):
This subclass is indented under subclass E23.001. This subclass is substantially the same in scope as ECLA classification H01L23/28.

SEE OR SEARCH THIS CLASS, SUBCLASS:
E23.167,for insulating layers for contacts or interconnections.

E23.117 Characterized by material, e.g., carbon (EPO):
This subclass is indented under subclass E23.116. This subclass is substantially the same in scope as ECLA classification H01L23/29.

E23.118 Oxides or nitrides or carbides, e.g., ceramics, glass (EPO):
This subclass is indented under subclass E23.117. This subclass is substantially the same in scope as ECLA classification H01L23/29C.

E23.119 Organic, e.g., plastic, epoxy (EPO):
This subclass is indented under subclass E23.117. This subclass is substantially the same in scope as ECLA classification H01L23/29P.

E23.12 Organo-silicon compounds, e.g., silicone (EPO):
This subclass is indented under subclass E23.119. This subclass is substantially the same in scope as ECLA classification H01L23/29P6.

E23.121 Containing filler (EPO):
This subclass is indented under subclass E23.119. This subclass is substantially the same in scope as ECLA classification H01L23/29P4.

E23.122 Semiconductor material, e.g., amorphous silicon (EPO):
This subclass is indented under subclass E23.117. This subclass is substantially the same in scope as ECLA classification H01L23/29S.

E23.123 Characterized by arrangement or shape (EPO):
This subclass is indented under subclass E23.116. This subclass is substantially the same in scope as ECLA classification H01L23/31.

E23.124 Device being completely enclosed (EPO):
This subclass is indented under subclass E23.123. This subclass is substantially the same in scope as ECLA classification H01L23/31H.

E23.125 Substrate forming part of encapsulation (EPO):
This subclass is indented under subclass E23.124. This subclass is substantially the same in scope as ECLA classification H01L23/31H2.

E23.126 Double encapsulation or coating and encapsulation (EPO):
This subclass is indented under subclass E23.124. This subclass is substantially the same in scope as ECLA classification H01L23/31H4.

E23.127 Sealing arrangements between parts, e.g., adhesion promoters (EPO):
This subclass is indented under subclass E23.124. This subclass is substantially the same in scope as ECLA classification H01L23/31H6.

E23.128 Encapsulation having cavity (EPO):
This subclass is indented under subclass E23.124. This subclass is substantially the same in scope as ECLA classification H01L23/31H8.

E23.129 Partial encapsulation or coating (EPO):
This subclass is indented under subclass E23.123. This subclass is substantially the same in scope as ECLA classification H01L23/31P.

SEE OR SEARCH THIS CLASS, SUBCLASS:
E21.240,for mask layer used as insulation layer.

E23.13 Coating being foil (EPO):
This subclass is indented under subclass E23.129. This subclass is substantially the same in scope as ECLA classification H01L23/31P4.

E23.131 Coating or filling in grooves made in semiconductor body (EPO):
This subclass is indented under subclass E23.129. This subclass is substantially the same in scope as ECLA classification H01L23/31P8.

E23.132 Coating being directly applied to semiconductor body, e.g., passivation layer (EPO):
This subclass is indented under subclass E23.129. This subclass is substantially the same in scope as ECLA classification H01L23/31P6.

E23.133 Coating also covering sidewalls of semiconductor body (EPO):
This subclass is indented under subclass E23.129. This subclass is substantially the same in scope as ECLA classification H01L23/31P10.

E23.134 Multilayer coating (EPO):
This subclass is indented under subclass E23.129. This subclass is substantially the same in scope as ECLA classification H01L23/31P12.

E23.135 Fillings or auxiliary members in containers or encapsulations, e.g., centering rings (EPO):
This subclass is indented under subclass E23.001. This subclass is substantially the same in scope as ECLA classification H01L23/16.

E23.136 Fillings characterized by material, its physical or chemical properties, or its arrangement within complete device (EPO):
This subclass is indented under subclass E23.135. This subclass is substantially the same in scope as ECLA classification H01L23/18.

E23.137 Including materials for absorbing or reacting with moisture or other undesired substances, e.g., getters (EPO):
This subclass is indented under subclass E23.136. This subclass is substantially the same in scope as ECLA classification H01L23/26.

E23.138 Gaseous at normal operating temperature of device (EPO):
This subclass is indented under subclass E23.136. This subclass is substantially the same in scope as ECLA classification H01L23/20.

E23.139 Liquid at normal operating temperature of device (EPO):
This subclass is indented under subclass E23.136. This subclass is substantially the same in scope as ECLA classification H01L23/22.

E23.14 Solid or gel at normal operating temperature of device (EPO):
This subclass is indented under subclass E23.136. This subclass is substantially the same in scope as ECLA classification H01L23/24.

E23.141 Arrangements for conducting electric current within device in operation from one component to another, interconnections, e.g., wires, lead frames (EPO):
This subclass is indented under subclass E23.001. This subclass is substantially the same in scope as ECLA classification H01L23/52.

E23.142 Including external interconnections consisting of multilayer structure of conductive and insulating layers inseparably formed on semiconductor body (EPO):
This subclass is indented under subclass E23.141. This subclass is substantially the same in scope as ECLA classification H01L23/522.

E23.143 Crossover interconnections (EPO):
This subclass is indented under subclass E23.142. This subclass is substantially the same in scope as ECLA classification H01L23/522A.

E23.144 Capacitive arrangements or effects of, or between wiring layers (EPO):
This subclass is indented under subclass E23.142. This subclass is substantially the same in scope as ECLA classification H01L23/522C.

E23.145 Via connections in multilevel interconnection structure (EPO):
This subclass is indented under subclass E23.142. This subclass is substantially the same in scope as ECLA classification H01L23/522E.

E23.146 With adaptable interconnections (EPO):
This subclass is indented under subclass E23.142. This subclass is substantially the same in scope as ECLA classification H01L23/525.

E23.147 Comprising antifuses, i.e., connections having their state changed from nonconductive to conductive (EPO):
This subclass is indented under subclass E23.146. This subclass is substantially the same in scope as ECLA classification H01L23/525A.

E23.148 Change of state resulting from use of external beam, e.g., laser beam or ion beam (EPO):
This subclass is indented under subclass E23.147. This subclass is substantially the same in scope as ECLA classification H01L23/525A4.

E23.149 Comprising fuses, i.e., connections having their state changed from conductive to nonconductive (EPO):
This subclass is indented under subclass E23.146. This subclass is substantially the same in scope as ECLA classification H01L23/525F.

E23.15 Change of state resulting from use of external beam, e.g., laser beam or ion beam (EPO):
This subclass is indented under subclass E23.149. This subclass is substantially the same in scope as ECLA classification H01L23/525F4.

E23.151 Geometry or layout of interconnection structure (EPO):
This subclass is indented under subclass E23.142. This subclass is substantially the same in scope as ECLA classification H01L23/528.

E23.152 Cross-sectional geometry (EPO):
This subclass is indented under subclass E23.151. This subclass is substantially the same in scope as ECLA classification H01L23/528C.

E23.153 Arrangements of power or ground buses (EPO):
This subclass is indented under subclass E23.151. This subclass is substantially the same in scope as ECLA classification H01L23/528P.

E23.154 Characterized by materials (EPO):
This subclass is indented under subclass E23.142. This subclass is substantially the same in scope as ECLA classification H01L23/532.

E23.155 Conductive materials (EPO):
This subclass is indented under subclass E23.154. This subclass is substantially the same in scope as ECLA classification H01L23/532M.

E23.156 Containing superconducting materials (EPO):
This subclass is indented under subclass E23.155. This subclass is substantially the same in scope as ECLA classification H01L23/532M6.

E23.157 Based on metals, e.g., alloys, metal silicides (EPO):
This subclass is indented under subclass E23.155. This subclass is substantially the same in scope as ECLA classification H01L23/532M1.

E23.158 Principal metal being aluminum (EPO):
This subclass is indented under subclass E23.157. This subclass is substantially the same in scope as ECLA classification H01L23/532M1A.

E23.159 Aluminum alloys (EPO):
This subclass is indented under subclass E23.158. This subclass is substantially the same in scope as ECLA classification H01L23/532M1A2.

E23.16 Additional layers associated with aluminum layers, e.g., adhesion, barrier, cladding layers (EPO):
This subclass is indented under subclass E23.158. This subclass is substantially the same in scope as ECLA classification H01L23/532M1A4.

E23.161 Principal metal being copper (EPO):
This subclass is indented under subclass E23.157. This subclass is substantially the same in scope as ECLA classification H01L23/532M1C.

E23.162 Principal metal being noble metal, e.g., gold (EPO):
This subclass is indented under subclass E23.157. This subclass is substantially the same in scope as ECLA classification H01L23/532M1N.

E23.163 Principal metal being refractory metal (EPO):
This subclass is indented under subclass E23.157. This subclass is substantially the same in scope as ECLA classification H01L23/532M1R.

E23.164 Containing semiconductor material, e.g., polysilicon (EPO):
This subclass is indented under subclass E23.155. This subclass is substantially the same in scope as ECLA classification H01L23/532M2.

E23.165 Containing carbon, e.g., fullerenes (EPO):
This subclass is indented under subclass E23.155. This subclass is substantially the same in scope as ECLA classification H01L23/532M3.

SEE OR SEARCH THIS CLASS, SUBCLASS:
E39.008, for superconducting fullerenes.

E23.166 Containing conductive organic materials or pastes, e.g., conductive adhesives, inks (EPO):
This subclass is indented under subclass E23.155. This subclass is substantially the same in scope as ECLA classification H01L23/532M4.

E23.167 Insulating materials (EPO):
This subclass is indented under subclass E23.154. This subclass is substantially the same in scope as ECLA classification H01L23/532N.

E23.168 Including internal interconnections, e.g., cross-under constructions (EPO):
This subclass is indented under subclass E23.141. This subclass is substantially the same in scope as ECLA classification H01L23/535.

SEE OR SEARCH THIS CLASS, SUBCLASS:
E23.011, for internal lead connections.

E23.169 Interconnection structure between plurality of semiconductor chips being formed on or in insulating substrates (EPO):
This subclass is indented under subclass E23.141. This subclass is substantially the same in scope as ECLA classification H01L23/538.

SEE OR SEARCH THIS CLASS, SUBCLASS:
E23.003, for mountings, per se.
E23.072, for materials of leads.

E23.17 Crossover interconnections, e.g., bridge stepovers (EPO):
This subclass is indented under subclass E23.169. This subclass is substantially the same in scope as ECLA classification H01L23/538A.

E23.171 Adaptable interconnections, e.g., for engineering changes (EPO):
This subclass is indented under subclass E23.169. This subclass is substantially the same in scope as ECLA classification H01L23/538B.

E23.172 Assembly of plurality of insulating substrates (EPO):
This subclass is indented under subclass E23.169. This subclass is substantially the same in scope as ECLA classification H01L23/538F.

E23.173 Multilayer substrates (EPO):
This subclass is indented under subclass E23.169. This subclass is substantially the same in scope as ECLA classification H01L23/538D.

SEE OR SEARCH THIS CLASS, SUBCLASS:
E23.169, for multilayer metallisation on monolayer substrates.

E23.174 Conductive vias through substrate with or without pins, e.g., buried coaxial conductors (EPO):
This subclass is indented under subclass E23.169. This subclass is substantially the same in scope as ECLA classification H01L23/538E.

SEE OR SEARCH THIS CLASS, SUBCLASS:
E23.068, for pins attached to insulating substrates.

E23.175 Geometry or layout of interconnection structure (EPO):
This subclass is indented under subclass E23.169. This subclass is substantially the in Same scope as ECLA classification H01L23/538G.

E23.176 For flat cards, e.g., credit cards (EPO):
This subclass is indented under subclass E23.169. This subclass is substantially the same in scope as ECLA classification H01L23/538K.

E23.177 Flexible insulating substrates (EPO):
This subclass is indented under subclass E23.169. This subclass is substantially the same in scope as ECLA classification H01L23/538J.

E23.178 Chips being integrally enclosed by interconnect and support structures (EPO):
This subclass is indented under subclass E23.169. This subclass is substantially the same in scope as ECLA classification H01L23/538V.

E23.179 Marks applied to semiconductor devices or parts, e.g., registration marks, test patterns, alignment structures, wafer maps (EPO):
This subclass is indented under subclass E23.001. This subclass is substantially the same in scope as ECLA classification H01L23/544.

SEE OR SEARCH THIS CLASS, SUBCLASS:
E21.522, for structural arrangements for measurement.

E23.18 Containers; seals (EPO):
This subclass is indented under subclass E23.001. This subclass is substantially the same in scope as ECLA classification H01L23/02.

E23.181 Characterized by shape of container or parts, e.g., caps, walls (EPO):
This subclass is indented under subclass E23.180. This subclass is substantially the same in scope as ECLA classification H01L23/04.

E23.182 Container being hollow construction having no base used as mounting for semiconductor body (EPO):
This subclass is indented under subclass E23.181. This subclass is substantially the same in scope as ECLA classification H01L23/04B.

E23.183 Container being hollow construction and having conductive base as mounting as well as lead for the semiconductor body (EPO):
This subclass is indented under subclass E23.181. This subclass is substantially the same in scope as ECLA classification H01L23/043.

E23.184 Other leads having insulating passage through base (EPO):
This subclass is indented under subclass E23.183. This subclass is substantially the

same in scope as ECLA classification H01L23/045.

E23.185 Other leads being parallel to base (EPO):
This subclass is indented under subclass E23.183. This subclass is substantially the same in scope as ECLA classification H01L23/047.

E23.186 Other leads being perpendicular to base (EPO):
This subclass is indented under subclass E23.183. This subclass is substantially the same in scope as ECLA classification H01L23/049.

E23.187 Another lead being formed by cover plate parallel to base plate, e.g., sandwich type (EPO):
This subclass is indented under subclass E23.183. This subclass is substantially the same in scope as ECLA classification H01L23/051.

E23.188 Container being hollow construction and having insulating or insulated base as mounting for semiconductor body (EPO):
This subclass is indented under subclass E23.181. This subclass is substantially the same in scope as ECLA classification H01L23/053.

E23.189 Leads being parallel to base (EPO):
This subclass is indented under subclass E23.188. This subclass is substantially the same in scope as ECLA classification H01L23/057.

E23.19 Leads having passage through base (EPO):
This subclass is indented under subclass E23.188. This subclass is substantially the same in scope as ECLA classification H01L23/055.

E23.191 Characterized by material of container or its electrical properties (EPO):
This subclass is indented under subclass E23.18. This subclass is substantially the same in scope as ECLA classification H01L23/06.

E23.192 Material being electrical insulator, e.g., glass (EPO):
This subclass is indented under subclass E23.191. This subclass is substantially the same in scope as ECLA classification H01L23/08.

E23.193 Characterized by material or arrangement of seals between parts, e.g., between cap and base of container or between leads and walls of container (EPO):
This subclass is indented under subclass E23.18. This subclass is substantially the same in scope as ECLA classification H01L23/10.

E23.194 Protection against mechanical damage (EPO):
This subclass is indented under subclass E23.001. This subclass is substantially the same in scope as ECLA classification H01L23/00M.

E25.001 ASSEMBLIES CONSISTING OF PLURALITY OF INDIVIDUAL SEMICONDUCTOR OR OTHER SOLID-STATE DEVICES (EPO):
This main group provides for housing or mounting arrangements of a plurality of discrete semiconductor or other solid state devices, e.g., side-by-side and/or stacked arrangement of devices such as solar cells and diodes. This subclass is substantially the same in scope as ECLA classification H01L25/00.

SEE OR SEARCH THIS CLASS, SUBCLASS:
E23.031 through E23.059, for assembly including lead frames interconnection.
E27.001, for devices consisting of a plurality of solid state components formed in or on a common substrate.

E25.002 All devices being of same type, e.g., assemblies of rectifier diodes (EPO):
This subclass is indented under subclass E25.001. This subclass is substantially the same in scope as ECLA classification H01L25/03.

(1) Note. This subclass includes assembly of all the devices being of a type provided for in the same main groups of E27.001, E29.001, E31.001, E33.001, E39.001, E43.001, E45.001, E47.001, and E49.001.

E25.003 Devices not having separate containers (EPO):
This subclass is indented under subclass E25.002. This subclass is substantially the same in scope as ECLA classification H01L25/04.

E25.004 Devices responsive or sensitive to electromagnetic radiation, e.g., infrared radiation, adapted for conversion of radiation into electrical energy or for control of electrical energy by such radiation (EPO):
This subclass is indented under subclass E25.003. This subclass is substantially the same in scope as ECLA classification H01L25/04C.

E25.005 Devices being arranged next to each other (EPO):
This subclass is indented under subclass E25.004. This subclass is substantially the same in scope as ECLA classification H01L25/04C2.

E25.006 Stacked arrangements of devices (EPO):
This subclass is indented under subclass E25.004. This subclass is substantially the same in scope as ECLA classification H01L25/04C4.

E25.007 Devices being solar cells (EPO):
This subclass is indented under subclass E25.006. This subclass is substantially the same in scope as ECLA classification H01L25/04C4C.

E25.008 Organic solid-state devices (EPO):
This subclass is indented under subclass E25.003. This subclass is substantially the same in scope as ECLA classification H01L25/04E.

E25.009 Devices responsive or sensitive to electromagnetic radiation, e.g., infrared radiation, adapted for conversion of radiation into electrical energy or for control of electrical energy by such radiation, e.g., photovoltaic modules based on organic solar cells (EPO):
This subclass is indented under subclass E25.008. This subclass is substantially the same in scope as ECLA classification H01L25/04E2.

E25.01 Device consisting of plurality of semiconductor or other solid state devices or components formed in or on common substrate, e.g., integrated circuit device (EPO):
This subclass is indented under subclass E25.003. This subclass is substantially the same in scope as ECLA classification H01L25/065.

E25.011 Devices being arranged next and on each other, i.e., mixed assemblies (EPO):
This subclass is indented under subclass E25.01. This subclass is substantially the same in scope as ECLA classification H01L25/065M.

E25.012 Devices being arranged next to each other (EPO):
This subclass is indented under subclass E25.01. This subclass is substantially the same in scope as ECLA classification H01L25/065N.

E25.013 Stacked arrangements of devices (EPO):
This subclass is indented under subclass E25.01. This subclass is substantially the same in scope as ECLA classification H01L25/065S.

E25.014 Semiconductor devices adapted for rectifying, amplifying, oscillating, or switching, capacitors, or resistors with at least one potential-jump barrier or surface barrier (EPO):
This subclass is indented under subclass E25.003. This subclass is substantially the same in scope as ECLA classification H01L25/07.

E25.015 Devices being arranged next and on each other, i.e., mixed assemblies (EPO):
This subclass is indented under subclass E25.014. This subclass is substantially the same in scope as ECLA classification H01L25/07M.

E25.016 Devices being arranged next to each other (EPO):
This subclass is indented under subclass E25.014. This subclass is substantially the same in scope as ECLA classification H01L25/07N.

E25.017 Apertured devices mounted on one or more rods passed through apertures (EPO):
This subclass is indented under subclass E25.014. This subclass is substantially the same in scope as ECLA classification H01L25/07R.

E25.018 Stacked arrangements of nonapertured devices (EPO):
This subclass is indented under subclass E25.014. This subclass is substantially the same in scope as ECLA classification H01L25/07S.

E25.019 Incoherent light-emitting semiconductor devices having potential or surface barrier (EPO):
This subclass is indented under subclass E25.003. This subclass is substantially the same in scope as ECLA classification H01L25/075.

E25.02 Devices being arranged next to each other (EPO):
This subclass is indented under subclass E25.019. This subclass is substantially the same in scope as ECLA classification H01L25/075N.

E25.021 Stacked arrangements of devices (EPO):
This subclass is indented under subclass E25.019. This subclass is substantially the same in scope as ECLA classification H01L25/075S.

E25.022 Devices having separate containers (EPO):
This subclass is indented under subclass E25.002. This subclass is substantially the same in scope as ECLA classification H01L25/10.

E25.023 Device consisting of plurality of semiconductor or other solid-state devices or components formed in or on common substrate, e.g., integrated circuit device (EPO):
This subclass is indented under subclass E25.022. This subclass is substantially the same in scope as ECLA classification H01L25/10J.

E25.024 Semiconductors devices adapted for rectifying, amplifying, oscillating, or switching, capacitors, or resistors with at least one potential-jump barrier or surface barrier (EPO):
This subclass is indented under subclass E25.022. This subclass is substantially the same in scope as ECLA classification H01L25/11.

E25.025 Mixed assemblies (EPO):
This subclass is indented under subclass E25.024. This subclass is substantially the same in scope as ECLA classification H01L25/11M.

E25.026 Devices being arranged next to each other (EPO):
This subclass is indented under subclass E25.024. This subclass is substantially the same in scope as ECLA classification H01L25/11N.

E25.027 Stacked arrangements of devices (EPO):
This subclass is indented under subclass E25.024. This subclass is substantially the same in scope as ECLA classification H01L25/11S.

E25.028 Incoherent light-emitting semiconductor devices having potential or surface barrier (EPO):
This subclass is indented under subclass E25.022. This subclass is substantially the same in scope as ECLA classification H01L25/13.

E25.029 Devices being of two or more types, e.g., forming hybrid circuits (EPO):
This subclass is indented under subclass E25.001. This subclass is substantially the same in scope as ECLA classification H01L25/16.

(1) Note. This subclass includes assembly of the devices being of types provided for in two or more different main groups of E27.001, E29.001, E31.001, E33.001, E39.001, E43.001, E45.001, E47.001, and E49.001.

E25.03 Devices being mounted on two or more different substrates (EPO):
This subclass is indented under subclass E25.029. This subclass is substantially the same in scope as ECLA classification H01L25/16F.

E25.031 Containers (EPO):
This subclass is indented under subclass E25.029. This subclass is substantially the same in scope as ECLA classification H01L25/16H.

E25.032 Comprising optoelectronic devices, e.g., LED, photodiodes (EPO):
This subclass is indented under subclass E25.029. This subclass is substantially the same in scope as ECLA classification H01L25/16L.

E27.001 DEVICE CONSISTING OF A PLURALITY OF SEMICONDUCTOR OR OTHER SOLID STATE COMPONENTS FORMED IN OR ON A COMMON SUBSTRATE, E.G., INTEGRATED CIRCUIT DEVICE (EPO):
This main group provides for device which includes a plurality of semiconductor or other solid state components with specific structural features related to the device, material, or layout, and integrated on a common substrate. This subclass is substantially the same in scope as ECLA classification H01L27/00.

(1) Note. See E21.001, E31.001, E33.001, E39.001, E45.001, E47.001, E49.001, and E51.001 for processes or apparatus adapted for manufacture or treatment of semiconductor or solid state devices or of parts thereof.

E27.002 Including bulk negative resistance effect component (EPO):
This subclass is indented under subclass E27.001. This subclass is substantially the same in scope as ECLA classification H01L27/26.

E27.003 Including Gunn-effect device (EPO):
This subclass is indented under subclass E27.002. This subclass is substantially the same in scope as ECLA classification H01L27/26B.

E27.004 Including solid state component for rectifying, amplifying, or switching without a potential barrier or surface barrier (EPO):
This subclass is indented under subclass E27.001. This subclass is substantially the same in scope as ECLA classification H01L27/24.

E27.005 Including component using galvano-magnetic effects, e.g. Hall effect (EPO):
This subclass is indented under subclass E27.001. This subclass is substantially the same in scope as ECLA classification H01L27/22.

E27.006 Including piezo-electric, electro-resistive, or magneto-resistive component (EPO):
This subclass is indented under subclass E27.001. This subclass is substantially the same in scope as ECLA classification H01L27/20.

E27.007 Including superconducting component (EPO):
This subclass is indented under subclass E27.001. This subclass is substantially the same in scope as ECLA classification H01L27/18.

E27.008 Including thermo-electric or thermo-magnetic component with or without a junction of dissimilar material or thermo-magnetic component (EPO):
This subclass is indented under subclass E27.001. This subclass is substantially the same in scope as ECLA classification H01L27/16.

E27.009 Including semiconductor component with at least one potential barrier or surface barrier adapted for rectifying, oscillating, amplifying, or switching, or Including integrated passive circuit elements (EPO):
This subclass is indented under subclass E27.001. This subclass is substantially the same in scope as ECLA classification H01L27/02.

E27.01 With semiconductor substrate only (EPO):
This subclass is indented under subclass E27.009. This subclass is substantially the same in scope as ECLA classification H01L27/04.

SEE OR SEARCH THIS CLASS, SUBCLASS:
E27.111, for substrate comprising other than a semiconductor material

E27.112, for substrate including insulator on semiconductor or vise versa, e.g., silicon on insulator (SOI)

E27.011 Including a plurality of components in a non-repetitive configuration (EPO):
This subclass is indented under subclass E27.01. This subclass is substantially the same in scope as ECLA classification H01L27/06.

E27.012 Made of compound semiconductor material, e.g. III-V material (EPO):
This subclass is indented under subclass E27.011. This subclass is substantially the same in scope as ECLA classification H01L27/06C.

E27.013 Integrated circuit having a two-dimensional layout of components without a common active region (EPO):
This subclass is indented under subclass E27.011. This subclass is substantially the same in scope as ECLA classification H01L27/06D.

E27.014 Including a field-effect type component (EPO):
This subclass is indented under subclass E27.013. This subclass is substantially the same in scope as ECLA classification H01L27/06D4.

E27.015 In combination with bipolar transistor (EPO):
This subclass is indented under subclass E27.014. This subclass is substantially the same in scope as ECLA classification H01L27/06D4T.

E27.016 In combination with diode, resistor, or capacitor (EPO):
This subclass is indented under subclass E27.014. This subclass is substantially the same in scope as ECLA classification H01L27/06D4V.

E27.017 In combination with bipolar transistor and diode, resistor, or capacitor (EPO):
This subclass is indented under subclass E27.014. This subclass is substantially the same in scope as ECLA classification H01L27/06D4W.

E27.018 With component other than field-effect type (EPO):
This subclass is indented under subclass E27.013. This subclass is substantially the same in scope as ECLA classification H01L27/06D6.

E27.019 Bipolar transistor in combination with diode, capacitor, or resistor (EPO):
This subclass is indented under subclass E27.018. This subclass is substantially the same in scope as ECLA classification H01L27/06D6T.

E27.02 Vertical bipolar transistor in combination with diode, capacitor, or resistor (EPO):
This subclass is indented under subclass E27.019. This subclass is substantially the same in scope as ECLA classification H01L27/06D6T2.

E27.021 Vertical bipolar transistor in combination with resistor or capacitor only (EPO):
This subclass is indented under subclass E27.02. This subclass is substantially the same in scope as ECLA classification H01L27/06D6T2B.

E27.022 Vertical bipolar transistor in combination with diode only (EPO):
This subclass is indented under subclass E27.02. This subclass is substantially the same in scope as ECLA classification H01L27/06D6T2D.

E27.023 Lateral bipolar transistor in combination with diode, capacitor, or resistor (EPO):
This subclass is indented under subclass E27.019. This subclass is substantially the same in scope as ECLA classification H01L27/06D6T4.

E27.024 Including combination of diode, capacitor, or resistor (EPO):
This subclass is indented under subclass E27.018. This subclass is substantially the same in scope as ECLA classification H01L27/06D6V.

E27.025 Including combination of capacitor or resistor only (EPO):
This subclass is indented under subclass E27.024. This subclass is substantially the

same in scope as ECLA classification H01L27/06D6V2.

E27.026 Integrated circuit having a three-dimensional layout (EPO):
This subclass is indented under subclass E27.011. This subclass is substantially the same in scope as ECLA classification H01L27/06E.

E27.027 Including components formed on opposite sides of a semiconductor substrate (EPO):
This subclass is indented under subclass E27.026. This subclass is substantially the same in scope as ECLA classification H01L27/600.

E27.028 Including component having an active region in common (EPO):
This subclass is indented under subclass E27.011. This subclass is substantially the same in scope as ECLA classification H01L27/07.

E27.029 Including component of the field-effect type (EPO):
This subclass is indented under subclass E27.028. This subclass is substantially the same in scope as ECLA classification H01L27/07F.

SEE OR SEARCH THIS CLASS, SUBCLASS:

E27.059, for integrated circuit device containing field effect components of single kind only.

E27.081, for integrated circuit device including of plurality of field effect components in a repetitive configuration.

E27.107, for masterslice integrated circuit using field effect structure.

E27.148, for Junction field effect transistor imager.

E29.242, for electrodes controlled by field effect transistor.

E27.03 In combination with bipolar transistor and diode, capacitor, or resistor (EPO):
This subclass is indented under subclass E27.029. This subclass is substantially the same in scope as ECLA classification H01L27/07F2.

E27.031 In combination with vertical bipolar transistor and diode, capacitor, or resistor (EPO):
This subclass is indented under subclass E27.03. This subclass is substantially the same in scope as ECLA classification H01L27/07F2B.

E27.032 In combination with lateral bipolar transistor and diode, capacitor, or resistor (EPO):
This subclass is indented under subclass E27.03. This subclass is substantially the same in scope as ECLA classification H01L27/07F2L.

E27.033 In combination with diode, capacitor, or resistor (EPO):
This subclass is indented under subclass E27.029. This subclass is substantially the same in scope as ECLA classification H01L27/07F4.

E27.034 In combination with capacitor only (EPO):
This subclass is indented under subclass E27.033. This subclass is substantially the same in scope as ECLA classification H01L27/07F4C.

E27.035 In combination with resistor only (EPO):
This subclass is indented under subclass E27.033. This subclass is substantially the same in scope as ECLA classification H01L27/07F4R.

E27.036 With component other than field-effect type (EPO):
This subclass is indented under subclass E27.028. This subclass is substantially the same in scope as ECLA classification H01L27/07T.

E27.037 Bipolar transistor in combination with diode, capacitor, or resistor (EPO):
This subclass is indented under subclass E27.036. This subclass is substantially the same in scope as ECLA classification H01L27/07T2.

E27.038 Vertical bipolar transistor in combination with diode, capacitor, or resistor (EPO):
This subclass is indented under subclass E27.037. This subclass is substantially the same in scope as ECLA classification H01L27/07T2C.

E27.039 Vertical bipolar transistor in combination with diode only (EPO):
This subclass is indented under subclass E27.038. This subclass is substantially the same in scope as ECLA classification H01L27/07T2C2.

E27.04 With Schottky diode only (EPO):
This subclass is indented under subclass E27.039. This subclass is substantially the same in scope as ECLA classification H01L27/07T2C2S.

E27.041 Vertical bipolar transistor in combination with resistor only (EPO):
This subclass is indented under subclass E27.038. This subclass is substantially the same in scope as ECLA classification H01L27/07T2C4.

E27.042 Vertical bipolar transistor in combination with capacitor only (EPO):
This subclass is indented under subclass E27.038. This subclass is substantially the same in scope as ECLA classification H01L27/07T2C6.

E27.043 Lateral bipolar transistor in combination with diode, capacitor, or resistor (EPO):
This subclass is indented under subclass E27.037. This subclass is substantially the same in scope as ECLA classification H01L27/07T2L.

E27.044 Including combination of diode, capacitor, or resistor (EPO):
This subclass is indented under subclass E27.036. This subclass is substantially the same in scope as ECLA classification H01L27/07T5.

E27.045 Combination of capacitor and resistor (EPO):
This subclass is indented under subclass E27.044. This subclass is substantially the same in scope as ECLA classification H01L27/07T5C.

E27.046 Including only semiconductor components of a single kind, e.g., all bipolar transistors, all diodes, or all CMOS (EPO):
This subclass is indented under subclass E27.01. This subclass is substantially the same in scope as ECLA classification H01L27/08.

E27.047 Resistor only (EPO):
This subclass is indented under subclass E27.046. This subclass is substantially the same in scope as ECLA classification H01L27/08B.

E27.048 Capacitor only (EPO):
This subclass is indented under subclass E27.046. This subclass is substantially the same in scope as ECLA classification H01L27/08C.

E27.049 Varactor diode (EPO):
This subclass is indented under subclass E27.048. This subclass is substantially the same in scope as ECLA classification H01L27/08C2.

E27.05 Metal-insulated-semiconductor (MIS) diode (EPO):
This subclass is indented under subclass E27.048. This subclass is substantially the same in scope as ECLA classification H01L27/08C3.

E27.051 Diode only (EPO):
This subclass is indented under subclass E27.046. This subclass is substantially the same in scope as ECLA classification H01L27/08D.

E27.052 Thyristor only (EPO):
This subclass is indented under subclass E27.046. This subclass is substantially the same in scope as ECLA classification H01L27/08U.

E27.053 Bipolar component only (EPO):
This subclass is indented under subclass E27.046. This subclass is substantially the same in scope as ECLA classification H01L27/082.

E27.054 Combination of lateral and vertical transistors only (EPO):
This subclass is indented under subclass E27.053. This subclass is substantially the same in scope as ECLA classification H01L27/082L.

E27.055 Vertical bipolar transistor only (EPO):
This subclass is indented under subclass E27.053. This subclass is substantially the same in scope as ECLA classification H01L27/082V.

E27.056 Vertical direct transistor of the same conductivity type having different characteristics, (e.g. Darlington transistor) (EPO):
This subclass is indented under subclass E27.055. This subclass is substantially the same in scope as ECLA classification H01L27/082V2.

E27.057 Vertical complementary transistor (EPO):
This subclass is indented under subclass E27.055. This subclass is substantially the same in scope as ECLA classification H01L27/082V4.

E27.058 Combination of direct and inverse vertical transistors (e.g., collector acts as emitter) (EPO):
This subclass is indented under subclass E27.055. This subclass is substantially the same in scope as ECLA classification H01L27/082V6.

E27.059 Including field-effect component only (EPO):
This subclass is indented under subclass E27.046. This subclass is substantially the same in scope as ECLA classification H01L27/085.

E27.06 Field-effect transistor with insulated gate (EPO):
This subclass is indented under subclass E27.059. This subclass is substantially the same in scope as ECLA classification H01L27/088.

E27.061 Combination of depletion and enhancement field-effect transistors (EPO):
This subclass is indented under subclass E27.06. This subclass is substantially the same in scope as ECLA classification H01L27/088D.

E27.062 Complementary MIS (EPO):
This subclass is indented under subclass E27.06. This subclass is substantially the same in scope as ECLA classification H01L27/092.

E27.063 Means for preventing a parasitic bipolar action between the different transistor regions, e.g. latch-up prevention (EPO):
This subclass is indented under subclass E27.062. This subclass is substantially the same in scope as ECLA classification H01L27/092B.

E27.064 Combination of complementary transistors having a different structure, e.g. stacked CMOS, high-voltage and low-voltage CMOS (EPO):
This subclass is indented under subclass E27.062. This subclass is substantially the same in scope as ECLA classification H01L27/092D.

E27.065 Including an N-well only in the substrate (EPO):
This subclass is indented under subclass E27.062. This subclass is substantially the same in scope as ECLA classification H01L27/092N.

E27.066 Including a P-well only in the substrate (EPO):
This subclass is indented under subclass E27.062. This subclass is substantially the same in scope as ECLA classification H01L27/092P.

E27.067 Including both N- and P-wells in the substrate, e.g. twin-tub (EPO):
This subclass is indented under subclass E27.062. This subclass is substantially the same in scope as ECLA classification H01L27/092T.

E27.068 Schottky barrier gate field-effect transistor (EPO):
This subclass is indented under subclass E27.059. This subclass is substantially the same in scope as ECLA classification H01L27/095.

E27.069 PN junction gate field-effect transistor (EPO):
This subclass is indented under subclass E27.059. This subclass is substantially the same in scope as ECLA classification H01L27/098.

E27.07 Including a plurality of individual components in a repetitive configuration (EPO):
This subclass is indented under subclass E27.01. This subclass is substantially the same in scope as ECLA classification H01L27/10.

E27.071 Including resistor or capacitor only (EPO):
This subclass is indented under subclass E27.07. This subclass is substantially the same in scope as ECLA classification H01L27/10C.

E27.072 Including bipolar component (EPO):
This subclass is indented under subclass E27.07. This subclass is substantially the same in scope as ECLA classification H01L27/102.

E27.073 Including diode only (EPO):
This subclass is indented under subclass E27.072. This subclass is substantially the same in scope as ECLA classification H01L27/102D.

E27.074 Including bipolar transistor (EPO):
This subclass is indented under subclass E27.072. This subclass is substantially the same in scope as ECLA classification H01L27/102T.

E27.075 Bipolar dynamic random access memory structure (EPO):
This subclass is indented under subclass E27.074. This subclass is substantially the same in scope as ECLA classification H01L27/102T2.

E27.076 Array of single bipolar transistors only, e.g. read only memory structure (EPO):
This subclass is indented under subclass E27.074. This subclass is substantially the same in scope as ECLA classification H01L27/102T4.

E27.077 Static bipolar memory cell structure (EPO):
This subclass is indented under subclass E27.074. This subclass is substantially the same in scope as ECLA classification H01L27/102T5.

E27.078 Bipolar electrically programmable memory structure (EPO):
This subclass is indented under subclass E27.074. This subclass is substantially the same in scope as ECLA classification H01L27/102T6.

E27.079 Thyristor (EPO):
This subclass is indented under subclass E27.072. This subclass is substantially the same in scope as ECLA classification H01L27/102U.

E27.08 Unijunction transistor, i.e., three terminal device with only one p-n junction having a negative resistance region in the I-V characteristic (EPO):
This subclass is indented under subclass E27.072. This subclass is substantially the same in scope as ECLA classification H01L27/102V.

E27.081 Including field-effect component (EPO):
This subclass is indented under subclass E27.07. This subclass is substantially the same in scope as ECLA classification H01L27/105.

E27.082 Including bucket brigade type charge coupled device (C.C.D) (EPO):
This subclass is indented under subclass E27.0081. This subclass is substantially the same in scope as ECLA classification H01L27/105B.

E27.083 Including charge coupled device (C.C.D) or charge injection device (C.I.D) (EPO):
This subclass is indented under subclass E27.0081. This subclass is substantially the same in scope as ECLA classification H01L27/105C.

SEE OR SEARCH THIS CLASS, SUBCLASS:
E27.15, for charge coupled imager.
E27.153,for linear CCD imager.
E27.154,for area CCD imager.
E27.159,for CCD color imager.
E27.16, for infrared CCD imager.
E29.227,for electrodes controlled by CCD.

E27.084 Dynamic random access memory, DRAM, structure (EPO):
This subclass is indented under subclass E27.0081. This subclass is substantially the same in scope as ECLA classification H01L27/108.

E27.085 One-transistor memory cell structure, i.e., each memory cell containing only one transistor (EPO):
This subclass is indented under subclass E27.0084. This subclass is substantially the same in scope as ECLA classification H01L27/108F.

E27.086 Storage electrode stacked over the transistor:
This subclass is indented under subclass E27.078. This subclass is substantially the same in scope as ECLA classification H01L27/108F2.

E27.087 With bit line higher than capacitor (EPO):
This subclass is indented under subclass E27.086. This subclass is substantially the same in scope as ECLA classification H01L27/108F2B.

E27.088 With capacitor higher than bit line level (EPO):
This subclass is indented under subclass E27.086. This subclass is substantially the same in scope as ECLA classification H01L27/108F2C.

E27.089 Storage electrode having multiple wings (EPO):
This subclass is indented under subclass E27.086. This subclass is substantially the same in scope as ECLA classification H01L27/108F2M.

E27.09 Capacitor extending under the transistor (EPO):
This subclass is indented under subclass E27.078. This subclass is substantially the same in scope as ECLA classification H01L27/108F4.

E27.091 Transistor in trench (EPO):
This subclass is indented under subclass E27.078. This subclass is substantially the same in scope as ECLA classification H01L27/108F6.

E27.092 Capacitor in trench (EPO):
This subclass is indented under subclass E27.078. This subclass is substantially the same in scope as ECLA classification H01L27/108F8.

E27.093 Capacitor extending under or around the transistor (EPO):
This subclass is indented under subclass E27.092. This subclass is substantially the same in scope as ECLA classification H01L27/108F8E.

E27.094 Having storage electrode extension stacked over the transistor (EPO):
This subclass is indented under subclass E27.092. This subclass is substantially the same in scope as ECLA classification H01L27/108F8S.

E27.095 Capacitor and transistor in common trench (EPO):
This subclass is indented under subclass E27.078. This subclass is substantially the same in scope as ECLA classification H01L27/108F10.

E27.096 Vertical transistor (EPO):
This subclass is indented under subclass E27.095. This subclass is substantially the same in scope as ECLA classification H01L27/108F10V.

E27.097 Peripheral structure (EPO):
This subclass is indented under subclass E27.083. This subclass is substantially the same in scope as ECLA classification H01L27/108P.

E27.098 Static random access memory, SRAM, structure (EPO):
This subclass is indented under subclass E27.081. This subclass is substantially the same in scope as ECLA classification H01L27/11.

E27.099 Load element being a MOSFET transistor (EPO):
OLE_LINK1This subclass is indented under subclass E27.098. This subclass is substan-

tially the same in scope as ECLA classification OLE_LINK1 H01L27/11F.

E27.1 Load element being a thin film transistor (EPO):
This subclass is indented under subclass E27.099. This subclass is substantially the same in scope as ECLA classification H01L27/11F2.

E27.101 Load element being a resistor (EPO):
This subclass is indented under subclass E27.098. This subclass is substantially the same in scope as ECLA classification H01L27/11R.

E27.102 Read-only memory, ROM, structure (EPO):
This subclass is indented under subclass E27.081. This subclass is substantially the same in scope as ECLA classification H01L27/112.

E27.103 Electrically programmable ROM (EPO):
This subclass is indented under subclass E27.102. This subclass is substantially the same in scope as ECLA classification H01L27/115.

E27.104 Ferroelectric non-volatile memory structure (EPO):
This subclass is indented under subclass E27.103. This subclass is substantially the same in scope as ECLA classification H01L27/115F.

E27.105 Masterslice integrated circuit (EPO):
This subclass is indented under subclass E27.07. This subclass is substantially the same in scope as ECLA classification H01L27/118.

(1) Note: Masterslice integrated circuit is a gate array wherein the circuit elements can be interconnected by more than one wirings pattern to have different designed devices.

E27.106 Using bipolar structure (EPO):
This subclass is indented under subclass E27.105. This subclass is substantially the same in scope as ECLA classification H01L27/118B.

E27.107 Using field-effect structure (EPO):
This subclass is indented under subclass E27.105. This subclass is substantially the same in scope as ECLA classification H01L27/118G.

E27.108 CMOS gate array (EPO):
This subclass is indented under subclass E27.107. This subclass is substantially the same in scope as ECLA classification H01L27/118G4.

E27.109 Using combined field-effect/bipolar structure (EPO):
This subclass is indented under subclass E27.105. This subclass is substantially the same in scope as ECLA classification H01L27/118M.

E27.11 Input and output buffer/driver (EPO):
This subclass is indented under subclass E27.105. This subclass is substantially the same in scope as ECLA classification H01L27/118P.

E27.111 Substrate comprising other than a semiconductor material, e.g. insulating substrate or layered substrate Including a non-semiconductor layer (EPO):
This subclass is indented under subclass E27.009. This subclass is substantially the same in scope as ECLA classification H01L27/12.

E27.112 Including insulator on semiconductor, e.g. SOI (silicon on insulator) (EPO):
This subclass is indented under subclass E27.111. This subclass is substantially the same in scope as ECLA classification H01L27/12B.

E27.113 Combined with thin-film or thick-film passive component (EPO):
This subclass is indented under subclass E27.111. This subclass is substantially the same in scope as ECLA classification H01L27/13.

E27.114 Including only passive thin-film or thick-film elements on a common insulating substrate (EPO):
This subclass is indented under subclass E27.001. This subclass is substantially the

same in scope as ECLA classification H01L27/01.

E27.115 Thick-film circuits (EPO):
This subclass is indented under subclass E27.114. This subclass is substantially the same in scope as ECLA classification H01L27/01B.

E27.116 Thin-film circuits (EPO):
This subclass is indented under subclass E27.114. This subclass is substantially the same in scope as ECLA classification H01L27/01C.

E27.117 Including organic material in active region:
This subclass is indented under subclass E27.001. This subclass is substantially the same in scope as ECLA classification H01L27/00C.

E27.118 Including semiconductor components sensitive to infrared radiation, light, or electromagnetic radiation of a shorter wavelength (EPO):
This subclass is indented under subclass E27.117. This subclass is substantially the same in scope as ECLA classification H01L27/00C10.

E27.119 Including semiconductor components with at least one potential barrier, surface barrier, or recombination zone adapted for light emission (EPO):
This subclass is indented under subclass E27.117. This subclass is substantially the same in scope as ECLA classification H01L27/00C20.

E27.12 Including semiconductor component with at least one potential barrier or surface barrier adapted for light emission structurally associated with controlling devices having a variable impedance and not being light sensitive (EPO):
This subclass is indented under subclass E27.001. This subclass is substantially the same in scope as ECLA classification H01L27/15.

E27.121 In a repetitive configuration (EPO):
This subclass is indented under subclass E27.12. This subclass is substantially the same in scope as ECLA classification H01L27/15B.

E27.122 Including active semiconductor component sensitive to infrared radiation, light, or electromagnetic radiation of a shorter wavelength (EPO):
This subclass is indented under subclass E27.001. This subclass is substantially the same in scope as ECLA classification H01L27/14.

E27.123 Energy conversion device (EPO):
This subclass is indented under subclass E27.123. This subclass is substantially the same in scope as ECLA classification H01L27/142.

E27.124 In a repetitive configuration, e.g. planar multi-junction solar cells (EPO):
This subclass is indented under subclass E27.123. This subclass is substantially the same in scope as ECLA classification H01L27/142R.

E27.125 Including only thin film solar cells deposited on a substrate (EPO):
This subclass is indented under subclass E27.124. This subclass is substantially the same in scope as ECLA classification H01L27/142R2.

E27.126 Including multiple vertical junction or V-groove junction solar cells formed in a semiconductor substrate (EPO):
This subclass is indented under subclass E27.124. This subclass is substantially the same in scope as ECLA classification H01L27/142R3.

E27.127 Device controlled by radiation (EPO):
This subclass is indented under subclass E27.122. This subclass is substantially the same in scope as ECLA classification H01L27/144.

E27.128 With at least one potential barrier or surface barrier (EPO):
This subclass is indented under subclass E27.127. This subclass is substantially the same in scope as ECLA classification H01L27/144B.

E27.129 In a repetitive configuration (EPO):
This subclass is indented under subclass E27.128. This subclass is substantially the

same in scope as ECLA classification H01L27/144R.

E27.13 Imager Including structural or functional details of the device (EPO):
This subclass is indented under subclass E27.127. This subclass is substantially the same in scope as ECLA classification H01L27/146.

E27.131 Geometry or disposition of pixel-elements, address-lines, or gate-electrodes (EPO):
This subclass is indented under subclass E27.13. This subclass is substantially the same in scope as ECLA classification H01L27/146A2.

E27.132 Pixel-elements with integrated switching, control, storage, or amplification elements (EPO):
This subclass is indented under subclass E27.13. This subclass is substantially the same in scope as ECLA classification H01L27/146A4.

E27.133 Photodiode array or MOS imager (EPO):
This subclass is indented under subclass E27.13. This subclass is substantially the same in scope as ECLA classification H01L27/146F.

E27.134 Color imager (EPO):
This subclass is indented under subclass E27.133. This subclass is substantially the same in scope as ECLA classification H01L27/146F2.

E27.135 Multicolor imager having a stacked pixel-element structure, e.g. npn, npnpn or MQW elements (EPO):
This subclass is indented under subclass E27.134. This subclass is substantially the same in scope as ECLA classification H01L27/146F2M.

E27.136 Infrared imager (EPO):
This subclass is indented under subclass E27.133. This subclass is substantially the same in scope as ECLA classification H01L27/146F3.

E27.137 Of the hybrid type (e.g., chip-on-chip, bonded substrates) (EPO):
This subclass is indented under subclass E27.136. This subclass is substantially the same in scope as ECLA classification H01L27/146F3H.

E27.138 Multispectral infrared imager having a stacked pixel-element structure, e.g., npn, npnpn or MQW structures (EPO):
This subclass is indented under subclass E27.136. This subclass is substantially the same in scope as ECLA classification H01L27/146F3M.

E27.139 Anti-blooming (EPO):
This subclass is indented under subclass E27.133. This subclass is substantially the same in scope as ECLA classification H01L27/146F4.

SEE OR SEARCH THIS CLASS, SUBCLASS:
E27.145, for anti-blooming in imager using a photoconductor layer
E27.162, for anti-blooming in charge coupled imager

E27.14 X-ray, gamma-ray, or high energy radiation imager (measuring X-, gamma- or corpuscular radiation) (EPO):
This subclass is indented under subclass E27.133. This subclass is substantially the same in scope as ECLA classification H01L27/146F5.

E27.141 Imager using a photoconductor layer (e.g., single photoconductor layer for all pixels) (EPO):
This subclass is indented under subclass E27.13. This subclass is substantially the same in scope as ECLA classification H01L27/146P.

E27.142 Color imager (EPO):
This subclass is indented under subclass E27.141. This subclass is substantially the same in scope as ECLA classification H01L27/146P2.

E27.143 Infrared imager (EPO):
This subclass is indented under subclass E27.141. This subclass is substantially the same in scope as ECLA classification H01L27/146P3.

E27.144 Of the hybrid type (e.g., chip-on-chip, bonded substrates) (EPO):
This subclass is indented under subclass E27.143. This subclass is substantially the same in scope as ECLA classification H01L27/146P3H.

E27.145 Anti-blooming (EPO):
This subclass is indented under subclass E27.141. This subclass is substantially the same in scope as ECLA classification H01L27/146P4.

E27.146 X-ray, gamma-ray, or high energy radiation imagers (EPO):
This subclass is indented under subclass E27.141. This subclass is substantially the same in scope as ECLA classification H01L27/146P5.

E27.147 Contact-type imager (e.g., contacts document surface) (EPO):
This subclass is indented under subclass E27.13. This subclass is substantially the same in scope as ECLA classification H01L27/146R.

E27.148 Junction field effect transistor (JFET) imager or static induction transistor (SIT) imager (EPO):
This subclass is indented under subclass E27.13. This subclass is substantially the same in scope as ECLA classification H01L27/146S.

E27.149 Bipolar transistor imager (EPO):
This subclass is indented under subclass E27.13. This subclass is substantially the same in scope as ECLA classification H01L27/146T.

E27.15 Charge coupled imager (EPO):
This subclass is indented under subclass E27.13. This subclass is substantially the same in scope as ECLA classification H01L27/148.

SEE OR SEARCH THIS CLASS, SUBCLASS:
E29.065,for individual charge coupled devices.

E27.151 Structural or functional details (EPO):
This subclass is indented under subclass E27.15. This subclass is substantially the same in scope as ECLA classification H01L27/148A.

E27.152 Geometry or disposition of pixel-elements, address lines or gate-electrodes (EPO):
This subclass is indented under subclass E27.151. This subclass is substantially the same in scope as ECLA classification H01L27/148A2.

E27.153 Linear CCD imager (EPO):
This subclass is indented under subclass E27.15. This subclass is substantially the same in scope as ECLA classification H01L27/148B.

E27.154 Area CCD imager (EPO):
This subclass is indented under subclass E27.15. This subclass is substantially the same in scope as ECLA classification H01L27/148C.

E27.155 Frame-interline transfer (EPO):
This subclass is indented under subclass E27.154. This subclass is substantially the same in scope as ECLA classification H01L27/148C2.

E27.156 Interline transfer (EPO):
This subclass is indented under subclass E27.154. This subclass is substantially the same in scope as ECLA classification H01L27/148C4.

E27.157 Frame transfer (EPO):
This subclass is indented under subclass E27.154. This subclass is substantially the same in scope as ECLA classification H01L27/148C6.

E27.158 Charge injection device (CID) imager (EPO):
This subclass is indented under subclass E27.15. This subclass is substantially the same in scope as ECLA classification H01L27/148D.

E27.159 CCD or CID color imager (EPO):
This subclass is indented under subclass E27.15. This subclass is substantially the same in scope as ECLA classification H01L27/148F.

E27.16 Infrared CCD or CID imager (EPO):
This subclass is indented under subclass E27.15. This subclass is substantially the same in scope as ECLA classification H01L27/148J.

E27.161 Of the hybrid type (e.g., chip-on-chip, bonded substrates) (EPO):
This subclass is indented under subclass E27.16. This subclass is substantially the same in scope as ECLA classification H01L27/148J2.

E27.162 Anti-blooming (EPO):
This subclass is indented under subclass E27.15. This subclass is substantially the same in scope as ECLA classification H01L27/148M.

E27.163 Including a photoconductive layer deposited on the CCD structure (EPO):
This subclass is indented under subclass E27.15. This subclass is substantially the same in scope as ECLA classification H01L27/148P.

E29.001 Semiconductors devices adapted for rectifying, amplifying, oscillating, or switching, capacitors, or resistors with at least one potential-jump barrier or surface barrier (EPO):
This main group provides for semiconductor devices which operate by the movement of charge carriers, i.e. electrons and holes, from one energy level to another within the semiconductor material and can modify an input voltage to achieve rectification, amplification, oscillation or switching action, or capacitors or resistors with at least one potential-jump barrier or surface barrier. This subclass is substantially the same in scope as ECLA classification H01L29/00.

(1) Note: See E21.001 for processes or apparatus adapted for manufacture or treatment of semiconductor or solid state devices or of parts thereof.

E29.002 Electrical characteristics due to properties of entire semiconductor body rather than just surface region (EPO):
This subclass is indented under subclass E29.001. This subclass is substantially the same in scope as ECLA classification H01L29/02.

E29.003 Characterized by their crystalline structure (e.g., polycrystalline, cubic) particular orientation of crystalline planes (EPO):
This subclass is indented under subclass E29.002. This subclass is substantially the same in scope as ECLA classification H01L29/04.

SEE OR SEARCH THIS CLASS, SUBCLASS:
E29.106, for imperfections.

E29.004 With specified crystalline planes or axis (EPO):
This subclass is indented under subclass E29.003. This subclass is substantially the same in scope as ECLA classification H01L29/04B.

E29.005 Characterized by specified shape or size of PN junction or by specified impurity concentration gradient within the device (EPO):
This subclass is indented under subclass E29.002. This subclass is substantially the same in scope as ECLA classification H01L29/06.

E29.006 Characterized by particular design considerations to control electrical field effect within device (EPO):
This subclass is indented under subclass E29.005. This subclass is substantially the same in scope as ECLA classification H01L29/06B.

SEE OR SEARCH THIS CLASS, SUBCLASS:
E29.022, for geometrical design considerations for devices

E29.007 For controlling surface leakage or electric field concentration (EPO):
This subclass is indented under subclass E29/006. This subclass is substantially the same in scope as ECLA classification H01L29/06B2.

E29.008 For controlling breakdown voltage of reverse biased devices (EPO):
This subclass is indented under subclass E29.007. This subclass is substantially the same in scope as ECLA classification H01L29/06B2B.

E29.009 With field relief electrode (field plate) (EPO):
This subclass is indented under subclass E29.008. This subclass is substantially the same in scope as ECLA classification H01L29/06B2B2.

E29.01 With at least two field relief electrodes used in combination and not electrically interconnected (EPO):
This subclass is indented under subclass E29.009. This subclass is substantially the same in scope as ECLA classification H01L29/06B2B2C.

E29.011 With one or more field relief electrode comprising resistance material (e.g., semi insulating material, lightly doped poly-silicon) (EPO):
This subclass is indented under subclass E29.01. This subclass is substantially the same in scope as ECLA classification H01L29/06B2B2C2.

E29.012 By doping profile or shape or arrangement of the PN junction, or with supplementary regions (e.g., guard ring, LDD, drift region) (EPO):
This subclass is indented under subclass E29.008. This subclass is substantially the same in scope as ECLA classification H01L29/06B2B3.

E29.013 With supplementary region doped oppositely to or in rectifying contact with semiconductor containing or contacting region(e.g., guard rings with PN or Schottky junction) (EPO):
This subclass is indented under subclass E29.012. This subclass is substantially the same in scope as ECLA classification H01L29/06B2B3B.

E29.014 With breakdown supporting region for localizing breakdown or limiting its voltage (EPO):
This subclass is indented under subclass E29.012. This subclass is substantially the same in scope as ECLA classification H01L29/06B2B3C.

E29.015 With insulating layer characterized by dielectric or electrostatic property (e.g., including fixed charge or semi-insulating surface layer) (EPO):
This subclass is indented under subclass E29.008. This subclass is substantially the same in scope as ECLA classification H01L29/06B2B4.

E29.016 For preventing surface leakage due to surface inversion layer (e.g., channel stop) (EPO):
This subclass is indented under subclass E29.007. This subclass is substantially the same in scope as ECLA classification H01L29/06B2C.

E29.017 With field relief electrodes acting on insulator potential or insulator charges (EPO):
This subclass is indented under subclass E29.016. This subclass is substantially the same in scope as ECLA classification H01L29/06B2C2.

SEE OR SEARCH THIS CLASS, SUBCLASS:
E29.015, for controlling surface effect and preventing surface correlated breakdown with plate acting on the insulator potential or the insulator charges.

E29.018 Comprising internal isolation within devices or components (EPO):
This subclass is indented under subclass E29.006. This subclass is substantially the same in scope as ECLA classification H01L29/06B3.

E29.019 Isolation by PN junctions (EPO):
This subclass is indented under subclass E29.018. This subclass is substantially the same in scope as ECLA classification H01L29/06B3B.

E29.02 Isolation by dielectric regions (EPO):
This subclass is indented under subclass E29.018. This subclass is substantially the same in scope as ECLA classification H01L29/06B3C.

E29.021 For source or drain region of field-effect device (EPO):
This subclass is indented under subclass E29.02. This subclass is substantially the same in scope as ECLA classification H01L29/06B3C2.

E29.022 Characterized by shape of semiconductor body (EPO):
This subclass is indented under subclass E29.005. This subclass is substantially the same in scope as ECLA classification H01L29/06C.

E29.023 Adapted for altering junction breakdown voltage by shape of semiconductor body (EPO):
This subclass is indented under subclass E29.022. This subclass is substantially the same in scope as ECLA classification H01L29/06C4.

E29.024 Characterized by shape, relative sizes or dispositions of semiconductor regions or junctions between regions (EPO):
This subclass is indented under subclass E29.005. This subclass is substantially the same in scope as ECLA classification H01L29/06D.

E29.025 Characterized by particular shape of junction between semiconductor regions (EPO):
This subclass is indented under subclass E29.024. This subclass is substantially the same in scope as ECLA classification H01L29/06D2.

E29.026 Surface layout of device (EPO):
This subclass is indented under subclass E29.024. This subclass is substantially the same in scope as ECLA classification H01L29/06D3.

SEE OR SEARCH THIS CLASS, SUBCLASS:
E29.066, for surface shape of the base only.

E29.027 Surface layout of MOS gated device (e.g., DMOSFET or IGBT) (EPO):
This subclass is indented under subclass E29.026. This subclass is substantially the same in scope as ECLA classification H01L29/06D3B.

E29.028 With a nonplanar gate structure (EPO):
This subclass is indented under subclass E29.027. This subclass is substantially the same in scope as ECLA classification H01L29/06D3B2.

E29.029 With semiconductor regions connected to electrode carrying current to be rectified, amplified or switched and such electrode being part of semiconductor device which comprises three or more electrodes (EPO):
This subclass is indented under subclass E29.005. This subclass is substantially the same in scope as ECLA classification H01L29/08.

E29.03 Emitter regions of bipolar transistors (EPO):
This subclass is indented under subclass E29.029. This subclass is substantially the same in scope as ECLA classification H01L29/08B.

E29.031 Of lateral transistors (EPO):
This subclass is indented under subclass E29.03. This subclass is substantially the same in scope as ECLA classification H01L29/08B2.

E29.032 Noninterconnected multiemitter structures (EPO):
This subclass is indented under subclass E29.03. This subclass is substantially the same in scope as ECLA classification H01L29/08B5.

E29.033 Of heterojunction bipolar transistors (EPO):
This subclass is indented under subclass E29.03. This subclass is substantially the same in scope as ECLA classification H01L29/08B7.

E29.034 Collector regions of bipolar transistors (EPO):
This subclass is indented under subclass E29.029. This subclass is substantially the same in scope as ECLA classification H01L29/08C.

E29.035 Pedestal collectors (EPO):
This subclass is indented under subclass E29.034. This subclass is substantially the same in scope as ECLA classification H01L29/08C2.

E29.036 Anode or cathode regions of thyristors or gated bipolar-mode devices (EPO):
This subclass is indented under subclass E29.029. This subclass is substantially the same in scope as ECLA classification H01L29/08D.

E29.037 Anode regions of thyristors or gated bipolar-mode devices (EPO):
This subclass is indented under subclass E29.036. This subclass is substantially the same in scope as ECLA classification H01L29/08D2.

E29.038 Cathode regions of thyristors (EPO):
This subclass is indented under subclass E29.036. This subclass is substantially the same in scope as ECLA classification H01L29/08D3.

E29.039 Source or drain regions of field-effect devices (EPO):
This subclass is indented under subclass E29.029. This subclass is substantially the same in scope as ECLA classification H01L29/08E.

E29.04 Of field-effect transistors with insulated gate (EPO):
This subclass is indented under subclass E29.039. This subclass is substantially the same in scope as ECLA classification H01L29/08E2.

SEE OR SEARCH THIS CLASS, SUBCLASS:
E29.062, with a passive supplementary region between source or drain and substrate related to punch-through, capacity or isolation phenomena.
E29.266, with LDD or DDD structure.
E29.277, for thin film transistors.

E29.041 Of field-effect transistors with Schottky gate (EPO):
This subclass is indented under subclass E29.039. This subclass is substantially the same in scope as ECLA classification H01L29/08E3.

E29.042 Tunneling barrier (EPO):
This subclass is indented under subclass E29.029. This subclass is substantially the same in scope as ECLA classification H01L29/08T.

E29.043 With semiconductor regions connected to electrode not carrying current to be rectified, amplified or switched and such electrode being part of semiconductor device which comprises three or more electrodes (EPO):
This subclass is indented under subclass E29.005. This subclass is substantially the same in scope as ECLA classification H01L29/10.

E29.044 Base region of bipolar transistors (EPO):
This subclass is indented under subclass E29.043. This subclass is substantially the same in scope as ECLA classification H01L29/10B.

E29.045 Of lateral transistors (EPO):
This subclass is indented under subclass E29.044. This subclass is substantially the same in scope as ECLA classification H01L29/10B2.

E29.046 Base regions of thyristors (EPO):
This subclass is indented under subclass E29.043. This subclass is substantially the same in scope as ECLA classification H01L29/10C.

E29.047 Anode base regions of thyristors (EPO):
This subclass is indented under subclass E29.046. This subclass is substantially the same in scope as ECLA classification H01L29/10C2.

E29.048 Cathode base regions of thyristors (EPO):
This subclass is indented under subclass E29.046. This subclass is substantially the same in scope as ECLA classification H01L29/10C3.

E29.049 Channel region of field-effect devices (EPO):
This subclass is indented under subclass E29.043. This subclass is substantially the same in scope as ECLA classification H01L29/10D.

E29.05 Of field-effect transistors (EPO):
This subclass is indented under subclass E29.049. This subclass is substantially the

same in scope as ECLA classification H01L29/10D2.

E29.051 With insulated gate (EPO):
This subclass is indented under subclass E29.05. This subclass is substantially the same in scope as ECLA classification H01L29//10D2B.

SEE OR SEARCH THIS CLASS, SUBCLASS:
E29.135,with channel and gate aligned in the lengthwise direction.
E29.270,with buried channel.

E29.052 Nonplanar channel (EPO):
This subclass is indented under subclass E29.051. This subclass is substantially the same in scope as ECLA classification H01L29/10D2B1.

SEE OR SEARCH THIS CLASS, SUBCLASS:
E29.130, if characterised only by the shape of a non-planar gate structure.

E29.053 With nonuniform doping structure in channel region surface (EPO):
This subclass is indented under subclass E29.051. This subclass is substantially the same in scope as ECLA classification H01L29/10D2B2.

E29.054 Doping structure being parallel to channel length (EPO):
This subclass is indented under subclass E29.053. This subclass is substantially the same in scope as ECLA classification H01L29/10D2B2B.

E29.055 With vertical doping variation (EPO):
This subclass is indented under subclass E29.051. This subclass is substantially the same in scope as ECLA classification H01L29/10D2B3.

E29.056 With variation of composition of channel (EPO):
This subclass is indented under subclass E29.051. This subclass is substantially the same in scope as ECLA classification H01L29/10D2B4.

E29.057 With PN junction gate:
This subclass is indented under subclass E29.05. This subclass is substantially the same in scope as ECLA classification H01L29/10D2C.

E29.058 Of charge coupled devices (EPO):
This subclass is indented under subclass E29.049. This subclass is substantially the same in scope as ECLA classification H01L29/10D3.

E29.059 Gate region of field-effect devices with PN junction gate (EPO):
This subclass is indented under subclass E29.043. This subclass is substantially the same in scope as ECLA classification H01L29/10E.

E29.06 Substrate region of field-effect devices (EPO):
This subclass is indented under subclass E29.043. This subclass is substantially the same in scope as ECLA classification H01L29/10F.

E29.061 Of field-effect transistors (EPO):
This subclass is indented under subclass E29.06. This subclass is substantially the same in scope as ECLA classification H01L29/10F2.

E29.062 With insulated gate (EPO):
This subclass is indented under subclass E29.061. This subclass is substantially the same in scope as ECLA classification H01L29/10F2B.

E29.063 With inactive supplementary region (e.g., for preventing punch-through, improving capacity effect or leakage current) (EPO):
This subclass is indented under subclass E29.062. This subclass is substantially the same in scope as ECLA classification H01L29/10F2B2.

E29.064 Characterized by contact structure of substrate region (EPO):
This subclass is indented under subclass E29.062. This subclass is substantially the same in scope as ECLA classification H01L29/10F2B3.

E29.065 Of charge coupled devices (EPO):
This subclass is indented under subclass E29.06. This subclass is substantially the same in scope as ECLA classification H01L29/10F3.

E29.066 Body region structure of IGFET's with channel containing layer (DMOSFET or IGBT) (EPO):
This subclass is indented under subclass E29.043. This subclass is substantially the same in scope as ECLA classification H01L29/10G.

E29.067 With nonplanar gate structure (EPO):
This subclass is indented under subclass E29.066. This subclass is substantially the same in scope as ECLA classification H01L29/10G2.

E29.068 Characterized by materials of semiconductor body (EPO):
This subclass is indented under subclass E29.002. This subclass is substantially the same in scope as ECLA classification H01L29/12.

E29.069 Single quantum well structures (EPO):
This subclass is indented under subclass E29.068. This subclass is substantially the same in scope as ECLA classification H01L29/12W.

SEE OR SEARCH THIS CLASS, SUBCLASS:
E29.081,E29.085, E29.091, E29.097, for single heterojunctions, couples of materials.

E29.07 Quantum wire structures (EPO):
This subclass is indented under subclass E29.069. This subclass is substantially the same in scope as ECLA classification H01L29/12W2.

E29.071 Quantum box or quantum dot structures (EPO):
This subclass is indented under subclass E29.069. This subclass is substantially the same in scope as ECLA classification H01L29/12W4.

E29.072 Structures with periodic or quasi-periodic potential variation, (e.g., multiple quantum wells, superlattices) (EPO):
This subclass is indented under subclass E29.068. This subclass is substantially the same in scope as ECLA classification H01L29/15.

OTHER CLASSIFICATION SYSTEMS:

ECLA G02F 1/017, for such structures applied for the control of light.
ECLA H01S 5/34, applied in semiconductor lasers.

E29.073 Doping structures (e.g., doping superlattices, nipi-superlattices) (EPO):
This subclass is indented under subclass E29.072. This subclass is substantially the same in scope as ECLA classification H01L29/15C.

SEE OR SEARCH THIS CLASS, SUBCLASS:
E29.110,for delta doping in general.

E29.074 Structures without potential periodicity in direction perpendicular to major surface of substrate (e.g., lateral superlattice) (EPO):
This subclass is indented under subclass E29.072. This subclass is substantially the same in scope as ECLA classification H01L29/15D.

E29.075 Compositional structures (EPO):
This subclass is indented under subclass E29.072. This subclass is substantially the same in scope as ECLA classification H01L29/15B.

E29.076 With layered structures with quantum effects in vertical direction (EPO):
This subclass is indented under subclass E29.075. This subclass is substantially the same in scope as ECLA classification H01L29/15B2.

E29.077 Comprising at least one long-range structurally disordered material (e.g., one-dimen-

sional vertical amorphous superlattices) (EPO):
This subclass is indented under subclass E29.076. This subclass is substantially the same in scope as ECLA classification H01L29/15B2B.

E29.078 Comprising only semiconductor materials (EPO):
This subclass is indented under subclass E 29.076. This subclass is substantially the same in scope as ECLA classification H01L29/15B2C.

E29.079 Two or more elements from two or more groups of Periodic Table of elements (e.g., alloys) (EPO):
This subclass is indented under subclass E29.068. This subclass is substantially the same in scope as ECLA classification H01L29/26.

E29.08 Amorphous materials (EPO):
This subclass is indented under subclass E29.79. This subclass is substantially the same in scope as ECLA classification H01L29/26E.

E29.081 In different semiconductor regions (e.g., heterojunctions) (EPO):
This subclass is indented under subclass E29.079. This subclass is substantially the same in scope as ECLA classification H01L29/267.

E29.082 Only element from fourth group of Periodic System in uncombined form (EPO):
This subclass is indented under subclass E29.068. This subclass is substantially the same in scope as ECLA classification H01L29/16.

SEE OR SEARCH THIS CLASS, SUBCLASS:
E29.100, if including SiC.

E29.083 Amorphous materials (EPO):
This subclass is indented under subclass E29.082. This subclass is substantially the same in scope as ECLA classification H01L29/16E.

E29.084 Including two or more of elements from fourth group of Periodic System (EPO):
This subclass is indented under subclass E29.082. This subclass is substantially the same in scope as ECLA classification H01L29/161.

E29.085 In different semiconductor regions (e.g., heterojunctions) (EPO):
This subclass is indented under subclass E29.084. This subclass is substantially the same in scope as ECLA classification H01L29/165.

E29.086 Further characterized by doping material (EPO):
This subclass is indented under subclass E29.082. This subclass is substantially the same in scope as ECLA classification H01L29/167.

E29.087 Selenium or tellurium only (EPO):
This subclass is indented under subclass E29.068. This subclass is substantially the same in scope as ECLA classification H01L29/18.

E29.088 Amorphous materials (EPO):
This subclass is indented under subclass E29.087. This subclass is substantially the same in scope as ECLA classification H01L29/18E.

E29.089 Only Group III-V compounds (EPO):
This subclass is indented under subclass E29.068. This subclass is substantially the same in scope as ECLA classification H01L29/20.

E29.09 Including two or more compounds (e.g., alloys) (EPO):
This subclass is indented under subclass E29.089. This subclass is substantially the same in scope as ECLA classification H01L29/201.

E29.091 In different semiconductor regions (e.g., heterojunctions) (EPO):
This subclass is indented under subclass E29.09. This subclass is substantially the same in scope as ECLA classification H01L29/205.

E29.092 Amorphous materials (EPO):
This subclass is indented under subclass E29.089. This subclass is substantially the same in scope as ECLA classification H01L29/20E.

E29.093 Further characterized by doping material (EPO):
This subclass is indented under subclass E29.089. This subclass is substantially the same in scope as ECLA classification H01L29/207.

E29.094 Only Group II-VI compounds (EPO):
This subclass is indented under subclass E29.068. This subclass is substantially the same in scope as ECLA classification H01L29/22.

E29.095 Amorphous materials (EPO):
This subclass is indented under subclass E29.094. This subclass is substantially the same in scope as ECLA classification H01L29/22E.

E29.096 Including two or more compounds (e.g., alloys) (EPO):
This subclass is indented under subclass E29.094. This subclass is substantially the same in scope as ECLA classification H01L29/221.

E29.097 In different semiconductor regions (e.g., heterojunctions) (EPO):
This subclass is indented under subclass E29.096. This subclass is substantially the same in scope as ECLA classification H01L29/225.

E29.098 Further characterized by doping material (EPO):
This subclass is indented under subclass E29.094. This subclass is substantially the same in scope as ECLA classification H01L29/227.

E29.099 CdX compounds being one element of sixth group of Periodic System (EPO):
This subclass is indented under subclass E29.094. This subclass is substantially the same in scope as ECLA classification H01L29/22B.

E29.1 Semiconductor materials other than Group IV, selenium, tellurium, or Group III-V compounds (EPO):
This subclass is indented under subclass E29.068. This subclass is substantially the same in scope as ECLA classification H01L29/24.

E29.101 Amorphous materials (EPO):
This subclass is indented under subclass E29.1. This subclass is substantially the same in scope as ECLA classification H01L29/24E.

E29.102 Group I-VI or I-VII compounds (e.g., Cu_2O, CuI) (EPO):
This subclass is indented under subclass E29.1. This subclass is substantially the same in scope as ECLA classification H01L29/24B.

E29.103 Pb compounds (e.g., PbO) (EPO):
This subclass is indented under subclass E29.1. This subclass is substantially the same in scope as ECLA classification H01L29/24C.

E29.104 Si compounds (e.g., SiC) (EPO):
This subclass is indented under subclass E29.1. This subclass is substantially the same in scope as ECLA classification H01L29/24D.

E29.105 Characterized by combinations of two or more features of crystalline structure, shape, materials, physical imperfections, and concentration/distribution of impurities in bulk material (EPO):
This subclass is indented under subclass E29.002. This subclass is substantially the same in scope as ECLA classification H01L29/38.

E29.106 Characterized by physical imperfections; having polished or roughened surface (EPO):
This subclass is indented under subclass E29.002. This subclass is substantially the same in scope as ECLA classification H01L29/30.

E29.107 Imperfections within semiconductor body (EPO):
This subclass is indented under subclass E29.106. This subclass is substantially the same in scope as ECLA classification H01L29/32.

E29.108 Imperfections on surface of semiconductor body (EPO):
This subclass is indented under subclass E29.106. This subclass is substantially the same in scope as ECLA classification H01L29/34.

E29.109 Characterized by concentration or distribution of impurities in bulk material (EPO):
This subclass is indented under subclass E29.002. This subclass is substantially the same in scope as ECLA classification H01L29/36.

SEE OR SEARCH THIS CLASS, SUBCLASS:
E29.005, for within semiconductor regions.

E29.11 Planar doping (e.g., atomic-plane doping, delta-doping) (EPO):
This subclass is indented under subclass E29.109. This subclass is substantially the same in scope as ECLA classification H01L29/36D.

E29.111 Electrodes (EPO):
This subclass is indented under subclass E29.001. This subclass is substantially the same in scope as ECLA classification H01L29/40.

E29.112 Characterized by their shape, relative sizes or dispositions (EPO):
This subclass is indented under subclass E29.111. This subclass is substantially the same in scope as ECLA classification H01L29/41.

E29.113 Carrying current to be rectified, amplified or switched (EPO):
This subclass is indented under subclass E29.112. This subclass is substantially the same in scope as ECLA classification H01L29/417.

E29.114 Emitter or collector electrodes for bipolar transistors (EPO):
This subclass is indented under subclass E29.113. This subclass is substantially the same in scope as ECLA classification H01L29/417B.

E29.115 Cathode or anode electrodes for thyristors (EPO):
This subclass is indented under subclass E29.113. This subclass is substantially the same in scope as ECLA classification H01L29/417C.

E29.116 Source or drain electrodes for field-effect devices (EPO):
This subclass is indented under subclass E29.113. This subclass is substantially the same in scope as ECLA classification H01L29/417D.

SEE OR SEARCH THIS CLASS, SUBCLASS:
E29.039,with monocrystalline semiconductor on source/drain region.

E29.117 For thin film transistors with insulated gate (EPO):
This subclass is indented under subclass E29.116. This subclass is substantially the same in scope as ECLA classification H01L29/417D2.

E29.118 For vertical current flow (EPO):
This subclass is indented under subclass E29.116. This subclass is substantially the same in scope as ECLA classification H01L29/417D4.

E29.119 For lateral devices where connection to source or drain region is done through at least one part of semiconductor substrate thickness (e.g., with connecting sink or with via-hole) (EPO):
This subclass is indented under subclass E29.116. This subclass is substantially the same in scope as ECLA classification H01L29/417D6.

E29.12 Layout configuration for lateral device source or drain region (e.g., cellular, interdigitated or ring structure or being curved or angular) (EPO):
This subclass is indented under subclass E29.116. This subclass is substantially the same in scope as ECLA classification H01L29/417D8.

E29.121 Source or drain electrode in groove (EPO):
This subclass is indented under subclass E29.116. This subclass is substantially the same in scope as ECLA classification H01L29/417D10.

E29.122 Characterized by relative position of source or drain electrode and gate electrode (EPO):
This subclass is indented under subclass E29.116. This subclass is substantially the same in scope as ECLA classification H01L29/417D12.

E29.123 Not carrying current to be rectified, amplified, or switched (EPO):
This subclass is indented under subclass E29.112. This subclass is substantially the same in scope as ECLA classification H01L29/423.

E29.124 Base electrodes for bipolar transistors (EPO):
This subclass is indented under subclass E29.123. This subclass is substantially the same in scope as ECLA classification H01L29/423B.

E29.125 Gate electrodes for thyristors (EPO):
This subclass is indented under subclass E29.123. This subclass is substantially the same in scope as ECLA classification H01L29/423C.

E29.126 Gate stack for field-effect devices (EPO):
This subclass is indented under subclass E29.123. This subclass is substantially the same in scope as ECLA classification H01L29/423D.

E29.127 For field-effect transistors (EPO):
This subclass is indented under subclass E29.126. This subclass is substantially the same in scope as ECLA classification H01L29/423D2.

E29.128 With insulated gate (EPO):
This subclass is indented under subclass E29.127. This subclass is substantially the same in scope as ECLA classification H01L29/423D2B.

E29.129 Gate electrodes for transistors with floating gate (EPO):
This subclass is indented under subclass E29.128. This subclass is substantially the same in scope as ECLA classification H01L29/423D2B2.

E29.13 Gate electrodes for nonplanar MOSFET (EPO):
This subclass is indented under subclass E29.128. This subclass is substantially the same in scope as ECLA classification H01L29/423D2B4.

SEE OR SEARCH THIS CLASS, SUBCLASS:
E29.267,for MOSFET's with lightly doped drain (LDD) structure.

E29.131 Having drain and source regions at different vertical level having channel composed only of vertical sidewall connecting drain and source layers (EPO):
This subclass is indented under subclass E29.13. This subclass is substantially the same in scope as ECLA classification H01L29/423D2B4B.

E29.132 Characterized by insulating layer (EPO):
This subclass is indented under subclass E29.128. This subclass is substantially the same in scope as ECLA classification H01L29/423D2B6.

E29.133 Nonuniform insulating layer thickness (EPO):
This subclass is indented under subclass E29.132. This subclass is substantially the same in scope as ECLA classification H01L29/423D2B6B.

E29.134 Characterized by configuration of gate electrode layer (EPO):
This subclass is indented under subclass E29.128. This subclass is substantially the same in scope as ECLA classification H01L29/423D2B7.

E29.135 Characterized by length or sectional shape (EPO):
This subclass is indented under subclass E29.134. This subclass is substantially the

same in scope as ECLA classification H01L29/423D2B7B.

E29.136 Characterized by surface lay-out (EPO):
This subclass is indented under subclass E29.134. This subclass is substantially the same in scope as ECLA classification H01L29/423D2B7C.

E29.137 Characterized by configuration of gate stack of thin film FETs (EPO):
This subclass is indented under subclass E29.128. This subclass is substantially the same in scope as ECLA classification H01L29/423D2B8.

E29.138 For charge coupled devices (EPO):
This subclass is indented under subclass E29.126. This subclass is substantially the same in scope as ECLA classification H01L29/423D3.

E29.139 Of specified material (EPO):
This subclass is indented under subclass E29.002. This subclass is substantially the same in scope as ECLA classification H01L29/43.

E29.14 For gate of heterojunction field-effect devices (EPO):
This subclass is indented under subclass E29.139. This subclass is substantially the same in scope as ECLA classification H01L29/43B.

E29.141 Resistive materials for field-effect devices (EPO):
This subclass is indented under subclass E29.139. This subclass is substantially the same in scope as ECLA classification H01L29/43C.

E29.142 Superconductor materials (EPO):
This subclass is indented under subclass E29.139. This subclass is substantially the same in scope as ECLA classification H01L29/43D.

E29.143 Ohmic electrodes (EPO):
This subclass is indented under subclass E29.139. This subclass is substantially the same in scope as ECLA classification H01L29/45.

E29.144 On Group III-V material (EPO):
This subclass is indented under subclass E29.143. This subclass is substantially the same in scope as ECLA classification H01L29/45B.

E29.145 On thin-film Group III-V material (EPO):
This subclass is indented under subclass E29.144. This subclass is substantially the same in scope as ECLA classification H01L29/45B2.

E29.146 On silicon (EPO):
This subclass is indented under subclass E29.143. This subclass is substantially the same in scope as ECLA classification H01L29/45S.

E29.147 For thin-film silicon (EPO):
This subclass is indented under subclass E29.146. This subclass is substantially the same in scope as ECLA classification H01L29/45S2.

E29.148 Schottky barrier electrodes (EPO):
This subclass is indented under subclass E29.139. This subclass is substantially the same in scope as ECLA classification H01L29/47.

E29.149 On Group III-V material (EPO):
This subclass is indented under subclass E29.148. This subclass is substantially the same in scope as ECLA classification H01L29/47B.

E29.15 Electrodes for IGFET (EPO):
This subclass is indented under subclass E29.139. This subclass is substantially the same in scope as ECLA classification H01L29/49.

E29.151 For TFT (EPO):
This subclass is indented under subclass E29.15. This subclass is substantially the same in scope as ECLA classification H01L29/49B.

E29.152 With lateral structure (e.g., poly-silicon gate with lateral doping variation or with lateral composition variation or characterized by

sidewalls being composed of conductive, resistivity) (EPO):
This subclass is indented under subclass E29.15. This subclass is substantially the same in scope as ECLA classification H01L29/49F.

E29.154 Silicon gate conductor material (EPO):
This subclass is indented under subclass E29.15. This subclass is substantially the same in scope as ECLA classification H01L29/49C.

E29.155 Multiple silicon layers:
This subclass is indented under subclass E29.154. This subclass is substantially the same in scope as ECLA classification H01L29/49C2

SEE OR SEARCH THIS CLASS, SUBCLASS:
E29.154,with only a vertical doping structure or vertical doping variation.

E29.156 Including silicide layer contacting silicon layer (EPO):
This subclass is indented under subclass E29.155. This subclass is substantially the same in scope as ECLA classification H01L29/49C2B.

SEE OR SEARCH THIS CLASS, SUBCLASS:
E29.157,with a barrier layer between the silicide and silicon layers.

E29.157 Including barrier layer between silicon and non-Si electrode:
This subclass is indented under subclass E29.155. This subclass is substantially the same in scope as ECLA classification H01L29/49C2C.

E29.158 Elemental metal gate conductor material (e.g., W, Mo) (EPO):
This subclass is indented under subclass E29.15. This subclass is substantially the same in scope as ECLA classification H01L29/49D.

E29.159 Diverse conductors (EPO):
This subclass is indented under subclass E29.158. This subclass is substantially the same in scope as ECLA classification H01L29/49D2.

E29.16 Gate conductor material being compound or alloy material (e.g., organic material, TiN, $MoSi_2$) (EPO):
This subclass is indented under subclass E29.15. This subclass is substantially the same in scope as ECLA classification H01L29/49E.

E29.161 Silicide (EPO):
This subclass is indented under subclass E29.16. This subclass is substantially the same in scope as ECLA classification H01L29/49E2.

E29.162 Insulating materials for IGFET (EPO):
This subclass is indented under subclass E29.15. This subclass is substantially the same in scope as ECLA classification H01L29/51.

SEE OR SEARCH THIS CLASS, SUBCLASS:
E29.151,for MIS structures on thin film semiconductor.

E29.164 With at least one ferroelectric layer (EPO):
This subclass is indented under subclass E29.162. This subclass is substantially the same in scope as ECLA classification H01L29/51F.

E29.165 Multiple layers (EPO):
This subclass is indented under subclass E29.162. This subclass is substantially the same in scope as ECLA classification H01L29/51B.

E29.166 Types of semiconductor device (EPO):
This subclass is indented under subclass E29.001. This subclass is substantially the same in scope as ECLA classification H01L29/66.

E29.167 Controllable by plural effects that include variations in magnetic field, mechanical force, or electric current/potential applied to device or one or more electrodes of device (EPO):
This subclass is indented under subclass E29.166. Subject matter wherein the performance of the device is regulated by varying the

application of two or more forces (i.e., magnetic field, mechanical force, electric current/potential to the device or one or more of its electrodes). This subclass is substantially the same in scope as ECLA classification H01L29/96.

SEE OR SEARCH THIS CLASS, SUBCLASS:
E29.169, for control by a signal.
E29.323, for control by variation in a magnetic field, per se.
E29.324, for control by variation of mechanical force, per se.
E29.325, for control by variation of electrical current/potential applied.

E29.168 Quantum effect device (EPO):
This subclass is indented under subclass E29.166. Subject matter wherein the device operation uses a quantum effect. This subclass is substantially the same in scope as ECLA classification H01L29/66Q.

(1) Note. Examples include using quantum reflection, diffraction or interference effects, (i.e., Bragg-or Aharonov-Bohm-effects).

E29.169 Controllable by only signal applied to control electrode (e.g., base of bipolar transistor, gate of field-effect transistor) (EPO):
This subclass is indented under subclass E29.166 Subject matter wherein the device operation is regulated solely by an electrical signal input to one of its control electrodes. This subclass is substantially the same in scope as ECLA classification H01L29/68.

(1) Note. Examples of control electrodes include the base of bipolar transistor, gate of field effect transistor, etc.

E29.17 Memory effect devices (EPO):
This subclass is indented under subclass E29.169. This subclass is substantially the same in scope as ECLA classification H01L29/68E.

E29.171 Bipolar device (EPO):
This subclass is indented under subclass E29.169. This subclass is substantially the same in scope as ECLA classification H01L29/70.

E29.172 Double-base diode (EPO):
This subclass is indented under subclass E29.171. This subclass is substantially the same in scope as ECLA classification H01L29/70B.

E29.173 Transistor-type device (i.e., able to continuously respond to applied control signal):
This subclass is indented under subclass E29.171. This subclass is substantially the same in scope as ECLA classification H01L29/72.

E29.174 Bipolar junction transistor:
This subclass is indented under subclass E29.173. This subclass is substantially the same in scope as ECLA classification H01L29/73.

E29.175 Structurally associated with other devices (EPO):
This subclass is indented under subclass E29.174. This subclass is substantially the same in scope as ECLA classification H01L29/73B.

SEE OR SEARCH THIS CLASS, SUBCLASS:
E29.197,IGBT.

E29.176 Device being resistive element (e.g., ballasting resistor) (EPO):
This subclass is indented under subclass E29.174. This subclass is substantially the same in scope as ECLA classification H01L29/73B2.

E29.177 Point contact transistors (EPO):
This subclass is indented under subclass E29.174. This subclass is substantially the same in scope as ECLA classification H01L29/73C.

E29.178 Schottky transistors (EPO):
This subclass is indented under subclass E29.174. This subclass is substantially the same in scope as ECLA classification H01L29/73D.

E29.179 Tunnel transistors (EPO):
This subclass is indented under subclass E29.174. This subclass is substantially the

same in scope as ECLA classification H01L29/73E.

E29.18 Avalanche transistors (EPO):
This subclass is indented under subclass E29.174. This subclass is substantially the same in scope as ECLA classification H01L29/73F.

E29.181 Transistors with hook collector (i.e., collector having two layers of opposite conductivity type (e.g., SCR)) (EPO):
This subclass is indented under subclass E29.174. This subclass is substantially the same in scope as ECLA classification H01L29/73J.

E29.182 Bipolar thin-film transistors (EPO):
This subclass is indented under subclass E29.174. This subclass is substantially the same in scope as ECLA classification H01L29/73K.

E29.183 Vertical transistor (EPO):
This subclass is indented under subclass E29.174. This subclass is substantially the same in scope as ECLA classification H01L29/732.

E29.184 Having emitter-base and base-collector junctions in same plane (EPO):
This subclass is indented under subclass E29.183. This subclass is substantially the same in scope as ECLA classification H01L29/732B.

E29.185 Having emitter-base junction and base-collector junction on different surfaces (e.g., mesa planar transistor) (EPO):
This subclass is indented under subclass E29.183. This subclass is substantially the same in scope as ECLA classification H01L29/732C.

E29.186 Inverse vertical transistor (EPO):
This subclass is indented under subclass E29.183. This subclass is substantially the same in scope as ECLA classification H01L29/732D.

E29.187 Lateral transistor (EPO):
This subclass is indented under subclass E29.174. This subclass is substantially the same in scope as ECLA classification H01L29/735.

E29.188 Hetero-junction transistor (EPO):
This subclass is indented under subclass E29.174. This subclass is substantially the same in scope as ECLA classification H01L29/737.

E29.189 Vertical transistors (EPO):
This subclass is indented under subclass E29.188. This subclass is substantially the same in scope as ECLA classification H01L29/737B.

E29.19 Having two-dimensional base (e.g., modulation-doped base, inversion layer base, delta-doped base) (EPO):
This subclass is indented under subclass E29.189. This subclass is substantially the same in scope as ECLA classification H01L29/737B2.

E29.191 Having emitter comprising one or more nonmonocrystalline elements of Group IV (e.g., amorphous silicon) alloys comprising Group IV elements (EPO):
This subclass is indented under subclass E29.189. This subclass is substantially the same in scope as ECLA classification H01L29/737B4.

E29.192 Resonant tunneling transistors (EPO):
This subclass is indented under subclass E29.189. This subclass is substantially the same in scope as ECLA classification H01L29/737B6.

E29.193 Comprising lattice mismatched active layers (e.g., SiGe strained layer transistors) (EPO):
This subclass is indented under subclass E29.189. This subclass is substantially the same in scope as ECLA classification H01L29/737B8.

E29.194 Controlled by field effect (e.g., bipolar static induction transistor (BSIT)) (EPO):
This subclass is indented under subclass E29.173. This subclass is substantially the same in scope as ECLA classification H01L29/739.

SEE OR SEARCH THIS CLASS, SUBCLASS:
E29.172, for unijunction transistors.

E29.195 Gated diode structure (EPO):
This subclass is indented under subclass E29.194. This subclass is substantially the same in scope as ECLA classification H01L29/739B.

E29.196 With PN junction gate (e.g., field-controlled thyristor (FCTh), static induction thyristor (SITh)) (EPO):
This subclass is indented under subclass E29.195. This subclass is substantially the same in scope as ECLA classification H01L29/739B2.

E29.197 Insulated gate bipolar mode transistor (e.g., IGBT; IGT; COMFET) (EPO):
This subclass is indented under subclass E29.194. This subclass is substantially the same in scope as ECLA classification H01L29/739C.

E29.198 Transistor with vertical current flow (EPO):
This subclass is indented under subclass E29.197. This subclass is substantially the same in scope as ECLA classification H01L29/739C2.

E29.199 With both emitter and collector contacts in same substrate side (EPO):
This subclass is indented under subclass E29.198. This subclass is substantially the same in scope as ECLA classification H01L29/739C2C.

E29.2 With nonplanar surface (e.g., with nonplanar gate or with trench or recess or pillar in surface of emitter, base, or collector region for improving current density or short-circuiting emitter and base regions) (EPO):
This subclass is indented under subclass E29.198. This subclass is substantially the same in scope as ECLA classification H01L29/739C2B.

E29.201 And gate structure lying on slanted or vertical surface or formed in groove (e.g., trench gate IGBT) (EPO):
This subclass is indented under subclass E29.2. This subclass is substantially the same in scope as ECLA classification H01L29/739C2B2.

E29.202 Thin-film device (EPO):
This subclass is indented under subclass E29.197. This subclass is substantially the same in scope as ECLA classification H01L29/739C1.

E29.211 Thyristor-type device (e.g., having four-zone regenerative action) (EPO):
This subclass is indented under subclass E29.171. This subclass is substantially the same in scope as ECLA classification H01L29/74.

SEE OR SEARCH THIS CLASS, SUBCLASS:
E29.337,for two-terminals thyristors.

E29.212 Gate-turn-off device (EPO):
This subclass is indented under subclass E29.211. This subclass is substantially the same in scope as ECLA classification H01L29/744.

E29.213 With turn off by field effect (EPO):
This subclass is indented under subclass E29.212. This subclass is substantially the same in scope as ECLA classification H01L29/745.

E29.214 Produced by insulated gate structure (EPO):
This subclass is indented under subclass E29.213. This subclass is substantially the same in scope as ECLA classification H01L29/745B.

E29.215 Bidirectional device (e.g., triac) (EPO):
This subclass is indented under subclass E29.211. This subclass is substantially the same in scope as ECLA classification H01L29/747.

E29.216 With turn on by field effect (EPO):
This subclass is indented under subclass E29.211. This subclass is substantially the

same in scope as ECLA classification H01L29/749.

E29.217 Combined structurally with at least one other device (EPO):
This subclass is indented under subclass E29.211. This subclass is substantially the same in scope as ECLA classification H01L29/74B.

E29.218 Combined with capacitor or resistor (EPO):
This subclass is indented under subclass E29.217. This subclass is substantially the same in scope as ECLA classification H01L29/74B2.

E29.219 Combined with diode (EPO):
This subclass is indented under subclass E29.217. This subclass is substantially the same in scope as ECLA classification H01L29/74B4.

E29.22 Antiparallel diode (EPO):
This subclass is indented under subclass E29.219. This subclass is substantially the same in scope as ECLA classification H01L29/74B4B.

SEE OR SEARCH THIS CLASS, SUBCLASS:
E29.037,for shorted anode structures enabling reverse conduction.

E29.221 Combined with field-effect transistor (EPO):
This subclass is indented under subclass E29.217. This subclass is substantially the same in scope as ECLA classification H01L29/74B6.

SEE OR SEARCH THIS CLASS, SUBCLASS:
E29.213,and E29.216, for turn-on or turn-off by field effect.

E29.222 Having built-in localized breakdown/breakover region (EPO):
This subclass is indented under subclass E29.211. This subclass is substantially the same in scope as ECLA classification H01L29/74C.

E29.223 Having amplifying gate structure (e.g., Darlington configuration) (EPO):
This subclass is indented under subclass E29.211. This subclass is substantially the same in scope as ECLA classification H01L29/74D.

E29.224 Asymmetrical thyristor (EPO):
This subclass is indented under subclass E29.211. This subclass is substantially the same in scope as ECLA classification H01L29/74E.

SEE OR SEARCH THIS CLASS, SUBCLASS:
E29.037,with a particular shorted anode structure.

E29.225 Lateral thyristor (EPO):
This subclass is indented under subclass E29.211. This subclass is substantially the same in scope as ECLA classification H01L29/74F.

E29.226 Unipolar device (EPO):
This subclass is indented under subclass E29.169. This subclass is substantially the same in scope as ECLA classification H01L29/76.

E29.227 Charge transfer device (EPO):
This subclass is indented under subclass E29.226. This subclass is substantially the same in scope as ECLA classification H01L29/762.

E29.228 Charge-coupled device (EPO):
This subclass is indented under subclass E29.227. This subclass is substantially the same in scope as ECLA classification H01L29/765.

E29.229 With field effect produced by insulated gate (EPO):
This subclass is indented under subclass E29.228. This subclass is substantially the same in scope as ECLA classification H01L29/768.

E29.23 Input structure (EPO):
This subclass is indented under subclass E29.229. This subclass is substantially the

same in scope as ECLA classification H01L29/768B.

E29.231 Output structure (EPO):
This subclass is indented under subclass E29.229. This subclass is substantially the same in scope as ECLA classification H01L29/768C.

E29.232 Structure for improving output signal (EPO):
This subclass is indented under subclass E29.229. This subclass is substantially the same in scope as ECLA classification H01L29/768D.

E29.233 Buried channel CCD (EPO):
This subclass is indented under subclass E29.229. This subclass is substantially the same in scope as ECLA classification H01L29/768E.

E29.234 Two-phase CCD (EPO):
This subclass is indented under subclass E29.233. This subclass is substantially the same in scope as ECLA classification H01L29/768E2.

E29.235 Three-phase CCD (EPO):
This subclass is indented under subclass E29.233. This subclass is substantially the same in scope as ECLA classification H01L29/768E3.

E29.236 Four-phase CCD (EPO):
This subclass is indented under subclass E29.233. This subclass is substantially the same in scope as ECLA classification H01L29/768E4.

E29.237 Surface channel CCD (EPO):
This subclass is indented under subclass E29.229. This subclass is substantially the same in scope as ECLA classification H01L29/768F.

E29.238 Two-phase CCD (EPO):
This subclass is indented under subclass E29.237. This subclass is substantially the same in scope as ECLA classification H01L29/768F2.

E29.239 Three-phase CCD (EPO):
This subclass is indented under subclass E29.237. This subclass is substantially the same in scope as ECLA classification H01L29/768F3.

E29.24 Four-phase CCD (EPO):
This subclass is indented under subclass E29.237. This subclass is substantially the same in scope as ECLA classification H01L29/768F4.

E29.241 Hot electron transistor (HET) or metal base transistor (MBT) (EPO):
This subclass is indented under subclass E29.226. This subclass is substantially the same in scope as ECLA classification H01L29/76C.

E29.242 Field-effect transistor (EPO):
This subclass is indented under subclass E29.226. This subclass is substantially the same in scope as ECLA classification H01L29/772.

E29.243 Using static field induced region (e.g., SIT, PBT) (EPO):
This subclass is indented under subclass E29.242. This subclass is substantially the same in scope as ECLA classification H01L29/772B.

E29.244 Velocity modulations transistor (i.e., VMT) (EPO):
This subclass is indented under subclass E29.242. This subclass is substantially the same in scope as ECLA classification H01L29/772D.

E29.245 With one-dimensional charge carrier gas channel (e.g., quantum wire FET) (EPO):
This subclass is indented under subclass E29.242. This subclass is substantially the same in scope as ECLA classification H01L29/775.

E29.246 With two-dimensional charge carrier gas channel (e.g., HEMT; with two-dimensional charge-carrier layer formed at heterojunction interface) (EPO):
This subclass is indented under subclass E29.242. This subclass is substantially the

same in scope as ECLA classification H01L29/778.

E29.247 With inverted single heterostructure (i.e., with active layer formed on top of wide bandgap layer (e.g., IHEMT)) (EPO):
This subclass is indented under subclass E29.246. This subclass is substantially the same in scope as ECLA classification H01L29/778B.

E29.248 With confinement of carriers by at least two heterojunctions (e.g., DHHEMT, quantum well HEMT, DHMODFET) (EPO):
This subclass is indented under subclass E29.246. This subclass is substantially the same in scope as ECLA classification H01L29/778C.

E29.249 Using Group III-V semiconductor material (EPO):
This subclass is indented under subclass E29.248. This subclass is substantially the same in scope as ECLA classification H01L29/778C2.

E29.25 With more than one donor layer (EPO):
This subclass is indented under subclass E29.249. This subclass is substantially the same in scope as ECLA classification H01L29/778C2C.

E29.251 With delta or planar doped donor layer (EPO):
This subclass is indented under subclass E29.249. This subclass is substantially the same in scope as ECLA classification H01L29/778C2B.

E29.252 With direct single heterostructure (i.e., with wide bandgap layer formed on top of active layer (e.g., direct single heterostructure MIS-like HEMT)) (EPO):
This subclass is indented under subclass E29.246. This subclass is substantially the same in scope as ECLA classification H01L29/778E.

E29.253 With wide bandgap charge-carrier supplying layer (e.g., direct single heterostructure MODFET) (EPO):
This subclass is indented under subclass E29.252. This subclass is substantially the same in scope as ECLA classification H01L29/778E2.

E29.254 With delta-doped channel (EPO):
This subclass is indented under subclass E29.242. This subclass is substantially the same in scope as ECLA classification H01L29/772C.

E29.255 With field effect produced by insulated gate (EPO):
This subclass is indented under subclass E29.242. This subclass is substantially the same in scope as ECLA classification H01L29/78.

E29.256 With channel containing layer contacting drain drift region (e.g., DMOS transistor) (EPO):
This subclass is indented under subclass E29.255. This subclass is substantially the same in scope as ECLA classification H01L29/78B.

E29.257 Having vertical bulk current component or current vertically following trench gate (e.g., vertical power DMOS transistor) (EPO):
This subclass is indented under subclass E29.256. This subclass is substantially the same in scope as ECLA classification H01L29/78B2.

E29.258 With both source and drain contacts in same substrate side (EPO):
This subclass is indented under subclass E29.257. This subclass is substantially the same in scope as ECLA classification H01L29/78B2C.

E29.259 With nonplanar surface (EPO):
This subclass is indented under subclass E29.257. This subclass is substantially the same in scope as ECLA classification H01L29/78B2B.

E29.26 Channel structure lying under slanted or vertical surface or being formed along surface of groove (e.g., trench gate DMOSFET) (EPO):
This subclass is indented under subclass E29.259. This subclass is substantially the same in scope as ECLA classification H01L29/78B2B2.

E29.261 With at least part of active region on insulating substrate (e.g., lateral DMOS in oxide isolated well) (EPO):

This subclass is indented under subclass E29.256. This subclass is substantially the same in scope as ECLA classification H01L29/78B1.

SEE OR SEARCH THIS CLASS, SUBCLASS:

E29.273,for thin film transistors.

E29.262 Vertical transistor (EPO):

This subclass is indented under subclass E29.255. This subclass is substantially the same in scope as ECLA classification H01L29/78C.

SEE OR SEARCH THIS CLASS, SUBCLASS:

E29.131,for gate electrodes for channels having a nonvertical component.

E29.257,for vertical transistors with a drain drift region contacting the channel.

E29.274,for unipolar insulated gate field effect thin film vertical transistors.

E29.263 Comprising gate-to-body connection (i.e., bulk dynamic threshold voltage MOSFET) (EPO):

This subclass is indented under subclass E29.255. This subclass is substantially the same in scope as ECLA classification H01L29/78D.

SEE OR SEARCH THIS CLASS, SUBCLASS:

E29.281,and E29.299, for thin film transistors.

E29.264 With multiple gate structure (EPO):

This subclass is indented under subclass E29.255. This subclass is substantially the same in scope as ECLA classification H01L29/78E.

SEE OR SEARCH THIS CLASS, SUBCLASS:

E29.275,for thin film transistors.

E29.265 Structure comprising MOS gate and at least one non-MOS gate (e.g., JFET or MESFET gate) (EPO):

This subclass is indented under subclass E29.264. This subclass is substantially the same in scope as ECLA classification H01L29/78E2.

E29.266 With lightly doped drain or source extension (EPO):

This subclass is indented under subclass E29.255. This subclass is substantially the same in scope as ECLA classification H01L29/78F.

SEE OR SEARCH THIS CLASS, SUBCLASS:

E29.277,for vertical thin film transistors having particular drain or source properties.

E29.267 With nonplanar structure (e.g., gate or source or drain being nonplanar) (EPO):

This subclass is indented under subclass E29.266. This subclass is substantially the same in scope as ECLA classification H01L29/78F2.

(1) Note. Field oxide sunken in the substrate and not filling a groove is not an element characterizing a nonplanar structure.

E29.268 Source region and drain region having nonsymmetrical structure about gate electrode (EPO):

This subclass is indented under subclass E29.266. This subclass is substantially the same in scope as ECLA classification H01L29/78F3.

E29.269 With overlap between lightly doped extension and gate electrode (EPO):

This subclass is indented under subclass E29.266. This subclass is substantially the same in scope as ECLA classification H01L29/78F4.

E29.27 With buried channel (EPO):

This subclass is indented under subclass E29.255. This subclass is substantially the same in scope as ECLA classification H01L29/78G.

E29.271 With Schottky drain or source contact (EPO):
This subclass is indented under subclass E29.255. This subclass is substantially the same in scope as ECLA classification H01L29/78H.

E29.272 Gate comprising ferroelectric layer (EPO):
This subclass is indented under subclass E29.255. This subclass is substantially the same in scope as ECLA classification H01L29/78K.

E29.273 Thin-film transistor (EPO):
This subclass is indented under subclass E29.255. This subclass is substantially the same in scope as ECLA classification H01L29/786.

SEE OR SEARCH THIS CLASS, SUBCLASS:
E29.021, for transistors having only the source or the drain region on an insulator layer.

E29.274 Vertical transistor (EPO):
This subclass is indented under subclass E29.273. This subclass is substantially the same in scope as ECLA classification H01L29/786C.

E29.275 With multiple gates (EPO):
This subclass is indented under subclass E29.273. This subclass is substantially the same in scope as ECLA classification H01L29/786D.

SEE OR SEARCH THIS CLASS, SUBCLASS:
E29.285 through E29.299, the materials specified for the transistors are the material of the channel region.

E29.276 With supplementary region or layer in thin film or in insulated bulk substrate supporting it for controlling or increasing voltage resistance of device (EPO):
This subclass is indented under subclass E29.273. This subclass is substantially the same in scope as ECLA classification H01L29/786B.

E29.277 Characterized by drain or source properties (EPO):
This subclass is indented under subclass E29.276. This subclass is substantially the same in scope as ECLA classification H01L29/786B4.

SEE OR SEARCH THIS CLASS, SUBCLASS:
E29.147, for silicide contacts; electrodes, in general.

E29.278 With LDD structure or extension or offset region or characterized by doping profile (EPO):
This subclass is indented under subclass 29.277. This subclass is substantially the same in scope as ECLA classification H01L29/786B4B.

E29.279 Asymmetrical source and drain regions (EPO):
This subclass is indented under subclass E29.278. This subclass is substantially the same in scope as ECLA classification H01L29/786B4B2.

E29.28 For preventing leakage current (EPO):
This subclass is indented under subclass E29.276. This subclass is substantially the same in scope as ECLA classification H01L29/786B2.

E29.281 For preventing kink or snapback effect (e.g., discharging minority carriers of channel region for preventing bipolar effect) (EPO):
This subclass is indented under subclass E29.276. This subclass is substantially the same in scope as ECLA classification H01L29/786B3.

E29.282 With light shield (EPO):
This subclass is indented under subclass E29.276. This subclass is substantially the same in scope as ECLA classification H01L29/786B5.

E29.283 With supplementary region or layer for improving flatness of device (EPO):
This subclass is indented under subclass E29.276. This subclass is substantially the same in scope as ECLA classification H01L29/786B6.

E29.284 With drain or source connected to bulk conducting substrate (EPO):
This subclass is indented under subclass E29.276. This subclass is substantially the same in scope as ECLA classification H01L29/786B7.

E29.285 Silicon transistor (EPO):
This subclass is indented under subclass E29.273. This subclass is substantially the same in scope as ECLA classification H01L29/786E.

E29.286 Monocrystalline only (EPO):
This subclass is indented under subclass E29.285. This subclass is substantially the same in scope as ECLA classification H01L29/786E2.

E29.287 SOS transistor (EPO):
This subclass is indented under subclass E29.286. This subclass is substantially the same in scope as ECLA classification H01L29/786E2B.

E29.288 Nonmonocrystalline (EPO):
This subclass is indented under subclass E29.285. This subclass is substantially the same in scope as ECLA classification H01L29/786E4.

E29.289 Amorphous silicon transistor (EPO):
This subclass is indented under subclass E29.288. This subclass is substantially the same in scope as ECLA classification H01L29/786E4B.

E29.29 With top gate (EPO):
This subclass is indented under subclass E29.289. This subclass is substantially the same in scope as ECLA classification H01L29/786E4B2.

E29.291 With inverted transistor structure (EPO):
This subclass is indented under subclass E29.289. This subclass is substantially the same in scope as ECLA classification H01L29/786E4B4.

E29.292 Polycrystalline or microcrystalline silicon transistor (EPO):
This subclass is indented under subclass E29.288. This subclass is substantially the same in scope as ECLA classification H01L29/786E4C.

E29.293 With top gate (EPO):
This subclass is indented under subclass E29.292. This subclass is substantially the same in scope as ECLA classification H01L29/786E4C2.

E29.294 With inverted transistor structure (EPO):
This subclass is indented under subclass E29.292. This subclass is substantially the same in scope as ECLA classification H01L29/786E4C4.

E29.295 Characterized by insulating substrate or support (EPO):
This subclass is indented under subclass E29.273. This subclass is substantially the same in scope as ECLA classification H01L29/786A.

E29.296 Comprising Group III-V or II-VI compound, or of Se, Te, or oxide semiconductor (EPO):
This subclass is indented under subclass E29.273. This subclass is substantially the same in scope as ECLA classification H01L29/786F.

E29.297 Comprising Group IV non-Si semiconductor materials or alloys (e.g., Ge, SiN alloy, SiC alloy) (EPO):
This subclass is indented under subclass E29.273. This subclass is substantially the same in scope as ECLA classification H01L29/786G.

E29.298 With multilayer structure or superlattice structure (EPO):
This subclass is indented under subclass E29.297. This subclass is substantially the same in scope as ECLA classification H01L29/786G2.

E29.299 Characterized by property or structure of channel or contact thereto (EPO):
This subclass is indented under subclass E29.273. This subclass is substantially the same in scope as ECLA classification H01L29/786H.

SEE OR SEARCH THIS CLASS, SUBCLASS:
E29.278,for transistors having a drain offset region or a lightly doped drain (LDD).

E29.3 With floating gate (EPO):
This subclass is indented under subclass E29.255. This subclass is substantially the same in scope as ECLA classification H01L29/788.

E29.301 Programmable by two single electrons (EPO):
This subclass is indented under subclass E29.3. This subclass is substantially the same in scope as ECLA classification H01L29/788D.

E29.302 Hi-lo programming levels only (EPO):
This subclass is indented under subclass E29.300. This subclass is substantially the same in scope as ECLA classification H01L29/788B.

E29.303 Charging by injection of carriers through conductive insulator (e.g., Poole-Frankel conduction) (EPO):
This subclass is indented under subclass E29.302. This subclass is substantially the same in scope as ECLA classification H01L29/788B2.

E29.304 Charging by tunneling of carriers (e.g., Fowler-Nordheim tunneling) (EPO):
This subclass is indented under subclass E29.302. This subclass is substantially the same in scope as ECLA classification H01L29/788B4.

E29.305 Charging by hot carrier injection (EPO):
This subclass is indented under subclass E29.302. This subclass is substantially the same in scope as ECLA classification H01L29/788B6.

E29.306 Hot carrier injection from channel (EPO):
This subclass is indented under subclass E29.305. This subclass is substantially the same in scope as ECLA classification H01L29/788B6B.

E29.307 Hot carrier produced by avalanche breakdown of PN junction (e.g., FAMOS) (EPO):
This subclass is indented under subclass E29.305. This subclass is substantially the same in scope as ECLA classification H01L29/788B6C.

E29.308 Programmable with more than two possible different levels (EPO):
This subclass is indented under subclass E29.3. This subclass is substantially the same in scope as ECLA classification H01L29/788C.

E29.309 With charge trapping gate insulator (e.g., MNOS-memory transistors) (EPO):
This subclass is indented under subclass E29.255. This subclass is substantially the same in scope as ECLA classification H01L29/792.

E29.31 With field effect produced by PN or other rectifying junction gate (i.e., potential barrier) (EPO):
This subclass is indented under subclass E29.242. This subclass is substantially the same in scope as ECLA classification H01L29/80.

E29.311 With Schottky drain or source contact (EPO):
This subclass is indented under subclass E29.31. This subclass is substantially the same in scope as ECLA classification H01L29/80C.

E29.312 With PN junction gate (e.g., PN homojunction gate) (EPO):
This subclass is indented under subclass E29.31. This subclass is substantially the same in scope as ECLA classification H01L29/808.

E29.313 Vertical transistors (EPO):
This subclass is indented under subclass E29.312. This subclass is substantially the same in scope as ECLA classification H01L29/808B.

SEE OR SEARCH THIS CLASS, SUBCLASS:
E29.243,for SIT.

E29.314 Thin-film JFET (EPO):
This subclass is indented under subclass E29.312. This subclass is substantially the

same in scope as ECLA classification H01L29/808C.

E29.315 With heterojunction gate (e.g., transistors with semiconductor layer acting as gate insulating layer) (EPO):
This subclass is indented under subclass E29.31. This subclass is substantially the same in scope as ECLA classification H01L29/80B.

SEE OR SEARCH THIS CLASS, SUBCLASS:
E29.245,with one-dimensional electron gas.
E29.246,with two-dimensional electron gas.

E29.316 Programmable transistor (e.g., with charge-trapping quantum well) (EPO):
This subclass is indented under subclass E29.315. This subclass is substantially the same in scope as ECLA classification H01L29/80B2.

E29.317 With Schottky gate (EPO):
This subclass is indented under subclass E29.31. This subclass is substantially the same in scope as ECLA classification H01L29/812.

SEE OR SEARCH THIS CLASS, SUBCLASS:
E29.315, for Schottky contact on top of heterojunction gate.

E29.318 Vertical transistors (EPO):
This subclass is indented under subclass E29.317. This subclass is substantially the same in scope as ECLA classification H01L29/812B.

SEE OR SEARCH THIS CLASS, SUBCLASS:
E29.243,for SIT, PBT.

E29.319 With multiple gate (EPO):
This subclass is indented under subclass E29.317. This subclass is substantially the same in scope as ECLA classification H01L29/812C.

E29.32 Thin-film MESFET (EPO):
This subclass is indented under subclass E29.317. This subclass is substantially the same in scope as ECLA classification H01L29/812D.

E29.321 With recessed gate (EPO):
This subclass is indented under subclass E29.317. This subclass is substantially the same in scope as ECLA classification H01L29/812E.

E29.322 Single electron transistors: Coulomb blockade device (EPO):
This subclass is indented under subclass E29.226. This subclass is substantially the same in scope as ECLA classification H01L29/76D.

E29.323 Controllable by variation of magnetic field applied to device (EPO):
This subclass is indented under subclass E29.166. This subclass is substantially the same in scope as ECLA classification H01L29/82.

E29.324 Controllable by variation of applied mechanical force (e.g., of pressure) (EPO):
This subclass is indented under subclass E29.166. This subclass is substantially the same in scope as ECLA classification H01L29/84.

E29.325 Controllable only by variation of electric current supplied or only electric potential applied to electrode carrying current to be rectified, amplified, oscillated, or switched (EPO):
This subclass is indented under subclass E29.166. This subclass is substantially the same in scope as ECLA classification H01L29/86.

E29.326 Resistor with PN junction (EPO):
This subclass is indented under subclass E29.325. This subclass is substantially the same in scope as ECLA classification H01L29/8605.

E29.327 Diode (EPO):
This subclass is indented under subclass E29.325. This subclass is substantially the same in scope as ECLA classification H01L29/861.

E29.328 Planar PN junction diode (EPO):
This subclass is indented under subclass E29.327. This subclass is substantially the

same in scope as ECLA classification H01L29/861B.

E29.329 Mesa PN junction diode (EPO):
This subclass is indented under subclass E29.327. This subclass is substantially the same in scope as ECLA classification H01L29/861C.

E29.33 Hi-lo semiconductor device (e.g., memory device) (EPO):
This subclass is indented under subclass E29.327. This subclass is substantially the same in scope as ECLA classification H01L29/861E.

E29.331 Charge trapping diode (EPO):
This subclass is indented under subclass E29.327. This subclass is substantially the same in scope as ECLA classification H01L29/861F.

E29.332 Punchthrough diode (i.e., with bulk potential barrier (e.g., camel diode, planar doped barrier diode, graded bandgap diode)) (EPO):
This subclass is indented under subclass E29.327. This subclass is substantially the same in scope as ECLA classification H01L29/861P.

E29.333 Point contact diode (EPO):
This subclass is indented under subclass E29.327. This subclass is substantially the same in scope as ECLA classification H01L29/862.

E29.334 Transit-time diode (e.g., IMPATT, TRAPATT diode) (EPO):
This subclass is indented under subclass E29.327. This subclass is substantially the same in scope as ECLA classification H01L29/864.

E29.335 Avalanche diode (e.g., Zener diode) (EPO):
This subclass is indented under subclass E29.327. This subclass is substantially the same in scope as ECLA classification H01L29/866.

E29.336 PIN diode (EPO):
This subclass is indented under subclass E29.327. This subclass is substantially the same in scope as ECLA classification H01L29/868.

E29.337 Thyristor diode (i.e., having only two terminals and no control electrode (e.g., Shockley diode, break-over diode)) (EPO):
This subclass is indented under subclass E29.327. This subclass is substantially the same in scope as ECLA classification H01L29/87.

E29.338 Schottky diode (EPO):
This subclass is indented under subclass E29.327. This subclass is substantially the same in scope as ECLA classification H01L29/872.

E29.339 Tunneling diode (EPO):
This subclass is indented under subclass E29.327. This subclass is substantially the same in scope as ECLA classification H01L29/88.

E29.34 Resonant tunneling diode (i.e., RTD, RTBD) (EPO):
This subclass is indented under subclass E29.339. This subclass is substantially the same in scope as ECLA classification H01L29/88R.

E29.341 Esaki diode (EPO):
This subclass is indented under subclass E29.339. This subclass is substantially the same in scope as ECLA classification H01L29/885.

E29.342 Capacitor with potential barrier or surface barrier (EPO):
This subclass is indented under subclass E29.325. This subclass is substantially the same in scope as ECLA classification H01L29/92.

E29.343 Conductor-insulator-conductor capacitor on semiconductor substrate (EPO):
This subclass is indented under subclass E29.342. This subclass is substantially the same in scope as ECLA classification H01L29/92B.

E29.344 Variable capacitance diode (e.g., varactors) (EPO):
This subclass is indented under subclass E29.342. This subclass is substantially the

same in scope as ECLA classification H01L29/93.

E29.345 Metal-insulator-semiconductor (e.g., MOS capacitor) (EPO):
This subclass is indented under subclass E29.342. This subclass is substantially the same in scope as ECLA classification H01L29/94.

E29.346 Trench capacitor (EPO):
This subclass is indented under subclass E29.345. This subclass is substantially the same in scope as ECLA classification H01L29/94B.

E29.347 Controllable by thermal signal (e.g., IR) (EPO):
This subclass is indented under subclass E29.166. This subclass is substantially the same in scope as ECLA classification H01L29/66B.

E31.001 Semiconductor devices responsive or sensitive to electromagnetic radiation (e.g., infra-red radiation, adapted for conversion of radiation into electrical energy or for control of electrical energy by such radiation, processes or apparatus peculiar to manufacture or treatment of such devices, or of parts thereof) (EPO):
This main group provides for semiconductor devices that are sensitive to infra-red radiation, light, electromagnetic radiation of shorter wavelength or corpuscular radiation and adapted either for the conversion of the energy of such radiation into electrical energy or for the control of electrical energy by such radiation, and processes or apparatus peculiar to the manufacture or treatment of such devices or of parts thereof. This subclass is substantially the same in scope as ECLA classification H01L31/00.

E31.002 Characterized by semiconductor body (EPO):
This subclass is indented under subclass E31.001. This subclass is substantially the same in scope as ECLA classification H01L31/0248.

E31.003 Characterized by semiconductor body material (EPO):
This subclass is indented under subclass E31.002. This subclass is substantially the same in scope as ECLA classification H01L31/0256.

E31.004 Inorganic materials (EPO):
This subclass is indented under subclass E31.003. This subclass is substantially the same in scope as ECLA classification H01L31/0264.

E31.005 In different semiconductor regions (e.g., Cu_2X/CdX heterojunction and X being Group VI element) (EPO):
This subclass is indented under subclass E31.004. This subclass is substantially the same in scope as ECLA classification H01L31/0336.

E31.006 Comprising only Cu_2X/CdX heterojunction and X being Group VI element (EPO):
This subclass is indented under subclass E31.005. This subclass is substantially the same in scope as ECLA classification H01L31/0336B.

E31.007 Comprising only heterojunction including Group I-III-VI compound (e.g., CdS/$CuInSe_2$ heterojunction) (EPO):
This subclass is indented under subclass E31.005. This subclass is substantially the same in scope as ECLA classification H01L31/0336C.

E31.008 Selenium or tellurium (EPO):
This subclass is indented under subclass E31.004. This subclass is substantially the same in scope as ECLA classification H01L31/0272.

E31.009 For device having potential or surface barrier (EPO):
This subclass is indented under subclass E31.008. This subclass is substantially the same in scope as ECLA classification H01L31/0272B.

E31.01 Characterized by doping material (EPO):
This subclass is indented under subclass E31.008. This subclass is substantially the

same in scope as ECLA classification H01L31/0272C.

E31.011 Including, apart from doping material or other impurity, only Group IV element (EPO):
This subclass is indented under subclass E31.004. This subclass is substantially the same in scope as ECLA classification H01L31/028.

E31.012 For device having potential or surface barrier (EPO):
This subclass is indented under subclass E31.011. This subclass is substantially the same in scope as ECLA classification H01L31/028B.

E31.013 Comprising porous silicon as part of active layer (EPO):
This subclass is indented under subclass E31.011. This subclass is substantially the same in scope as ECLA classification H01L31/028P.

E31.014 Characterized by doping material (EPO):
This subclass is indented under subclass E31.011. This subclass is substantially the same in scope as ECLA classification H01L31/0288.

E31.015 Including, apart from doping material or other impurity, only Group II-VI compound (e.g., CdS, ZnS, HgCdTe) (EPO):
This subclass is indented under subclass E31.004. This subclass is substantially the same in scope as ECLA classification H01L31/0296.

E31.016 For device having potential or surface barrier (EPO):
This subclass is indented under subclass E31.015. This subclass is substantially the same in scope as ECLA classification H01L31/0296B.

E31.017 Characterized by doping material (EPO):
This subclass is indented under subclass E31.016. This subclass is substantially the same in scope as ECLA classification H01L31/0296B2.

E31.018 Including ternary compound (e.g., HgCdTe) (EPO):
This subclass is indented under subclass E31.015. This subclass is substantially the same in scope as ECLA classification H01L31/0296C.

E31.019 Including, apart from doping material or other impurity, only Group III-V compound (EPO):
This subclass is indented under subclass E31.004. This subclass is substantially the same in scope as ECLA classification H01L31/0304.

E31.02 For device having potential or surface barrier (EPO):
This subclass is indented under subclass E31.019. This subclass is substantially the same in scope as ECLA classification H01L31/0304B.

E31.021 Characterized by doping material GaAlAs, InGaAs, InGaAsP (EPO):
This subclass is indented under subclass E31.02. This subclass is substantially the same in scope as ECLA classification H01L31/0304B2.

E31.022 Including ternary or quaternary compound (EPO):
This subclass is indented under subclass E31.019. This subclass is substantially the same in scope as ECLA classification H01L31/0304C.

E31.023 Including, apart from doping material or other impurity, only Group IV compound (e.g., SiC) (EPO):
This subclass is indented under subclass E31.004. This subclass is substantially the same in scope as ECLA classification H01L31/0312.

E31.024 For device having potential or surface barrier (EPO):
This subclass is indented under subclass E31.023. This subclass is substantially the same in scope as ECLA classification H01L31/0312B.

E31.025 Characterized by doping material (EPO):
This subclass is indented under subclass E31.023. This subclass is substantially the same in scope as ECLA classification H01L31/0312C.

E31.026 Including, apart from doping material or other impurity, only compound other than Group II-VI, III-V, and IV compound (EPO):
This subclass is indented under subclass E31.004. This subclass is substantially the same in scope as ECLA classification H01L31/032.

E31.027 Comprising only Group I-III-VI chalcopyrite compound (e.g., $CuInSe_2$, $CuGaSe_2$, $CuInGaSe_2$) (EPO):
This subclass is indented under subclass E31.026. This subclass is substantially the same in scope as ECLA classification H01L31/032C.

E31.028 Characterized by doping material (EPO):
This subclass is indented under subclass E31.027. This subclass is substantially the same in scope as ECLA classification H01L31/032C2.

E31.029 Comprising only Group IV-VI or II-IV-VI chalcogenide compound (e.g., PbSnTe) (EPO):
This subclass is indented under subclass E31.026. This subclass is substantially the same in scope as ECLA classification H01L31/032D.

E31.03 Characterized by doping material (EPO):
This subclass is indented under subclass E31.029. This subclass is substantially the same in scope as ECLA classification H01L31/032D2.

E31.031 Characterized by doping material (EPO):
This subclass is indented under subclass E31.026. This subclass is substantially the same in scope as ECLA classification H01L31/032B.

E31.032 Characterized by semiconductor body shape, relative size, or disposition of semiconductor regions (EPO):
This subclass is indented under subclass E31.002. This subclass is substantially the same in scope as ECLA classification H01L31/0352.

E31.033 Multiple quantum well structure (EPO):
This subclass is indented under subclass E31.032. This subclass is substantially the same in scope as ECLA classification H01L31/0352B.

E31.034 Characterized by amorphous semiconductor layer (EPO):
This subclass is indented under subclass E31.033. This subclass is substantially the same in scope as ECLA classification H01L31/0352B2.

E31.035 Including, apart from doping material or other impurity, only Group IV element or compound (e.g., Si-SiGe superlattice) (EPO):
This subclass is indented under subclass E31.033. This subclass is substantially the same in scope as ECLA classification H01L31/0352B3.

E31.036 Doping superlattice (e.g., nipi superlattice) (EPO):
This subclass is indented under subclass E31.033. This subclass is substantially the same in scope as ECLA classification H01L31/0352B4.

E31.037 For device having potential or surface barrier (EPO):
This subclass is indented under subclass E31.032. This subclass is substantially the same in scope as ECLA classification H01L31/0352C.

E31.038 Shape of body (EPO):
This subclass is indented under subclass E31.037. This subclass is substantially the same in scope as ECLA classification H01L31/0352C2.

E31.039 Shape of potential or surface barrier (EPO):
This subclass is indented under subclass E31.037. This subclass is substantially the

same in scope as ECLA classification H01L31/0352C3.

E31.04 Characterized by semiconductor body crystalline structure or plane (EPO):
This subclass is indented under subclass E31.002. This subclass is substantially the same in scope as ECLA classification H01L31/036.

E31.041 Including thin film deposited on metallic or insulating substrate (EPO):
This subclass is indented under subclass E31.04. This subclass is substantially the same in scope as ECLA classification H01L31/0392.

E31.042 Including only Group IV element (EPO):
This subclass is indented under subclass E31.041. This subclass is substantially the same in scope as ECLA classification H01L31/0392B.

E31.043 Including polycrystalline semiconductor (EPO):
This subclass is indented under subclass E31.04. This subclass is substantially the same in scope as ECLA classification H01L31/0368.

E31.044 Including only Group IV element (EPO):
This subclass is indented under subclass E31.043. This subclass is substantially the same in scope as ECLA classification H01L31/0368B.

E31.045 Including microcrystalline silicon (c-Si) (EPO):
This subclass is indented under subclass E31.044. This subclass is substantially the same in scope as ECLA classification H01L31/0368B2.

E31.046 Including microcrystalline Group IV compound (e.g., c-SiGe, c-SiC) (EPO):
This subclass is indented under subclass E31.044. This subclass is substantially the same in scope as ECLA classification H01L31/0368B3.

E31.047 Including amorphous semiconductor (EPO):
This subclass is indented under subclass E31.04. This subclass is substantially the same in scope as ECLA classification H01L31/0376.

E31.048 Including only Group IV element (EPO):
This subclass is indented under subclass E31.047. This subclass is substantially the same in scope as ECLA classification H01L31/0376B.

E31.049 Including Group IV compound (e.g., SiGe, SiC) (EPO):
This subclass is indented under subclass E31.048. This subclass is substantially the same in scope as ECLA classification H01L31/0376B2.

E31.05 Having light-induced characteristic variation (e.g., Staebler-Wronski effect) (EPO):
This subclass is indented under subclass E31.048. This subclass is substantially the same in scope as ECLA classification H01L31/0376B3.

E31.051 Including other nonmonocrystalline material (e.g., semiconductor particles embedded in insulating material) (EPO):
This subclass is indented under subclass E31.04. This subclass is substantially the same in scope as ECLA classification H01L31/0384.

E31.052 Adapted to control current flow through device (e.g., photoresistor) (EPO):
This subclass is indented under subclass E31.001. This subclass is substantially the same in scope as ECLA classification H01L31/08.

E31.053 For device having potential or surface barrier (e.g., phototransistor) (EPO):
This subclass is indented under subclass E31.052. This subclass is substantially the same in scope as ECLA classification H01L31/10.

E31.054 Device sensitive to infrared, visible, or ultraviolet radiation (EPO):
This subclass is indented under subclass E31.053. This subclass is substantially the same in scope as ECLA classification H01L31/101.

SEE OR SEARCH THIS CLASS, SUBCLASS:
E31.093,and its indents, for device sensitive to infrared, visible, or ultraviolet radia-

tion without a potential or surface barrier.

E31.055 Characterized by only one potential or surface barrier (EPO):
This subclass is indented under subclass E31.054. This subclass is substantially the same in scope as ECLA classification H01L31/102.

E31.056 Potential barrier being of point contact type (EPO):
This subclass is indented under subclass E31.055. This subclass is substantially the same in scope as ECLA classification H01L31/102B.

E31.057 PN homojunction potential barrier (EPO):
This subclass is indented under subclass E31.055. This subclass is substantially the same in scope as ECLA classification H01L31/103.

E31.058 Device comprising active layer formed only by Group II-VI compound (e.g., HgCdTe IR photodiode) (EPO):
This subclass is indented under subclass E31.057. This subclass is substantially the same in scope as ECLA classification H01L31/103B.

E31.059 Device comprising active layer formed only by Group III-V compound (EPO):
This subclass is indented under subclass E31.057. This subclass is substantially the same in scope as ECLA classification H01L31/103C.

E31.06 Device comprising active layer formed only by Group IV compound (EPO):
This subclass is indented under subclass E31.057. This subclass is substantially the same in scope as ECLA classification H01L31/103D.

E31.061 PIN potential barrier (EPO):
This subclass is indented under subclass E31.055. This subclass is substantially the same in scope as ECLA classification H01L31/105.

E31.062 Device comprising Group IV amorphous material (EPO):
This subclass is indented under subclass E31.061. This subclass is substantially the same in scope as ECLA classification H01L31/105B.

E31.063 Potential barrier working in avalanche mode (e.g., avalanche photodiode) (EPO):
This subclass is indented under subclass E31.055. This subclass is substantially the same in scope as ECLA classification H01L31/107.

E31.064 Heterostructure (e.g., surface absorption or multiplication (SAM) layer) (EPO):
This subclass is indented under subclass E31.063. This subclass is substantially the same in scope as ECLA classification H01L31/107B.

E31.065 Schottky potential barrier (EPO):
This subclass is indented under subclass E31.055. This subclass is substantially the same in scope as ECLA classification H01L31/108.

E31.066 Metal-semiconductor-metal (MSM) Schottky barrier (EPO):
This subclass is indented under subclass E31.065. This subclass is substantially the same in scope as ECLA classification H01L31/108B.

E31.067 PN heterojunction potential barrier (EPO):
This subclass is indented under subclass E31.055. This subclass is substantially the same in scope as ECLA classification H01L31/109.

E31.068 Characterized by two potential or surface barriers (EPO):
This subclass is indented under subclass E31.054. This subclass is substantially the same in scope as ECLA classification H01L31/11.

E31.069 Bipolar phototransistor (EPO):
This subclass is indented under subclass E31.068. This subclass is substantially the same in scope as ECLA classification H01L31/11B.

E31.07 Characterized by at least three potential barriers (EPO):
This subclass is indented under subclass E31.054. This subclass is substantially the same in scope as ECLA classification H01L31/111.

E31.071 Photothyristor (EPO):
This subclass is indented under subclass E31.07. This subclass is substantially the same in scope as ECLA classification H01L31/111B.

E31.072 Static induction type (i.e., SIT device) (EPO):
This subclass is indented under subclass E31.071. This subclass is substantially the same in scope as ECLA classification H01L31/111B2.

E31.073 Field-effect type (e.g., junction field-effect phototransistor) (EPO):
This subclass is indented under subclass E31.054. This subclass is substantially the same in scope as ECLA classification H01L31/112.

E31.074 With Schottky gate (EPO):
This subclass is indented under subclass E31.073. This subclass is substantially the same in scope as ECLA classification H01L31/112B.

E31.075 Charge-coupled device (CCD) (EPO):
This subclass is indented under subclass E31.074. This subclass is substantially the same in scope as ECLA classification H01L31/112B2.

E31.076 Photo MESFET (EPO):
This subclass is indented under subclass E31.074. This subclass is substantially the same in scope as ECLA classification H01L31/112B3.

E31.077 With PN homojunction gate (EPO):
This subclass is indented under subclass E31.073. This subclass is substantially the same in scope as ECLA classification H01L31/112C.

E31.078 Charge-coupled device (CCD) (EPO):
This subclass is indented under subclass E31.077. This subclass is substantially the same in scope as ECLA classification H01L31/112C2.

E31.079 Field-effect phototransistor (EPO):
This subclass is indented under subclass E31.077. This subclass is substantially the same in scope as ECLA classification H01L31/112C3.

E31.08 With PN heterojunction gate (EPO):
This subclass is indented under subclass E31.073. This subclass is substantially the same in scope as ECLA classification H01L31/112D.

E31.081 Charge-coupled device (CCD) (EPO):
This subclass is indented under subclass E31.08. This subclass is substantially the same in scope as ECLA classification H01L31/112D2.

E31.082 Field-effect phototransistor (EPO):
This subclass is indented under subclass E31.08. This subclass is substantially the same in scope as ECLA classification H01L31/112D3.

E31.083 Conductor-insulator-semiconductor type (EPO):
This subclass is indented under subclass E31.073. This subclass is substantially the same in scope as ECLA classification H01L31/113.

E31.084 Diode or charge-coupled device (CCD) (EPO):
This subclass is indented under subclass E31.083. This subclass is substantially the same in scope as ECLA classification H01L31/113B.

E31.085 Metal-insulator-semiconductor field-effect transistor (EPO):
This subclass is indented under subclass E31.083. This subclass is substantially the same in scope as ECLA classification H01L31/113C.

E31.086 Device sensitive to very short wavelength (e.g., X-ray, gamma-ray, or corpuscular radiation) (EPO):
This subclass is indented under subclass E31.053. This subclass is substantially the

same in scope as ECLA classification H01L31/115.

SEE OR SEARCH THIS CLASS, SUBCLASS:

E31.092, for device sensitive to very short wavelength (e.g., X-ray, gamma-ray, or corpuscular radiation without a potential or surface barrier).

E31.087 Bulk-effect radiation detector (e.g., Ge-Li compensated PIN gamma-ray detector) (EPO):

This subclass is indented under subclass E31.086. This subclass is substantially the same in scope as ECLA classification H01L31/117.

E31.088 Li-compensated PIN gamma-ray detector (EPO):

This subclass is indented under subclass E31.087. This subclass is substantially the same in scope as ECLA classification H01L31/117B.

E31.089 With surface barrier or shallow PN junction (e.g., surface barrier alpha-particle detector) (EPO):

This subclass is indented under subclass E31.086. This subclass is substantially the same in scope as ECLA classification H01L31/118.

E31.09 With shallow PN junction (EPO):

This subclass is indented under subclass E31.089. This subclass is substantially the same in scope as ECLA classification H01L31/118B.

E31.091 Field-effect type (e.g., MIS-type detector) (EPO):

This subclass is indented under subclass E31.086. This subclass is substantially the same in scope as ECLA classification H01L31/119.

E31.092 Device being sensitive to very short wavelength (e.g., X-ray, gamma-ray) (EPO):

This subclass is indented under subclass E31.052. This subclass is substantially the same in scope as ECLA classification H01L31/08C.

SEE OR SEARCH THIS CLASS, SUBCLASS:

E31.086, for device sensitive to very short wavelength (e.g., X-ray, gamma-ray, or corpuscular radiation with a potential or surface barrier).

E31.093 Device sensitive to infrared, visible, or ultraviolet radiation (EPO):

This subclass is indented under subclass E31.052. This subclass is substantially the same in scope as ECLA classification H01L31/09.

SEE OR SEARCH THIS CLASS, SUBCLASS:

E31.054, and its indents, for device sensitive to infrared, visible, or ultra-violet radiation with a potential or surface barrier.

E31.094 Comprising amorphous semiconductor (EPO):

This subclass is indented under subclass E31.093. This subclass is substantially the same in scope as ECLA classification H01L31/09B.

E31.095 Structurally associated with electric light source (e.g., electroluminescent light source) (EPO):

This subclass is indented under subclass E31.001. This subclass is substantially the same in scope as ECLA classification H01L31/12.

E31.096 Hybrid device containing photosensitive and electroluminescent components within one single body (EPO):

This subclass is indented under subclass E31.095. This subclass is substantially the same in scope as ECLA classification H01L31/12B.

E31.097 Light source controlled by radiation-sensitive semiconductor device (e.g., image converter, image amplifier, image storage device) (EPO):

This subclass is indented under subclass E31.095. This subclass is substantially the same in scope as ECLA classification H01L31/14.

E31.098 Device without potential or surface barrier (EPO):
This subclass is indented under subclass E31.097. This subclass is substantially the same in scope as ECLA classification H01L31/14B.

E31.099 Light source being semiconductor device with potential or surface barrier (e.g., light-emitting diode) (EPO):
This subclass is indented under subclass E31.098. This subclass is substantially the same in scope as ECLA classification H01L31/14B2.

E31.1 Device with potential or surface barrier (EPO):
This subclass is indented under subclass E31.097. This subclass is substantially the same in scope as ECLA classification H01L31/14C.

E31.101 Semiconductor light source and radiation-sensitive semiconductor device both having potential or surface barrier (EPO):
This subclass is indented under subclass E31.097. This subclass is substantially the same in scope as ECLA classification H01L31/147.

E31.102 Formed in or on common substrate (EPO):
This subclass is indented under subclass E31.101. This subclass is substantially the same in scope as ECLA classification H01L31/153.

E31.103 Radiation-sensitive semiconductor device controlled by light source (EPO):
This subclass is indented under subclass E31.095. This subclass is substantially the same in scope as ECLA classification H01L31/16.

E31.104 Radiation-sensitive semiconductor device without potential or surface barrier (e.g., photoresistor) (EPO):
This subclass is indented under subclass E31.103. This subclass is substantially the same in scope as ECLA classification H01L31/16B.

E31.105 Light source being semiconductor device having potential or surface barrier (e.g., light-emitting diode) (EPO):
This subclass is indented under subclass E31.104. This subclass is substantially the same in scope as ECLA classification H01L31/16B2.

E31.106 Optical potentiometer (EPO):
This subclass is indented under subclass E31.104. This subclass is substantially the same in scope as ECLA classification H01L31/16B4.

E31.107 Radiation-sensitive semiconductor device with potential or surface barrier (EPO):
This subclass is indented under subclass E31.103. This subclass is substantially the same in scope as ECLA classification H01L31/16C.

E31.108 Semiconductor light source and radiation-sensitive semiconductor device both having potential or surface barrier (EPO):
This subclass is indented under subclass E31.103. This subclass is substantially the same in scope as ECLA classification H01L31/167.

E31.109 Formed in or on common substrate (EPO):
This subclass is indented under subclass E31.108. This subclass is substantially the same in scope as ECLA classification H01L31/173.

E31.11 Detail of nonsemiconductor component of radiation-sensitive semiconductor device (EPO):
This subclass is indented under subclass E31.001. This subclass is substantially the same in scope as ECLA classification H01L31/02.

E31.111 Input/output circuit of device (EPO):
This subclass is indented under subclass E31.11. This subclass is substantially the same in scope as ECLA classification H01L31/02E.

E31.112 For device having potential or surface barrier (EPO):
This subclass is indented under subclass E31.111. This subclass is substantially the

same in scope as ECLA classification H01L31/02E2.

E31.113 Circuit arrangement of general character for device (EPO):
This subclass is indented under subclass E31.11. This subclass is substantially the same in scope as ECLA classification H01L31/02H.

E31.114 For device having potential or surface barrier (EPO):
This subclass is indented under subclass E31.113. This subclass is substantially the same in scope as ECLA classification H01L31/02H2.

E31.115 Position-sensitive and lateral-effect photodetector (e.g., quadrant photodiode) (EPO):
This subclass is indented under subclass E31.114. This subclass is substantially the same in scope as ECLA classification H01L31/02H2C.

E31.116 Device working in avalanche mode (EPO):
This subclass is indented under subclass E31.114. This subclass is substantially the same in scope as ECLA classification H01L31/02H2D.

E31.117 Encapsulation (EPO):
This subclass is indented under subclass E31.11. This subclass is substantially the same in scope as ECLA classification H01L31/0203.

SEE OR SEARCH THIS CLASS, SUBCLASS:
E33.059, for encapsulation of other light-emitting semiconductor device.
E51.02, for encapsulation of radiation-sensitive organic semiconductor device.

E31.118 For device having potential or surface barrier (EPO):
This subclass is indented under subclass E31.117. This subclass is substantially the same in scope as ECLA classification H01L31/0203B.

E31.119 Coatings (EPO):
This subclass is indented under subclass E31.11. This subclass is substantially the same in scope as ECLA classification H01L31/0216.

SEE OR SEARCH THIS CLASS, SUBCLASS:
E33.06, for coating details of light-emitting semiconductor device.

E31.12 For device having potential or surface barrier (EPO):
This subclass is indented under subclass E31.119. This subclass is substantially the same in scope as ECLA classification H01L31/0216B.

E31.121 For filtering or shielding light (e.g., multicolor filter for photodetector) (EPO):
This subclass is indented under subclass E31.12. This subclass is substantially the same in scope as ECLA classification H01L31/0216B2.

E31.122 For shielding light (e.g., light-blocking layer, cold shield for infrared detector) (EPO):
This subclass is indented under subclass E31.121. This subclass is substantially the same in scope as ECLA classification H01L31/0216B2B.

E31.123 For interference filter (e.g., multilayer dielectric filter) (EPO):
This subclass is indented under subclass E31.121. This subclass is substantially the same in scope as ECLA classification H01L31/0216B2C.

E31.124 Electrode (EPO):
This subclass is indented under subclass E31.11. This subclass is substantially the same in scope as ECLA classification H01L31/0224.

E31.125 For device having potential or surface barrier (EPO):
This subclass is indented under subclass E31.124. This subclass is substantially the same in scope as ECLA classification H01L31/0224B.

E31.126 Transparent conductive layer (e.g., transparent conductive oxide (TCO), indium tin oxide (ITO) layer) (EPO):
This subclass is indented under subclass E31.124. This subclass is substantially the same in scope as ECLA classification H01L31/0224C.

E31.127 Optical element associated with device (EPO):
This subclass is indented under subclass E31.11. This subclass is substantially the same in scope as ECLA classification H01L31/0232.

E31.128 Device having potential or surface barrier (EPO):
This subclass is indented under subclass E31.127. This subclass is substantially the same in scope as ECLA classification H01L31/0232B.

E31.129 Comprising luminescent member (e.g., fluorescent sheet) (EPO):
This subclass is indented under subclass E31.127. This subclass is substantially the same in scope as ECLA classification H01L31/0232C.

E31.13 Texturized surface (EPO):
This subclass is indented under subclass E31.11. This subclass is substantially the same in scope as ECLA classification H01L31/0236.

E31.131 Arrangement for temperature regulation (e.g., cooling, heating, or ventilating) (EPO):
This subclass is indented under subclass E31.11. This subclass is substantially the same in scope as ECLA classification H01L31/024.

SEE OR SEARCH THIS CLASS, SUBCLASS:
E33.075,for light-emitting cooling or heating means.

E33.001 Light emitting semiconductor devices having potential or surface barrier, processes or apparatus peculiar to manufacture or treatment of such devices, or of parts thereof (EPO):
This main group provides for semiconductor devices with at least one potential-jump barrier or surface barrier adapted for light emission, e.g. infra-red emission, and processes or apparatus peculiar to the manufacture or treatment of such devices or of parts thereof. This subclass is substantially the same in scope as ECLA classification H01L33/00.

(1) Note: This main group does not include semiconductor lasers.

E33.002 Device characterized by semiconductor body (EPO):
This subclass is indented under subclass E33.001. This subclass is substantially the same in scope as ECLA classification H01L33/00C.

E33.003 Particular crystalline orientation or structure (EPO):
This subclass is indented under subclass E33.002. This subclass is substantially the same in scope as ECLA classification H01L33/00C2.

E33.004 Comprising amorphous semiconductor (EPO):
This subclass is indented under subclass E33.003. This subclass is substantially the same in scope as ECLA classification H01L33/00C2B.

E33.005 Shape or structure (e.g., shape of epitaxial layer) (EPO):
This subclass is indented under subclass E33.002. This subclass is substantially the same in scope as ECLA classification H01L33/00C3.

E33.006 Shape of semiconductor body (EPO):
This subclass is indented under subclass E33.005. This subclass is substantially the same in scope as ECLA classification H01L33/00C3B.

E33.007 Shape of potential barrier (EPO):
This subclass is indented under subclass E33.005. This subclass is substantially the same in scope as ECLA classification H01L33/00C3C.

E33.008 Multiple quantum well structure (EPO):
This subclass is indented under subclass E33.005. This subclass is substantially the same in scope as ECLA classification H01L33/00C3D.

E33.009 Including, apart from doping materials or other only impurities, Group IV element (e.g., Si-SiGe superlattice) (EPO):
This subclass is indented under subclass E33.008. This subclass is substantially the same in scope as ECLA classification H01L33/00C3D2.

E33.01 Doped superlattice (e.g., nipi superlattice) (EPO):
This subclass is indented under subclass E33.008. This subclass is substantially the same in scope as ECLA classification H01L33/00C3D3.

E33.011 For current confinement (EPO):
This subclass is indented under subclass E33.005. This subclass is substantially the same in scope as ECLA classification H01L33/00C3E.

E33.012 Multiple active regions between two electrodes (e.g., stacks) (EPO):
This subclass is indented under subclass E33.005. This subclass is substantially the same in scope as ECLA classification H01L33/00C3F.

E33.013 Material of active region (EPO):
This subclass is indented under subclass E33.002. This subclass is substantially the same in scope as ECLA classification H01L33/00C4.

E33.014 In different regions (EPO):
This subclass is indented under subclass E33.013. This subclass is substantially the same in scope as ECLA classification H01L33/00C4G2.

E33.015 Comprising only Group IV element (EPO):
This subclass is indented under subclass E33.013. This subclass is substantially the same in scope as ECLA classification H01L33/00C4B.

E33.016 With heterojunction (EPO):
This subclass is indented under subclass E33.015. This subclass is substantially the same in scope as ECLA classification H01L33/00C4B2.

E33.017 Characterized by doping material (EPO):
This subclass is indented under subclass E33.015. This subclass is substantially the same in scope as ECLA classification H01L33/00C4B3.

E33.018 Including porous Si (EPO):
This subclass is indented under subclass E33.015. This subclass is substantially the same in scope as ECLA classification H01L33/00C4B4.

E33.019 Comprising only Group II-VI compound (EPO):
This subclass is indented under subclass E33.013. This subclass is substantially the same in scope as ECLA classification H01L33/00C4C.

E33.02 Ternary or quaternary compound (e.g., CdHgTe) (EPO):
This subclass is indented under subclass E33.019. This subclass is substantially the same in scope as ECLA classification H01L33/00C4C2.

E33.021 With heterojunction (EPO):
This subclass is indented under subclass E33.02. This subclass is substantially the same in scope as ECLA classification H01L33/00C4C2B.

E33.022 Characterized by doping material (EPO):
This subclass is indented under subclass E33.019. This subclass is substantially the same in scope as ECLA classification H01L33/00C4C3.

E33.023 Comprising only Group III-V compound (EPO):
This subclass is indented under subclass E33.013. This subclass is substantially the same in scope as ECLA classification H01L33/00C4D.

E33.024 Binary compound (e.g., GaAs) (EPO):
This subclass is indented under subclass E33.023. This subclass is substantially the same in scope as ECLA classification H01L33/00C4D2.

E33.025 Including nitride (e.g., GaN) (EPO):
This subclass is indented under subclass E33.024. This subclass is substantially the same in scope as ECLA classification H01L33/00C4D2B.

E33.026 Ternary or quaternary compound (e.g., AlGaAs) (EPO):
This subclass is indented under subclass E33.023. This subclass is substantially the same in scope as ECLA classification H01L33/00C4D3.

E33.027 With heterojunction (EPO):
This subclass is indented under subclass E33.026. This subclass is substantially the same in scope as ECLA classification H01L33/00C4D3B.

E33.028 Including nitride (e.g., AlGaN) (EPO):
This subclass is indented under subclass E33.026. This subclass is substantially the same in scope as ECLA classification H01L33/00C4D3C.

E33.029 Characterized by doping material (EPO):
This subclass is indented under subclass E33.023. This subclass is substantially the same in scope as ECLA classification H01L33/00C4D4.

E33.03 Nitride compound (EPO):
This subclass is indented under subclass E33.029. This subclass is substantially the same in scope as ECLA classification H01L33/00C4D4B.

E33.031 Including ternary or quaternary compound (e.g., AlGaAs) (EPO):
This subclass is indented under subclass E33.023. This subclass is substantially the same in scope as ECLA classification H01L33/00C4D6.

E33.032 With heterojunction (e.g., AlGaAs/GaAs) (EPO):
This subclass is indented under subclass E33.031. This subclass is substantially the same in scope as ECLA classification H01L33/00C4D6B.

E33.033 Comprising nitride compound (e.g., AlGaN) (EPO):
This subclass is indented under subclass E33.031. This subclass is substantially the same in scope as ECLA classification H01L33/00C4D6C.

E33.034 With heterojunction (e.g., AlGaN/GaN) (EPO):
This subclass is indented under subclass E33.033. This subclass is substantially the same in scope as ECLA classification H01L33/00C4D6C2.

E33.035 Comprising only Group IV compound (e.g., SiC) (EPO):
This subclass is indented under subclass E33.013. This subclass is substantially the same in scope as ECLA classification H01L33/00C4E.

E33.036 Characterized by doping material (EPO):
This subclass is indented under subclass E33.035. This subclass is substantially the same in scope as ECLA classification H01L33/00C4E2.

E33.037 Comprising compound other than Group II-VI, III-V, and IV compound (EPO):
This subclass is indented under subclass E33.013. This subclass is substantially the same in scope as ECLA classification H01L33/00C4F.

E33.038 Comprising only Group IV-VI compound (EPO):
This subclass is indented under subclass E33.037. This subclass is substantially the same in scope as ECLA classification H01L33/00C4F2.

E33.039 Comprising only Group II-IV-VI compound (EPO):
This subclass is indented under subclass E33.037. This subclass is substantially the same in scope as ECLA classification H01L33/00C4F3.

E33.04 Comprising only Group I-III-VI compound (EPO):
This subclass is indented under subclass E33.037. This subclass is substantially the same in scope as ECLA classification H01L33/00C4F4.

E33.041 Characterized by doping material (EPO):
This subclass is indented under subclass E33.037. This subclass is substantially the same in scope as ECLA classification H01L33/00C4F5.

E33.042 Comprising only Group IV-VI or II-IV-VI compound (EPO):
This subclass is indented under subclass E33.037. This subclass is substantially the same in scope as ECLA classification H01L33/00C4F6.

E33.043 Physical imperfections (e.g., particular concentration or distribution of impurity) (EPO):
This subclass is indented under subclass E33.002. This subclass is substantially the same in scope as ECLA classification H01L33/00C5.

E33.044 Device characterized by their operation (EPO):
This subclass is indented under subclass E33.001. This subclass is substantially the same in scope as ECLA classification H01L33/00D.

E33.045 Having p-n or hi-lo junction (EPO):
This subclass is indented under subclass E33.044. This subclass is substantially the same in scope as ECLA classification H01L33/00D2.

E33.046 P-I-N device (EPO):
This subclass is indented under subclass E33.045. This subclass is substantially the same in scope as ECLA classification H01L33/00D2B.

E33.047 Having at least two p-n junctions (EPO):
This subclass is indented under subclass E33.045. This subclass is substantially the same in scope as ECLA classification H01L33/00D2C.

E33.048 Having heterojunction or graded gap (EPO):
This subclass is indented under subclass E33.044. This subclass is substantially the same in scope as ECLA classification H01L33/00D3.

E33.049 Comprising only Group III-V compound (EPO):
This subclass is indented under subclass E33.048. This subclass is substantially the same in scope as ECLA classification H01L33/00D3B.

E33.05 Comprising only Group II-IV compound (EPO):
This subclass is indented under subclass E33.048. This subclass is substantially the same in scope as ECLA classification H01L33/00D3C.

E33.051 Having Schottky barrier (EPO):
This subclass is indented under subclass E33.044. This subclass is substantially the same in scope as ECLA classification H01L33/00D4.

E33.052 Having MIS barrier layer (EPO):
This subclass is indented under subclass E33.044. This subclass is substantially the same in scope as ECLA classification H01L33/00D5.

E33.053 Characterized by field-effect operation (EPO):
This subclass is indented under subclass E33.044. This subclass is substantially the same in scope as ECLA classification H01L33/00D6.

E33.054 Device being superluminescent diode (EPO):
This subclass is indented under subclass E33.044. This subclass is substantially the same in scope as ECLA classification H01L33/00D7.

E33.055 Detail of nonsemiconductor component other than light-emitting semiconductor device (EPO):
This subclass is indented under subclass E33.001. This subclass is substantially the same in scope as ECLA classification H01L33/00B.

E33.056 Packaging (EPO):
This subclass is indented under subclass E33.055. This subclass is substantially the same in scope as ECLA classification H01L33/00B2.

E33.057 Adapted for surface mounting (EPO):
This subclass is indented under subclass E33.056. This subclass is substantially the same in scope as ECLA classification H01L33/00B2B.

E33.058 Housing (EPO):
This subclass is indented under subclass E33.056. This subclass is substantially the same in scope as ECLA classification H01L33/00B2C.

E33.059 Encapsulation (EPO):
This subclass is indented under subclass E33.056. This subclass is substantially the same in scope as ECLA classification H01L33/00B2D.

SEE OR SEARCH THIS CLASS, SUBCLASS:
E31.117, for encapsulation of other radiation-sensitive semiconductor device.
E51.02, for encapsulation of radiation-sensitive organic semiconductor device.

E33.06 Coatings (EPO):
This subclass is indented under subclass E33.055. This subclass is substantially the same in scope as ECLA classification H01L33/00B3.

SEE OR SEARCH THIS CLASS, SUBCLASS:
E31.119, for coating details of radiation-sensitive semiconductor device.

E33.061 Comprising luminescent material (e.g., fluorescent) (EPO):
This subclass is indented under subclass E33.06. This subclass is substantially the same in scope as ECLA classification H01L33/00B3B.

E33.062 Electrodes (EPO):
This subclass is indented under subclass E33.055. This subclass is substantially the same in scope as ECLA classification H01L33/00B4.

E33.063 Characterized by material (EPO):
This subclass is indented under subclass E33.062. This subclass is substantially the same in scope as ECLA classification H01L33/00B4B.

E33.064 Comprising transparent conductive layers (e.g., transparent conductive oxides (TCO), indium tin oxide (ITO)) (EPO):
This subclass is indented under subclass E33.063. This subclass is substantially the same in scope as ECLA classification H01L33/00B4B2.

E33.065 Characterized by shape (EPO):
This subclass is indented under subclass E33.062. This subclass is substantially the same in scope as ECLA classification H01L33/00B4C.

E33.066 Electrical contact or lead (e.g., lead frame) (EPO):
This subclass is indented under subclass E33.055. This subclass is substantially the same in scope as ECLA classification H01L33/00B5.

E33.067 Means for light extraction or guiding (EPO):
This subclass is indented under subclass E33.055. This subclass is substantially the same in scope as ECLA classification H01L33/00B6.

E33.068 Integrated with device (e.g., back surface reflector, lens) (EPO):
This subclass is indented under subclass E33.067. This subclass is substantially the same in scope as ECLA classification H01L33/00B6B.

E33.069 Comprising resonant cavity structure (e.g., Bragg reflector pair) (EPO):
This subclass is indented under subclass E33.068. This subclass is substantially the same in scope as ECLA classification H01L33/00B6B2.

E33.07 Comprising window layer (EPO):
This subclass is indented under subclass E33.068. This subclass is substantially the same in scope as ECLA classification H01L33/00B6B3.

E33.071 Not integrated with device (EPO):
This subclass is indented under subclass E33.067. This subclass is substantially the same in scope as ECLA classification H01L33/00B6C.

E33.072 Reflective means (EPO):
This subclass is indented under subclass E33.071. This subclass is substantially the same in scope as ECLA classification H01L33/00B6C2.

E33.073 Refractive means (e.g., lens) (EPO):
This subclass is indented under subclass E33.071. This subclass is substantially the same in scope as ECLA classification H01L33/00B6C3.

E33.074 Scattering means (e.g., surface roughening) (EPO):
This subclass is indented under subclass E33.067. This subclass is substantially the same in scope as ECLA classification H01L33/00B6D.

E33.075 With means for cooling or heating (EPO):
This subclass is indented under subclass E33.055. This subclass is substantially the same in scope as ECLA classification H01L33/00B7.

SEE OR SEARCH THIS CLASS, SUBCLASS:
E31.131,for cooling means for radiation-sensitive semiconductor device.

E33.076 With means for light detecting (e.g., photodetector) (EPO):
This subclass is indented under subclass E33.055. This subclass is substantially the same in scope as ECLA classification H01L33/00B8.

E33.077 Monolithic integration with photosensitive device (EPO):
This subclass is indented under subclass E33.055. This subclass is substantially the same in scope as ECLA classification H01L33/00B9.

E39.001 DEVICES USING SUPERCONDUCTIVITY, PROCESSES, OR APPARATUS PECULIAR TO MANUFACTURE OR TREATMENT OF SUCH DEVICES, OR OF PARTS THEREOF (EPO):
This main group provides for semiconductor or solid state devices with at least one potential-jump barrier or surface barrier which include superconductive material, processes or apparatus peculiar to the manufacture or treatment of such devices or of parts thereof. This subclass is substantially the same in scope as ECLA classification H01L39/00.

(1) Note. Superconductive material is a material that is characterized by zero electrical resistivity and, ideally, zero permeability.

E39.002 Containers or mountings (EPO):
This subclass is indented under subclass E39.001. This subclass is substantially the same in scope as ECLA classification H01L39/04.

E39.003 For Josephson devices (EPO):
This subclass is indented under subclass E39.002. This subclass is substantially the same in scope as ECLA classification H01L39/04B.

E39.004 Characterized by current path (EPO):
This subclass is indented under subclass E.39.001. This subclass is substantially the same in scope as ECLA classification H01L39/06.

E39.005 Characterized by shape of element (EPO):
This subclass is indented under subclass E39.001. This subclass is substantially the same in scope as ECLA classification H01L39/08.

E39.006 Characterized by material (EPO):
This subclass is indented under subclass E39.001. This subclass is substantially the same in scope as ECLA classification H01L39/12.

E39.007 Organic materials (EPO):
This subclass is indented under subclass E39.006. This subclass is substantially the same in scope as ECLA classification H01L39/12B.

E39.008 Fullerene superconductors, e.g., soccerball-shaped allotrope of carbon, e.g., C60, C94 (EPO):
This subclass is indented under subclass E39.007. This subclass is substantially the same in scope as ECLA classification H01L39/12B2.

E39.009 Ceramic materials (EPO):
This subclass is indented under subclass E39.006. This subclass is substantially the

same in scope as ECLA classification H01L39/12C.

E39.01 Comprising copper oxide (EPO):
This subclass is indented under subclass E39.009. This subclass is substantially the same in scope as ECLA classification H01L39/12C2.

E39.011 Multilayered structures, e.g., super lattices (EPO):
This subclass is indented under subclass E39.01. This subclass is substantially the same in scope as ECLA classification H01L39/12C2B.

E39.012 Devices comprising junction of dissimilar materials, e.g., Josephson-effect devices (EPO):
This subclass is indented under subclass E39.001. This subclass is substantially the same in scope as ECLA classification H01L39/22.

E39.013 Single electron tunnelling devices (EPO):
This subclass is indented under subclass E39.012. This subclass is substantially the same in scope as ECLA classification H01L39/22B.

E39.014 Josephson-effect devices (EPO):
This subclass is indented under subclass E39.012. This subclass is substantially the same in scope as ECLA classification H01L39/22C.

E39.015 Comprising high Tc ceramic materials (EPO):
This subclass is indented under subclass E39.014. This subclass is substantially the same in scope as ECLA classification H01L39/22C2.

E39.016 Three or more electrode devices, e.g., transistor-like structures (EPO):
This subclass is indented under subclass E39.012. This subclass is substantially the same in scope as ECLA classification H01L39/22D.

E39.017 Permanent superconductor devices (EPO):
This subclass is indented under subclass E39.001. This subclass is substantially the same in scope as ECLA classification H01L39/14.

E39.018 Comprising high Tc ceramic materials (EPO):
This subclass is indented under subclass E39.017. This subclass is substantially the same in scope as ECLA classification H01L39/14B.

E39.019 Three or more electrode devices (EPO):
This subclass is indented under subclass E39.012. This subclass is substantially the same in scope as ECLA classification H01L39/14C.

E39.02 Field-effect devices (EPO):
This subclass is indented under subclass E39.019. This subclass is substantially the same in scope as ECLA classification H01L39/14C2.

E43.001 SEMICONDUCTOR OR SOLID-STATE DEVICES USING GALVANO-MAGNETIC OR SIMILAR MAGNETIC EFFECTS, PROCESSES, OR APPARATUS PECULIAR TO MANUFACTURE OR TREATMENT OF SUCH DEVICES, OR OF PARTS THEREOF (EPO):
This main group provides for semiconductor or solid state devices which respond to a magnetic field signal, processes or apparatus specially adapted for the manufacture or treatment of such devices, or of parts thereof. This subclass is substantially the same in scope as ECLA classification H01L43/00.

E43.002 Hall-effect devices (EPO):
This subclass is indented under subclass E43.43.001 This subclass is substantially the same in scope as ECLA classification H01L43/06.

E43.003 Semiconductor Hall-effect devices (EPO):
This subclass is indented under subclass E43.002. This subclass is substantially the same in scope as ECLA classification H01L43/06B.

E43.004 Magnetic-field-controlled resistors (EPO):
This subclass is indented under subclass E43.001. This subclass is substantially the same in scope as ECLA classification H01L43/08.

E43.005 Selection of materials (EPO):
This subclass is indented under subclass E43.001. This subclass is substantially the same in scope as ECLA classification H01L43/10.

E43.006 Processes or apparatus peculiar to manufacture or treatment of these devices or of parts thereof (EPO):
This subclass is indented under subclass E43.001. This subclass is substantially the same in scope as ECLA classification H01L43/12.

E43.007 For Hall-effect devices (EPO):
This subclass is indented under subclass E43.006. This subclass is substantially the same in scope as ECLA classification H01L43/14.

E45.001 SOLID-STATE DEVICES ADAPTED FOR RECTIFYING, AMPLIFYING, OSCILLATING, OR SWITCHING WITHOUT POTENTIAL-JUMP BARRIER OR SURFACE BARRIER, E.G., DIELECTRIC TRIODES; OVSHINSKY-EFFECT DEVICES, PROCESSES, OR APPARATUS PECULIAR TO MANUFACTURE OR TREATMENT THEREOF, OR OF PARTS THEREOF (EPO):
This main group provides for solid state devices which change from non-conductive state to semiconductive state to achieve rectification, amplification, oscillation or switching action, upon application of a minimum voltage, and processes or apparatus peculiar to the manufacture or treatment thereof or of parts thereof. This subclass is substantially the same in scope as ECLA classification H01L45/00.

SEE OR SEARCH THIS CLASS, SUBCLASS:
E29.001, for semiconductors devices adapted for rectifying, amplifying, oscillating, or switching, capacitors, or resistors with at least one potential-jump barrier or surface barrier.

E45.002 Bistable switching devices, e.g., Ovshinsky-effect devices (EPO):
This subclass is indented under subclass E45.001. This subclass is substantially the same in scope as ECLA classification H01L45/00B.

E45.003 Switching materials being oxides or nitrides (EPO):
This subclass is indented under subclass E45.002. This subclass is substantially the same in scope as ECLA classification H01L45/00B2.

E45.004 N: Light-controlled Ovshinsky devices (EPO):
This subclass is indented under subclass E45.002. This subclass is substantially the same in scope as ECLA classification H01L45/00B3.

E45.005 Charge density wave transport devices (EPO):
This subclass is indented under subclass E45.001. This subclass is substantially the same in scope as ECLA classification H01L45/00C.

E45.006 Solid-state travelling-wave devices (EPO):
This subclass is indented under subclass E45.001. This subclass is substantially the same in scope as ECLA classification H01L45/02.

E47.001 BULK NEGATIVE RESISTANCE EFFECT DEVICES, E.G., GUNN-EFFECT DEVICES, PROCESSES, OR APPARATUS PECULIAR TO MANUFACTURE OR TREATMENT OF SUCH DEVICES, OR OF PARTS THEREOF (EPO)
This main group provides for active devices which exhibit the characteristic of decreasing current rate with increasing applied voltage, processes or apparatus peculiar to the manufacture or treatment of such devices or of parts thereof. This subclass is substantially the same in scope as ECLA classification H01L47/00.

E47.002 Gunn-effect devices or transferred electron devices (EPO):
This subclass is indented under subclass E47.001. This subclass is substantially the same in scope as ECLA classification H01L47/02.

E47.003 Controlled by electromagnetic radiation (EPO):
This subclass is indented under subclass E47.002. This subclass is substantially the same in scope as ECLA classification H01L47/02B.

E47.004 Gunn diodes (EPO):
This subclass is indented under subclass E47.002. This subclass is substantially the same in scope as ECLA classification H01L47/02C.

E47.005 Processes or apparatus peculiar to manufacture or treatment of these devices or of parts thereof (EPO):
This subclass is indented under subclass E47.001. This subclass is substantially the same in scope as ECLA classification H01L47/00B.

E49.001 SOLID-STATE DEVICES WITH AT LEAST ONE POTENTIAL-JUMP BARRIER OR SURFACE BARRIER USING ACTIVE LAYER OF LOWER ELECTRICAL CONDUCTIVITY THAN MATERIAL ADJACENT THERETO AND THROUGH WHICH CARRIER TUNNELING OCCURS, PROCESSES OR APPARATUS PECULIAR TO MANUFACTURE OR TREATMENT OF SUCH DEVICES, OR OF PARTS THEREOF (EPO):
This main group provides for solid state devices with at least one potential-jump barrier or surface barrier using active layer of lower electrical conductivity than the material adjacent thereto, e.g., metal sandwiched between thin or thick film insulator or organic semiconductor material, and through which carrier tunneling occurs, and processes or apparatus adapted for the manufacture or treatment of such devices, or of parts thereof. This subclass is substantially the same in scope as ECLA classification H01L49/00.

E49.002 Devices using Mott metal-insulator transition, e.g., field-effect transistors (EPO):
This subclass is indented under subclass E49.001. This subclass is substantially the same in scope as ECLA classification H01L49/00A.

E49.003 Quantum devices, e.g., quantum interference devices, metal single electron transistor (EPO):
This subclass is indented under subclass E49.001. This subclass is substantially the same in scope as ECLA classification H01L49/00Q.

E49.004 Thin-film or thick-film devices (EPO):
This subclass is indented under subclass E49.001. This subclass is substantially the same in scope as ECLA classification H01L49/02.

E51.001 Organic solid state devices, processes or apparatus peculiar to manufacture or treatment of such devices, or of parts thereof (EPO):
This main group provides for solid state device using organic material or a combination of organic material with other material as active part of the device, processes or apparatus specially adapted for the manufacture or treatment of such devices, or of parts thereof. This subclass is substantially the same in scope as ECLA classification H01L51/00.

E51.002 Structural detail of device (EPO):
This subclass is indented under subclass E51.001. This subclass is substantially the same in scope as ECLA classification H01L51/20.

E51.003 Organic solid-state device adapted for rectifying, amplifying, oscillating, or switching, or capacitors or resistors with potential or surface barrier (EPO):
This subclass is indented under subclass E51.002. This subclass is substantially the same in scope as ECLA classification H01L51/20B.

SEE OR SEARCH THIS CLASS, SUBCLASS:
E29.001,and its indents, for details of other solid-state devices adapted for rectifying, amplifying, oscillating, or switching, or capacitors or resistors with a potential or surface barrier.

E51.004 Controllable by only signal applied to control electrode (e.g., base of bipolar transistor, gate of field-effect transistor) (EPO):
This subclass is indented under subclass E51.003. This subclass is substantially the same in scope as ECLA classification H01L51/20B2.

E51.005 Field-effect device (e.g., TFT, FET) (EPO):
This subclass is indented under subclass E51.004. This subclass is substantially the same in scope as ECLA classification H01L51/20B2B.

E51.006 Insulated gate field-effect transistor (EPO):
This subclass is indented under subclass E51.005. This subclass is substantially the same in scope as ECLA classification H01L51/20B2B2.

E51.007 Comprising organic gate dielectric (EPO):
This subclass is indented under subclass E51.006. This subclass is substantially the same in scope as ECLA classification H01L51/20B2B2B.

E51.008 Controllable only by variation of electric current supplied or only electric potential applied to electrode carrying current to be rectified, amplified, oscillated, or switched (e.g., two terminal device) (EPO):
This subclass is indented under subclass E51.003. This subclass is substantially the same in scope as ECLA classification H01L51/20B4.

E51.009 Comprising Schottky junction (EPO):
This subclass is indented under subclass E51.008. This subclass is substantially the same in scope as ECLA classification H01L51/20B4B.

E51.01 Comprising organic/organic junction (e.g., heterojunction) (EPO):
This subclass is indented under subclass E51.008. This subclass is substantially the same in scope as ECLA classification H01L51/20B4D.

E51.011 Comprising organic/inorganic heterojunction (EPO):
This subclass is indented under subclass E51.008. This subclass is substantially the same in scope as ECLA classification H01L51/20B4F.

E51.012 Radiation-sensitive organic solid-state device (EPO):
Subject matter under subclass E51.002 wherein the solid-state device is responsive or sensitive to electromagnetic radiation (e.g., infrared radiation), adapted for a conversion of the radiation into electrical energy or for a control of electrical energy by such radiation. This subclass is substantially the same in scope as ECLA classification H01L51/20C.

SEE OR SEARCH THIS CLASS, SUBCLASS:
E31.001,and its indents, for other radiation-sensitive semiconductor devices.

E51.013 Metal-organic semiconductor-metal device (EPO):
This subclass is indented under subclass E51.012. This subclass is substantially the same in scope as ECLA classification H01L51/20C2.

E51.014 Comprising bulk heterojunction (EPO):
This subclass is indented under subclass E51.012. This subclass is substantially the same in scope as ECLA classification H01L51/20C8.

E51.015 Comprising organic/inorganic heterojunction (EPO):
This subclass is indented under subclass E51.012. This subclass is substantially the same in scope as ECLA classification H01L51/20C4.

E51.016 Majority carrier device using sensitization of wide band gap semiconductor (e.g., TiO_2) (EPO):
This subclass is indented under subclass E51.015. This subclass is substantially the same in scope as ECLA classification H01L51/20C4B.

E51.017 Comprising organic semiconductor-organic semiconductor heterojunction (EPO):
This subclass is indented under subclass E51.012. This subclass is substantially the same in scope as ECLA classification H01L51/20C6.

E51.018 Light-emitting organic solid-state device with potential or surface barrier (EPO):
Subject matter under subclass E51.002 wherein the solid-state device having a potential or surface barrier is adapted for generating light. This subclass is substantially the same in scope as ECLA classification H01L51/20D.

SEE OR SEARCH THIS CLASS, SUBCLASS:
E33.001,and its indents, for other light-emitting semiconductor devices.

E51.019 Electrode (EPO):
This subclass is indented under subclass E51.018. This subclass is substantially the same in scope as ECLA classification H01L51/20D2B.

E51.02 Encapsulation (EPO):
This subclass is indented under subclass E51.019. This subclass is substantially the same in scope as ECLA classification H01L51/20D2C.

SEE OR SEARCH THIS CLASS, SUBCLASS:
E31.117,for encapsulation of other radiation-sensitive semiconductor devices.
E33.059,for encapsulation of other light-emitting semiconductor devices.

E51.021 Arrangements for extracting light from device (e.g., Bragg reflector pair) (EPO):
This subclass is indented under subclass E51.019. This subclass is substantially the same in scope as ECLA classification H01L51/20D2D.

E51.022 Multicolor organic light-emitting device (OLED) (EPO):
This subclass is indented under subclass E51.018. This subclass is substantially the same in scope as ECLA classification H01L51/20D4.

E51.023 Molecular electronic device (EPO):
This subclass is indented under subclass E51.002. This subclass is substantially the same in scope as ECLA classification H01L51/20F.

E51.024 Selection of material for organic solid-state device (EPO):
This subclass is indented under subclass E51.001. This subclass is substantially the same in scope as ECLA classification H01L51/30.

E51.025 For organic solid-state device adapted for rectifying, amplifying, oscillating, or switching, or capacitors or resistors with potential or surface barrier (EPO):
This subclass is indented under subclass E51.024. This subclass is substantially the same in scope as ECLA classification H01L51/30B.

E51.026 For radiation-sensitive or light-emitting organic solid-state device with potential or surface barrier (EPO):
This subclass is indented under subclass E51.024. This subclass is substantially the same in scope as ECLA classification H01L51/30C.

E51.027 Organic polymer or oligomer (EPO):
This subclass is indented under subclass E51.024. This subclass is substantially the same in scope as ECLA classification H01L51/30D.

E51.028 Comprising aromatic, heteroaromatic, or arrylic chains (e.g., polyaniline, polyphenylene, polyphenylene vinylene) (EPO):
This subclass is indented under subclass E51.027. This subclass is substantially the same in scope as ECLA classification H01L51/30D2.

E51.029 Heteroaromatic compound comprising sulfur or selene (e.g., polythiophene) (EPO):
This subclass is indented under subclass E51.028. This subclass is substantially the same in scope as ECLA classification H01L51/30D2B.

E51.03 Polyethylene dioxythiophene and derivative (EPO):
This subclass is indented under subclass E51.029. This subclass is substantially the same in scope as ECLA classification H01L51/30D2B2.

E51.031 Polyphenylenevinylene and derivatives (EPO):
This subclass is indented under subclass E51.028. This subclass is substantially the same in scope as ECLA classification H01L51/30D2D.

E51.032 Polyflurorene and derivative (EPO):
This subclass is indented under subclass E51.028. This subclass is substantially the same in scope as ECLA classification H01L51/30D2F.

E51.033 Comprising aliphatic or olefinic chains (e.g., polyN-vinylcarbazol, PVC, PTFE) (EPO):
This subclass is indented under subclass E51.027. This subclass is substantially the same in scope as ECLA classification H01L51/30D4.

E51.034 Polyacetylene or derivatives (EPO):
This subclass is indented under subclass E51.033. This subclass is substantially the same in scope as ECLA classification H01L51/30D4B.

E51.035 PolyN-vinylcarbazol and derivative (EPO):
This subclass is indented under subclass E51.033. This subclass is substantially the same in scope as ECLA classification H01L51/30D4D.

E51.036 Copolymers (EPO):
This subclass is indented under subclass E51.027. This subclass is substantially the same in scope as ECLA classification H01L51/30D6.

E51.037 Ladder-type polymer (EPO):
This subclass is indented under subclass E51.027. This subclass is substantially the same in scope as ECLA classification H01L51/30D8.

E51.038 Carbon-containing materials (EPO):
This subclass is indented under subclass E51.024. This subclass is substantially the same in scope as ECLA classification H01L51/30F.

E51.039 Fullerenes (EPO):
This subclass is indented under subclass E51.038. This subclass is substantially the same in scope as ECLA classification H01L51/30F2.

E51.04 Carbon nanotubes (EPO):
This subclass is indented under subclass E51.038. This subclass is substantially the same in scope as ECLA classification H01L51/30F4.

E51.041 Coordination compound (e.g., porphyrin, phthalocyanine, metal(II) polypyridine complexes) (EPO):
This subclass is indented under subclass E51.024. This subclass is substantially the same in scope as ECLA classification H01L51/30M.

E51.042 Phthalocyanine (EPO):
This subclass is indented under subclass E51.041. This subclass is substantially the same in scope as ECLA classification H01L51/30M2.

E51.043 Metal complexes comprising Group IIIB metal (Al, Ga, In, or Ti) (e.g., Tris (8-hydroxyquinoline) aluminium (Alq3)) (EPO):
This subclass is indented under subclass E51.041. This subclass is substantially the same in scope as ECLA classification H01L51/30M4.

E51.044 Transition metal complexes (e.g., Ru(II) polypyridine complexes) (EPO):
This subclass is indented under subclass E51.041. This subclass is substantially the same in scope as ECLA classification H01L51/30M6.

E51.045 Biomolecule or macromolecule (e.g., proteins, ATP, chlorophyl, beta-carotene, lipids, enzymes) (EPO):
This subclass is indented under subclass E51.024. This subclass is substantially the same in scope as ECLA classification H01L51/30P.

E51.046 Silicon-containing organic semiconductor (EPO):
This subclass is indented under subclass E51.024. This subclass is substantially the same in scope as ECLA classification H01L51/30S.

E51.047 Macromolecular system with low molecular weight (e.g., cyanine dyes, coumarine dyes, tetrathiafulvalene) (EPO):
This subclass is indented under subclass E51.024. This subclass is substantially the same in scope as ECLA classification H01L51/30H.

E51.048 Charge transfer complexes (EPO):
This subclass is indented under subclass E51.047. This subclass is substantially the same in scope as ECLA classification H01L51/30H2.

E51.049 Polycondensed aromatic or heteroaromatic compound (e.g., pyrene, perylene, pentacene) (EPO):
This subclass is indented under subclass E51.047. This subclass is substantially the same in scope as ECLA classification H01L51/30H4.

E51.05 Aromatic compound containing heteroatom (e.g., perylenetetracarboxylic dianhydride, perylene tetracarboxylic diimide) (EPO):
This subclass is indented under subclass E51.049. This subclass is substantially the same in scope as ECLA classification H01L51/30H4B.

E51.051 Amine compound having at least two aryl on amine-nitrogen atom (e.g., triphenylamine) (EPO):
This subclass is indented under subclass E51.047. This subclass is substantially the same in scope as ECLA classification H01L51/30H6.

E51.052 Langmuir Blodgett film (EPO):
This subclass is indented under subclass E51.024. This subclass is substantially the same in scope as ECLA classification H01L51/30L.

CROSS-REFERENCE ART COLLECTIONS

900 MOSFET TYPE GATE SIDEWALL INSULATING SPACER:
Subject matter wherein a metal oxide semiconductor field effect transistor with a gate electrode includes a relatively thick layer of electrically insulating material along the side wall of the gate electrode and wherein the source or drain region of the transistor has a distinct portion which is distant from the gate electrode and is aligned with the edge of the insulating material, so that the source or drain region is spaced from the gate electrode by the thickness of the insulating material.

901 MOSFET SUBSTRATE BIAS:
Subject matter wherein an electrical bias is applied between the substrate and the source electrode of a metal oxide field effect transistor.

SEE OR SEARCH THIS CLASS, SUBCLASS:
299, for an insulated gate capacitor, or transistor combined with capacitor, with a substrate bias generator.

902 FET WITH METAL SOURCE REGION:
Subject matter including a field effect transistor with a source region that comprises a metal material (e.g., a Schottky barrier or ohmic contact to the channel region).

903 FET CONFIGURATION ADAPTED FOR USE AS STATIC MEMORY CELL:
Subject matter wherein a field effect transistor is structurally arranged to be used in a static memory element (i.e., one in which information need not be periodically refreshed).

904 WITH PASSIVE COMPONENTS, (e.g., POLYSILICON RESISTORS):
This subclass is indented under subclass 903. Subject matter including a solid-state electronic part/component in which charge carriers do not change their energy levels and that does not provide rectification, amplification, or switching, but which does react to voltage and current. Examples are pure resistors, capacitors and inductors.

905 PLURAL DRAM CELLS SHARE COMMON CONTACT OR COMMON TRENCH:
Subject matter comprising plural dynamic random access memory elements which share an electrical contact or trench.

906 DRAM WITH CAPACITOR ELECTRODES USED FOR ACCESSING (E.G., BIT LINE IS CAPACITOR PLATE):
Subject matter comprising a dynamic random access memory element having an electrode which forms one plate of a storage capacitor, which electrode is adapted to be supplied with varying electrical signals to get information into or out of the memory element.

907 FOLDED BIT LINE DRAM CONFIGURATION:
Subject matter comprising an array of dynamic random access memory elements including differential sense amplifiers each connected to two different rows of memory cells, wherein the two rows of memory cells connected to a specific sense amplifier lie adjacent and parallel to each other on the same side of the sense amplifier.

908 DRAM CONFIGURATION WITH TRANSISTORS AND CAPACITORS OF PAIRS OF CELLS ALONG A STRAIGHT LINE BETWEEN ADJACENT BIT LINES:
Subject matter comprising dynamic random access memory elements having transistors and capacitors, where memory elements connected to adjacent bit lines have transistors and capacitors which are not staggered but which lie along a straight line which is located between the adjacent bit lines of the device.

909 MACROCELL ARRAYS (E.G., GATE ARRAYS WITH VARIABLE SIZE OR CONFIGURATION OF CELLS):
Subject matter comprising plural geometric arrangements of groups of active solid-state devices, each group being connectable into a logic circuit, in one integrated, monolithic semiconductor chip. in which different groups differ from each other in size, complexity, or number of components.

910 DIODE ARRAYS (E.G., DIODE READ-ONLY MEMORY ARRAY):
A repeating geometric arrangement of electronic devices which have two terminals and an asymmetrical or nonlinear voltage-current characteristic.

911 LIGHT SENSITIVE ARRAY ADAPTED TO BE SCANNED BY ELECTRON BEAM (E.G.,VIDICON DEVICE):
A repeating geometric arrangement of light sensitive devices structured to be scanned by an electron beam.

912 CHARGE TRANSFER DEVICE USING BOTH ELECTRON AND HOLE SIGNAL CARRIERS:
Subject matter wherein a charge transfer device* uses both electron and hole carriers in the same transfer or storage regions of the charge transfer device.

913 WITH MEANS TO ABSORB OR LOCALIZE UNWANTED IMPURITIES OR DEFECTS FROM SEMICONDUCTORS (E.G., HEAVY METAL GETTERING):
Subject matter including a semiconductor device having means to absorb or localize semiconductor impurities or defects which would adversely affect the performance of the device, e.g., phosphosilicate glass coating to absorb deep level impurities.

914 POLYSILICON CONTAINING OXYGEN, NITROGEN, OR CARBON (E.G., SIPOS):
Subject matter comprising polycrystalline silicon which contains oxygen, nitrogen, or carbon.

915 WITH TITANIUM NITRIDE PORTION OR REGION:
Subject matter wherein an active solid-state device includes a portion or region of the device which contains titanium nitride.

916 NARROW BAND GAP SEMICONDUCTOR MATERIAL (<<1eV):
Subject matter wherein an active solid-state device material is a semiconductor in which the difference between the energy levels of electrons bound to their nuclei (valence electrons) and the energy levels that allow electrons to migrate freely (conduction electrons) is less than one electron volt.

917 PLURAL DOPANTS OF SAME CONDUCTIVITY TYPE IN SAME REGION:
Subject matter wherein an active solid-state device has a region or portion which contains at least two different impurity elements which

have the same electrical conductivity type (i.e., both p-type or both n-type).

918 LIGHT EMITTING REGENERATIVE SWITCHING DEVICE (E.G., LIGHT EMITTING SCR) ARRAYS, CIRCUITRY, ETC.:
Subject matter wherein an active solid-state device acts as if it has two or more active emitter junctions each of which is associated with a separate, equivalent transistor having an individual gain and, when initiated by a base region* current, the equivalent transistors mutually drive each other in a regenerative manner to lower the voltage drop between the emitters, and which active solid-state device can generate light.

(1) Note. If the current is above a level IH, called the "holding current*", then the device will remain ON when the triggering signal is removed by the regenerative feedback therebetween, and is then said to be "latched*".

919 ELEMENTS OF SIMILAR CONSTRUCTION CONNECTED IN SERIES OR PARALLEL TO AVERAGE OUT MANUFACTURING VARIATIONS IN CHARACTERISTICS:
Subject matter comprising devices wherein components or portions or regions of the devices having similar structure are electrically connected in series or parallel to average out manufacturing variations in their operational characteristics.

920 CONDUCTOR LAYERS ON DIFFERENT LEVELS CONNECTED IN PARALLEL (E.G., TO REDUCE RESISTANCE):
Subject matter wherein a device contains layers of electrical conductors and different conductor layers are electrically connected in parallel, to improve device operation (e.g., to reduce conductor resistance).

921 RADIATION HARDENED SEMICONDUCTOR DEVICE:
Subject matter in which an active solid-state device is provided with means to render it relatively less susceptible to being damaged or deleteriously affected in any way by radiant energy (e.g., alpha particles).

SEE OR SEARCH THIS CLASS, SUBCLASS:
659+, for means to shield active solid-state devices from harmful radiation.

922 WITH MEANS TO PREVENT INSPECTION OF OR TAMPERING WITH AN INTEGRATED CIRCUIT (E.G., "SMART CARD", ANTI-TAMPER):
Subject matter comprising an integrated circuit with means to prevent inspection of, or tampering with the integrated circuit (e.g., an integrated circuit used in a "smart card" credit or bank card).

923 WITH MEANS TO OPTIMIZE ELECTRICAL CONDUCTOR CURRENT CARRYING CAPACITY (E.G., PARTICULAR CONDUCTOR ASPECT RATIO):
Subject matter in which an active solid-state device includes means to optimize the current carrying capacity of an electrical conductor of the device, e.g., by using a particular conductor cross-sectional configuration.

924 WITH PASSIVE DEVICE (E.G., CAPACITOR), OR BATTERY, AS INTEGRAL PART OF HOUSING OR HOUSING ELEMENT (E.G., CAP):
Subject matter which includes a distinct solid-state electronic device in which charge carriers do not change their energy levels and that does not provide rectification, amplification or switching, but which does react to voltage and current (e.g., resistors, capacitors, and inductors), or contains a battery, as an integral part of a housing or housing element for an active solid-state device.

925 BRIDGE RECTIFIER MODULE:
Subject matter comprising a self-contained element which includes two or more junction diodes structurally interconnected as a rectifier bridge circuit.

926 ELONGATED LEAD EXTENDING AXIALLY THROUGH ANOTHER ELONGATED LEAD:
Subject matter wherein an active solid-state device includes more than one electrical lead wherein one relatively long lead is coaxially located within another relatively long lead.

927 DIFFERENT DOPING LEVELS IN DIFFERENT PARTS OF PN JUNCTION TO PRODUCE SHAPED DEPLETION LAYER:

Subject matter wherein a pn junction device contains impurity dopants with differing concentrations of dopant in different parts of the PN junction such that a depletion region associated with the PN junction has a controlled shape.

928 WITH SHORTED PN OR SCHOTTKY JUNCTION OTHER THAN EMITTER JUNCTION:

Subject matter wherein a device has a pn or Schottky junction electrode which is electrically short circuited (i.e., there is a direct connection to both sides of the junction).

929 PN JUNCTION ISOLATED INTEGRATED CIRCUIT WITH ISOLATION WALLS HAVING MINIMUM DOPANT CONCENTRATION AT INTERMEDIATE DEPTH IN EPITAXIAL LAYER (E.G., DIFFUSED FROM BOTH SURFACES OF EPITAXIAL LAYER):

Subject matter comprising an integrated circuit with pn junction isolation and having boundary walls isolating the integrated circuit from its substrate, wherein the walls have a minimum concentration of dopant at an intermediate depth in an epitaxial layer substrate (e.g., diffused from both surfaces of an epitaxial layer).

930 THERMOELECTRIC (E.G., PELTIER EFFECT) COOLING:

Subject matter comprising means thermally connected to an active solid-state device which, when subjected to the application of an electric or magnetic field or electric current, causes heat to be absorbed and thereby to cool the active solid-state device.

END