The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 20

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte JAY B. RICKARD
and
FARID YAZDY

Appeal No. 1999-2258
Application No. 08/431,720

ON BRIEF

Before HAIRSTON, BARRY, and BLANKENSHIP, Administrative Patent Judges.

HAIRSTON, Administrative Patent Judge.

DECISION ON APPEAL

This is an appeal from the final rejection of claims 1 through 14.

The disclosed invention relates to a hardware graphics accelerator used in a computer system that has a memory subsystem that comprises main memory and video memory. The hardware graphics accelerator includes a datapath circuit that

receives data from either the main memory or the video memory and performs a graphics operation on the data, and a memory controller that controls the memory subsystem so that at one time the datapath circuit receives the data from the main memory and at another time the datapath circuit receives the data from the video memory.

Claim 1 is the only independent claim on appeal, and it reads as follows:

> 1. For use in a computer system having a data processor, a system bus, and a memory subsystem comprising main memory and video memory, a hardware graphics accelerator comprising:
>
> a datapath circuit connected to the system bus and to the memory subsystem for receiving data from the memory subsystem, performing a graphics operation upon the data, and returning the data to the memory subsystem; and
>
> a memory controller connected to the system bus, to the datapath circuit, and to the memory subsystem for controlling the memory subsystem such that at one time the datapath circuit receives the data from the main memory and at another time the datapath circuit receives the data from the video memory.

The reference relied on by the examiner is:

Lehman et al. (Lehman) 5,450,542 Sep. 12, 1995 (filed Nov. 30, 1993)

Claims 1 through 14 stand rejected under 35 U.S.C. §

102(e) as being anticipated by Lehman.

Reference is made to the briefs (paper numbers 15 and 17) and the answer (paper number 16) for the respective positions of the appellants and the examiner.

OPINION

We have carefully considered the entire record before us, and we will reverse the 35 U.S.C. § 102(e) rejection of claims 1 through 14.

To anticipate a claim, a prior art reference must disclose every limitation of the claimed invention, either explicitly or inherently. See Glaxo Inc. v. Novopharm Ltd., 52 F.3d 1043, 1047, 34 USPQ2d 1565, 1567 (Fed. Cir.), cert. denied, 516 U.S. 3378 (1995). The examiner's rejection of claim 1 is as follows (answer, pages 3 and 4):

> Regarding claim 1, Lehman et al.'s BUS INTERFACE WITH GRAPHICS AND SYSTEM PATHS FOR AN INTEGRATED MEMORY SYSTEM discloses a computer system having a data processor 302, "a system bus 500", and "a memory subsystem bus 408" comprising main memory and video memory 114, a hardware graphics accelerator comprising a "data path circuit 407 connected to the system bus to the memory and to the memory subsystem", as in fig[.] 4; for receiving data from the memory subsystem, performing a graphics operation upon the data, and returning to the memory subsystem (see col[.] 8, lines 18-40 and figure 4); and a memory controller 316 connect[ed] to the system bus, to the datapath circuit, and to the memory subsystem for controlling the memory

> subsystem such that at one time the datapath circuit receives the data from the video memory (see col[s.] 5-6, lines 10-65 and figures 3, 5).

Appellants argue (brief, page 7) that:

> Lehman discloses two separate paths and two distinct address ranges for each of the graphics and main memory accesses. As a result, Lehman's graphics circuitry (e.g.[,] ACCEL 414, PIXEL LOGIC 416, etc.) has no access to main memory data since as can be seen in Figure 4, graphics data, having a particular address range, is only routed through the graphics circuitry portion of controller 400 between bus 405 and the memory interface 408. Main memory data, having a different address range than the video data, passes through a separate route from memory interface 408 to bus interface 500 on bus 407 and bypasses the graphics circuitry. As a result, Lehman's graphics circuitry cannot perform any graphics operations on data from main memory.

In response to the examiner's statement (answer, page 6) that the shared memory 304 (Figure 3) "can be concurrently used, and dynamically reconfigured for both graphics and system function[s] as claimed," appellants argue (reply brief, page 3) that "[r]egardless of how the memory is configured, shared, or concurrently used, the graphics data and system data still follow their exclusive paths dictated by Lehman's underlying architectural structure and function (column 5, lines 15-26) and Lehman's clear division in address ranges between the

graphics and system memory (column 9, lines 40-43)." In summary, appellants argue (reply brief, page 3) that:

> Lehman does not teach a system that "at one time the datapath circuit receives data from the main memory and at another time the data path circuit receives the data from the video memory" (Claim 1). Lehman instead routes graphics and system data through separate buses having separate address ranges making it physically impossible for Lehman's graphics circuitry to receive data from the main memory at one time and at another time data from video memory.

We agree with appellants' arguments. Thus, the 35 U.S.C. § 102(e) rejection of claims 1 through 14 is reversed because the "datapath circuit" disclosed by Lehman is incapable of receiving data from main memory for graphics processing.

DECISION

The decision of the examiner rejecting claims 1 through 14 under 35 U.S.C. § 102(e) is reversed.

REVERSED

KENNETH W. HAIRSTON Administrative Patent Judge	)	
LANCE LEONARD BARRY Administrative Patent Judge	)	BOARD OF PATENT APPEALS AND INTERFERENCES
HOWARD B. BLANKENSHIP Administrative Patent Judge	)	

KWH:hh

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