

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 33

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte HIDEKI YAMANAKA
and SEIJI HINATA

Appeal No. 1999-2256
Application No. 08/686,477

HEARD: October 16, 2001

Before JERRY SMITH, RUGGIERO, and BARRY, Administrative Patent Judges.

BARRY, Administrative Patent Judge.

DECISION ON APPEAL

The examiner rejected the appellants' claims 1-6 and 9-24. They appeal therefrom under 35 U.S.C. § 134(a). We reverse.

BACKGROUND

The invention at issue in this appeal relates to a "watch dog timer" for a microprocessor-based system. A watch dog

timer sets a time-out value for a program being executed by a microprocessor-based system. When the program is operating normally, a central processing unit ("CPU") sends a signal via the system's bus to reset the timer before the latter "overflows," i.e., reaches the time-out value. When an abnormality such as a program runaway occurs, in contrast, the CPU does not reset the timer. Accordingly, the timer overflows, and an overflow signal is transmitted to the CPU and other devices in the system.

A problem occurs when using a watch dog timer in a microprocessor-based system that includes a bus master such as a direct memory access controller ("DMAC"). Specifically, when the DMAC uses the system's bus for a direct memory access ("DMA") transfer, the system's CPU cannot use the bus to send a reset signal, and the timer overflows.

According to the appellants' invention, when a DMA transfer is needed, the DMAC issues a request to the system's CPU. After processing the request, the CPU issues a bus permission signal to both the watch dog timer and the DMAC.

Responsive to the bus permission signal, the watch dog timer is stopped and the DMA transfer is done.

Claim 21, which is representative for present purposes, follows:

21. A watch dog timer device comprising:

a runaway detection circuit for counting a count clock signal and outputting a reset signal when overflow is caused; and

a count clock controller for supplying said count clock signal to said runaway detection circuit, receiving a bus permission signal from a CPU and halting the supplying of said count clock signal to said runaway detection circuit when said bus permission signal is received.

The prior art applied by the examiner in rejecting the claims follows:

Richardson et al. ("Richardson") 4,131,945 Dec. 26, 1978

Mager et al. ("Mager") 4,137,565 Jan. 30, 1979

Loftis et al. ("Loftis") 5,185,693 Feb. 9, 1993

Carr, Microprocessor Interfacing 11, 17 (1982).

Claims 1, 2, 4-6, 9-21 stand rejected under 35 U.S.C. § 103 as obvious over Mager in view of Loftis. Claim 3 stands rejected under § 103 as obvious over Mager in view of Loftis further in view of Carr. Claims 22-24 stand rejected under 35 U.S.C. §102(b) as anticipated by Richardson. Rather than reiterate the arguments of the appellants or examiner in toto, we refer the reader to the briefs and answer for the respective details thereof.

OPINION

After considering the record, we are persuaded that the examiner erred in rejecting claims 1-6 and 9-24. Accordingly, we reverse. We consider the obviousness of the following logical groups of claims:

- claims 1, 2, 3, 9, and 21
- claims 4, 5, 6, 10
- claims 11-20
- claims 22-24.

We begin with the first group of claims.

I. Claims 1, 2, 3, 9, and 21

The examiner asserts, "Mager teaches ... halting [27:50, e.g., 'indefinite reset'] the supplying of the count clock signal to the runaway detection circuit when the bus permission signal is received." (Examiner's Answer at 3.) The appellants argue, "[t]here is simply no disclosure or suggestion anywhere within Mager et al that the clock signal is halted" (Reply Br. at 2.)

In deciding obviousness, "[a]nalysis begins with a key legal question -- *what is the invention claimed?*" Panduit Corp. v. Dennison Mfg. Co., 810 F.2d 1561, 1567, 1 USPQ2d 1593, 1597 (Fed. Cir. 1987). "Claim interpretation ... will normally control the remainder of the decisional process." Id. at 1567-68, 1 USPQ2d at 1597. Here, claims 1 and 9 specify in pertinent part the following limitations: "count clock control means for receiving said count clock signal transmitted from a second external device and transmitting said count clock signal to said watch dog timer means, and for halting a transmission of said count clock signal transmitted from an external device to said watch dog timer means when said CPU transmits a bus permission signal to said DMAC for

using said bus by said DMAC." Similarly, claim 2 specifies in pertinent part the following limitations: "count clock control means for receiving said count clock signal transmitted from a second external device and transmitting said count clock signal to said watch dog timer means, and for halting a transmission of said count clock signal transmitted from an external device to said watch dog timer means under a condition that said DMAC uses said bus." Accordingly, the limitations of claims 1, 2, and 9 require inter alia halting the supply of a count clock signal to a watch dog timer because a DMAC is using a system bus.

Claim 21 specifies in pertinent part the following limitations: "a count clock controller for supplying said count clock signal to said runaway detection circuit, receiving a bus permission signal from a CPU and halting the supplying of said count clock signal to said runaway detection circuit when said bus permission signal is received." Accordingly, the limitations require inter alia halting the supply of a count clock signal to a runaway detection circuit because a bus permission signal has been issued by a CPU.

Having determined what subject matter is being claimed, the next inquiry is whether the subject matter is obvious. "A prima facie case of obviousness is established when the teachings from the prior art itself would appear to have suggested the claimed subject matter to a person of ordinary skill in the art.'" In re Bell, 991 F.2d 781, 782, 26 USPQ2d 1529, 1531 (Fed. Cir. 1993) (quoting In re Rinehart, 531 F.2d 1048, 1051, 189 USPQ 143, 147 (CCPA 1976)).

Here, as noted by the examiner, Mager does place "a binary counter **2900** operative to receive a clock signal of 154kc on **2905** from a source ... at terminal 'CLK,'" col. 26, ll. 13-16, in a state of indefinite reset. Specifically, "[c]oncurrent receipt of a D0 signal from data bus **195A** and a CPU command signal on line **3100** by AND gate **3120** will enable outputting [sic] thereof on line **3125** thereby putting time **2900** in indefinite reset and locking out fault detection until the data bus D0 signal is removed." Col. 27, ll. 47-51. The examiner fails to show, however, that placing the binary counter in the state of indefinite reset halts the supply of

the clock signal thereto. To the contrary, Figure 24 of the reference shows that the clock signal 2905 continues to be applied to the binary counter's CLK terminal.

Relying on Loftis to allegedly "disclose[s] a 'bus permission signal,'" (Examiner's Answer at 4), and Carr to disclose "two NOR gates configured as a flip-flop," (*id.* at 8), the examiner fails to allege, let alone show, that the additional reference cures the defect of Mager. Because the latter reference's clock signal is applied to its binary counter even in the state of indefinite reset, we are not persuaded that the teachings from the applied prior art would have suggested the limitations of "count clock control means for receiving said count clock signal transmitted from a second external device and transmitting said count clock signal to said watch dog timer means, and for halting a transmission of said count clock signal transmitted from an external device to said watch dog timer means when said CPU transmits a bus permission signal to said DMAC for using said bus by said DMAC," "count clock control means for receiving

said count clock signal transmitted from a second external device and transmitting said count clock signal to said watch dog timer means, and for halting a transmission of said count clock signal transmitted from an external device to said watch dog timer means under a condition that said DMAC uses said bus," or "a count clock controller for supplying said count clock signal to said runaway detection circuit, receiving a bus permission signal from a CPU and halting the supplying of said count clock signal to said runaway detection circuit when said bus permission signal is received." Therefore, we reverse the rejection of claims 1, 2, 9, and 21 and of claim 3, which depends from claim 1. We proceed to the second group of claims.

II. Claims 4, 5, 6, and 10

The examiner asserts, "*Mager explicitly teaches that binary counter 2900 (contained in watch dog timer 105) will be reset upon receipt of a signal by OR gate 3025 on line 104 indicating that a normal condition of a direct memory access*"

is currently being performed [col. 27, lines 1-5]."

(Examiner's Answer at 5.) The appellants argue, "[t]here is no disclosure or suggestion of such structure which is the same or equivalent to the structure disclosed in the specification which resets the watch dog timer means while said DMA uses said bus." (Appeal Br. at 12.) When asked about claim 10 at oral hearing, moreover, the appellants' counsel emphasized that the claim included means-plus-function language.

"[O]ne construing means-plus-function language in a claim must look to the specification and interpret that language in light of the corresponding structure, material, or acts described therein, and equivalents thereof, to the extent that the specification provides such disclosure." In re Donaldson Co., 16 F.3d 1189, 1193, 29 USPQ2d 1845, 1848 (Fed. Cir. 1994) (en banc). Here, claim 4 specifies in pertinent part the following limitations: "timer control means for resetting said watch dog timer means when said CPU transmits a bus permission signal to said DMAC for using said bus." Similarly, claims 5 and 10 specify in pertinent part the

following limitations: "timer control means for resetting said watch dog timer means while said DMAC uses said bus."

The appellants' specification describes the timer control means as "an AND circuit." (Spec. at 13) More specifically, "bus permission signal S5 is supplied to one input terminal of an AND circuit 74, and then the output from the AND circuit 74 is transmitted to a forced reset terminal R of the runaway control circuit [72]" (Id.) Figure 7 of the specification, furthermore, shows that a "control signal from CPU" is supplied to the other input terminal of the AND circuit. Interpreting claims 4, 5, and 10 in light of the corresponding structure described in the specification, the limitations require inter alia an AND gate receiving a CPU's control signal and bus permission signal and its outputting a forced reset signal to a runaway control circuit when the CPU transmits the bus permission signal or when a DMAC uses a system bus.

"In rejecting claims under 35 U.S.C. Section 103, the examiner bears the initial burden of presenting a prima facie

case of obviousness." In re Rijckaert, 9 F.3d 1531, 1532, 28 USPQ2d 1955, 1956 (Fed. Cir. 1993)(citing In re Oetiker, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992)). "If examination at the initial stage does not produce a prima facie case of unpatentability, then without more the applicant is entitled to grant of the patent." Oetiker, 977 F.2d at 1445, 24 USPQ2d at 1444 (citing In re Grabiak, 769 F.2d 729, 733, 226 USPQ 870, 873 (Fed. Cir. 1985) and In re Rinehart, 531 F.2d 1048, 1052, 189 USPQ 143, 147 (CCPA 1976)).

Here, the examiner fails to identify which of the AND gates shown in Figure 24 of the reference he believes discloses or would have suggested an AND gate receiving a CPU's control signal and bus permission signal and its outputting a forced reset signal to a runaway control circuit when the CPU transmits the bus permission signal or when a DMAC uses a system bus. We will not "resort to speculation," In re Warner, 379 F.2d 1011, 1017, 154 USPQ 173, 178 (CCPA 1967), as to his belief. Accordingly, we are not persuaded that the teachings from the applied prior art would have suggested the limitations of "timer control means for

resetting said watch dog timer means when said CPU transmits a bus permission signal to said DMAC for using said bus" or "timer control means for resetting said watch dog timer means while said DMAC uses said bus." Therefore, we reverse the rejection of claims 4, 5, and 10 and of claim 6, which depends from claim 4. We proceed to the third group of claims.

III. Claims 11-20

The examiner asserts, "Mager teaches ... transmitting the count clock signal to the watch dog timer when the CPU transmits a bus permission signal to the DMAC [27:-1-5]." (Examiner's Answer at 5-6.) Regarding claims 11-15, the appellants argue, "[n]o prior art of record, either alone or in combination, discloses this concept of the bus permission signal being received by both the watch dog timer and the DMA controller." (Appeal Br. at 12.) Regarding claims 16-20, they add, "[a]s explained above ... there is or disclosure or suggestion in the prior art of a bus permission line connected between a CPU, a DMA controller, and the watch dog timer." (Id. at 15.)

Claim 11 specifies in pertinent part the following limitations: "issuing a bus permission signal by the CPU; receiving the bus permission signal by the watch dog timer and the DMA controller" Similarly, claim 16 specifies in pertinent part the following limitations: "a bus permission line, different from the control bus, connected between the CPU, the DMA controller, and the watch dog timer" Accordingly, the limitations of claims 11 and 16 respectively require inter alia that a DMAC and a watch dog timer both receive a bus permission signal from a CPU and that a bus permission line, different from a control bus, connects the CPU, the DMAC, and the watch dog timer

The examiner fails to allege, let alone show, that Mager's "fault watch timer or watch dog timer (WDT) module **105** in the IOPM **90** of FIG. 24," col. 26, ll. 7-8, receives a bus permission signal from the reference's "CPU **40** in the central processor unit module **120**," col. 4, ll. 29-30, or is connected thereto by a bus permission line. Accordingly, we are not persuaded that the teachings from the applied prior art would

have suggested the limitations of "issuing a bus permission signal by the CPU [and] receiving the bus permission signal by the watch dog timer and the DMA controller" or "a bus permission line, different from the control bus, connected between the CPU, the DMA controller, and the watch dog timer" Therefore, we reverse the rejection of claim 11 and of claims 12-15, which depend therefrom. We also reverse the rejection of claim 16 and of claims 17-20, which depend therefrom. We proceed to the last group of claims.

IV. Claims 22-24

The examiner asserts, "Richardson teaches the controller halts the supplying of the clock signal to the counter when the controller receives the bus permission signal [see the hold signal, col. 2, lines 10, 11]." (Examiner's Answer at 14.) The appellants argue, "there is no disclosure within Richardson et al of the preventing of an outputting of the reset signal" (Reply Br. at 7.)

In deciding anticipation, "the first inquiry must be into exactly what the claims define." In re Wilder, 429 F.2d 447,

450, 166 USPQ 545, 548 (CCPA 1970). Here, claim 22 specifies in pertinent part the following limitations: "a controller having an input which receives a bus permission signal and an output connected to said runaway detection circuit which prevents outputting by said runaway detection circuit of said reset signal when said input receives the bus permission signal." Accordingly, the limitations require inter alia preventing a runaway detection circuit from outputting a reset signal because a bus permission signal has been issued.

"[H]aving ascertained exactly what subject matter is being claimed, the next inquiry must be into whether such subject matter is novel." Wilder, 429 F.2d at 450, 166 USPQ at 548. "A prior art reference anticipates a claim only if the reference discloses, either expressly or inherently, every limitation of the claim. See Verdegaal Bros., Inc. v. Union Oil Co., 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). '[A]bsence from the reference of any claimed element negates anticipation.'" Rowe v. Dror, 112 F.3d 473, 478, 42 USPQ2d 1550, 1553 (Fed. Cir. 1997)(quoting Kloster Speedsteel

AB v. Crucible, Inc., 793 F.2d 1565, 1571, 230 USPQ 81, 84
(Fed. Cir. 1986)).

Here, in the passage of Richardson on which the examiner relies, a DMA unit suspends operations of a control processor. Specifically, "a direct memory access unit in a controller is operative to receive an enabling address signal on a system bus from a control processor thereby allowing it to issue a hold signal back to the control processor for operational suspension thereof." Col. 2, ll. 7-11. The examiner fails to show that the control processor outputs a reset signal, let alone that the DMA unit prevents the control processor from outputting a reset signal because a bus permission signal has been issued.

Because there is no showing that Richardson's DMA unit prevents the reference's control processor from outputting a reset signal because a bus permission signal has been issued, we are not persuaded that the applied prior art discloses the limitations of "a controller having an input which receives a bus permission signal and an output connected to said runaway

detection circuit which prevents outputting by said runaway detection circuit of said reset signal when said input receives the bus permission signal." Therefore, we reverse the rejection of claim 22 and of claims 23 and 24, which depend therefrom.

CONCLUSION

In summary, the rejection of claims 1-6 and 9-21 under §
103 is reversed. The rejection of claims 22-24 under 35
U.S.C. §102(b) is also reversed.

REVERSED

JERRY SMITH)	
Administrative Patent Judge)	
)	
)	
)	
)	BOARD OF PATENT
JOSEPH F. RUGGIERO)	APPEALS
Administrative Patent Judge)	AND
)	INTERFERENCES
)	
)	
)	
LANCE LEONARD BARRY)	
Administrative Patent Judge)	

Appeal No. 1999-2256
Application No. 08/686,477

Page 20

LLB/kis

OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT
FOURTH FLOOR
1755 JEFFERSON DAVIS HIGHWAY
ARLINGTON, VA 22202