

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 20

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte BURHAN BAYRAKTAROGLU and MIKE L. SALIB

Appeal No. 1999-1850
Application No. 08/870,406

ON BRIEF

Before THOMAS, HAIRSTON, and KRASS, Administrative Patent Judges.

KRASS, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 1-7, all of the pending claims.

The invention is directed to bipolar transistors. More particularly, the invention seeks to improve the thermal stability of heterojunction bipolar transistors by placing current and power generation regions into separate temperature zones. With reference to Figure 2, collectors of

transistors in the common-emitter stage are connected to emitters of transistors in the common-base stage. Since the temperature is uniform, based on the low bias applied, current levels on the collectors in the common-emitter stage are uniform. The collector bias in the common base stage is substantially higher, which results in a higher junction temperature. However, even though there are temperature variations between emitters of the common-base cells, no thermal runaway can occur because the current of each emitter finger is limited by the collector current of the common-emitter cells.

Representative independent claim 1 is reproduced as follows:

1. A device for controlling thermal runaway comprising:
a common-emitter cell and a common-base cell;
each cell having a first subcell and a second subcell;
said first and second subcell of the common emitter cell having at least one transistor;
said first and second subcell of the common-base cell having at least one transistor;
each transistor of the subcells in the common-emitter cell and common-base cell further comprising an emitter, a collector and a base; and
the collectors of each subcell of the common-emitter cell being connected to the emitter of the transistor in the equivalent subcell of the common-base cell.

The examiner relies on the following reference:

Izuhara

5,497,155

Mar. 5, 1996

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Claims 1-5 and 7 stand rejected under 35 U.S.C. 112, second paragraph, as being vague and indefinite.

Claims 1, 2, 6 and 7 stand rejected under 35 U.S.C. 102(b) as anticipated by Izuhara.

Claims 3-5 stand rejected under 35 U.S.C. 103 as unpatentable over Izuhara.

Reference is made to the brief and answer for the respective positions of appellants and the examiner.

OPINION

Turning first to the rejection under 35 U.S.C. 112, second paragraph, it is the examiner's position that in claim 1, lines 4-5, it is not clear whether *each* of the first and second subcells has at least one transistor or whether the first and second subcells, *together*, include at least one transistor.

While the language of the claim could have been clearer¹, it is our view that the artisan, with the instant specification and drawings before him/her, would have understood that *each* of the first and second subcells has at least one transistor. But, even if the claim language is interpreted as meaning that each set of a first and second subcell has "at least one transistor," it would not be inaccurate since the fact that each subcell has at least one transistor means that each set of first and second subcells has *at least* one (viz., two) transistor. In any event, since an artisan can

¹Indeed, appellants attempted to amend the claims to clarify the meaning but the amendment was refused entry by the examiner.

easily determine what comprises the invention and what meaning to give the claimed terms by reference to the disclosure, we find no problem with the cited claim language, within the meaning of

35 U.S.C. 112, second paragraph.

The examiner also contends that it is not clear from the language of claim 1 what is meant by “the equivalent subcell” since this terminology lacks clear antecedent basis. Similarly, the examiner contends that the language “the corresponding subcell” in claim 7 is indefinite.

Again, while the claim language could have been clearer, it is our view that the meaning of these terms is made clear by reference to the instant disclosure. The device comprises a common-emitter cell and a common-base cell. Each of these cells has a first and second subcell. The first subcell of the common-emitter cell “corresponds”, or is equivalent to, the first subcell of the common-base cell which, together with the common-emitter cell, makes up a unit common-emitter/common-base cell arrangement. For example, with reference to instant Figure 2, and the attendant description in the specification, it is clear that the common-emitter stage and common-base stage in the top two boxes comprise a unit and that the collector, 14, of the common-emitter stage is connected to the emitter, 26, of the transistor “in the equivalent subcell” (i.e., the common-base stage that corresponds to the common-emitter stage in question) of the common-base cell.

Accordingly, we will not sustain the rejection of claims 1-5 and 7 under 35 U.S.C. 112, second paragraph.

Turning now, to the rejections based on prior art, we will sustain these rejections.

With regard to the rejection of claims 1, 2, 6 and 7 under 35 U.S.C. 102(b), the examiner contends that this claimed subject matter is anticipated by Izuhara and applies Izuhara to the instant claims as follows:

The examiner makes reference to Figure 12 of Izuhara and notes that transistors Q50 and Q51 comprise a common emitter cell while transistors Q52, Q52N, Q53 and Q53N comprise a common base cell. The claimed subcells read on the transistors of the common emitter and common base cells identified by the examiner in Izuhara. The examiner notes that the claim preambles have not been taken into account since they do not breathe life and meaning into the claims.

It appears to us that the examiner has established a prima facie case of anticipation in the application of Figure 12 of Izuhara to instant claims 1, 2, 6 and 7.

Appellants argue, first, that Izuhara teaches an analog-to-digital converter. This is irrelevant so long as the instant claims are anticipated by something disclosed within Izuhara.

Appellants agree that Izuhara contains transistors arranged in cells (brief-bottom of page 10). However, appellants contend that the examiner has failed to point out that the interconnection of the emitters and bases within each cell are not as claimed by appellants. The examiner has identified the common emitter cell as comprising transistors Q50 and Q51 and the common base cell as comprising transistors Q52, Q52N, Q53 and Q53N. Clearly, each of the transistors in Figure 12 of Izuhara comprises an emitter, a collector and a base. Further, the collector (of Q50,

for example, in the common emitter cell) is connected to the emitter of transistors Q52 and Q53 in the equivalent subcell of the common base cell. This appears to be a fair interpretation of Izuhara and appellants have not disputed it by pointing out how this analysis is in error.

At page 11 of the brief, appellants point out that Izuhara teaches the use of ballast resistors to prevent thermal runaway while the instant claimed invention does not claim any ballast resistors or show any ballast resistors in the associated figures. This argument is not persuasive since the instant claims do not preclude ballast resistors. While we understand that the instant invention was intended to improve upon the prior art by eliminating ballast resistors, such elimination is not required by the instant claims. Moreover, an applied reference may always show *more* than what is claimed but this does not preclude the reference from being a valid anticipatory reference so long as the reference discloses each and every claimed limitation. The examiner has shown that each limitation is met and appellants have pointed to nothing in the claims which is not disclosed by the reference.

Appellants further argue that in the instant invention the collectors are connected to the emitters in the line of the current flow which is said to be a “major difference” between the instant claimed device and Izuhara. However, we find nothing in the instant claims directed to “the line of current flow” and appellants have pointed to no such limitation within the claims. Arguments directed to limitations which do not appear in the claims are not persuasive as they are irrelevant to the instant *claimed* subject matter.

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By way of further explanation, at page 11 of the brief, appellants argue that the instant claims contain far more than just common emitters and bases but set forth how the emitters in the common-emitter cell are connected to the bases of the transistors in the common-base cell in the line of current flow, as opposed to Izuhara which shows the reverse connection, i.e., that a plurality of bases are connected to the emitters in the line of current flow. Whether or not this is a valid difference, this “difference” is not brought out in the instant claims, as there is no mention of “line of current flow.” Appellants point to no specific claim limitations on which they rely for patentability of the claimed subject matter. We find nothing in the instant claims relating to any connections of emitters and *bases*, as now argued by appellants as distinguishing over the prior art.

Since we find none of appellants’ arguments to be convincing of patentability over Izuhara, we will sustain the rejection of claims 1, 2, 6 and 7 under 35 U.S.C. 102(b).

Turning to the rejection of claims 3-5 under 35 U.S.C. 103 over Izuhara, based on the lack of argument at page 12 of the brief, appellants let these claims and the rejection thereof fall with claim 1, rejected under 35 U.S.C. 102(b).

Since we have sustained the rejection of claim 1 under 35 U.S.C. 102(b), claims 3-5 will fall therewith and we will sustain the rejection of claims 3-5 under 35 U.S.C. 103.

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