

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

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Paper No. 16

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES

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Ex parte TERRY R. LEE

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Appeal No. 1999-1796  
Application 08/705,149<sup>1</sup>

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ON BRIEF

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Before BARRETT, RUGGIERO, and LEVY, Administrative Patent Judges.

BARRETT, Administrative Patent Judge.

DECISION ON APPEAL

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<sup>1</sup> Application for patent filed August 29, 1996, entitled "Semiconductor Device With Self Refresh Test Mode."

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This is a decision on appeal under 35 U.S.C. § 134 from the final rejection of claims 1-5, 9-33, 36, and 38-51.

We reverse.

BACKGROUND

The disclosed invention relates to a semiconductor having dynamic memory, such as a dynamic random access memory (DRAM) device, that includes a self refresh test mode in which self refresh operations are monitored and/or modified by an external testing device.

Claim 1 is reproduced below.

1. A semiconductor device comprising:

an interface for receiving self refresh test control signals

from an external device;

a memory array;

a self refresh test mode controller coupled to the interface

for outputting internal test control signals in response to the self refresh test control signals during a self refresh test mode of the semiconductor device;

self refresh circuitry coupled to the self refresh test mode

controller for producing refresh signals including preliminary refresh signals and location refresh signals in response to the internal test control signals during the self refresh test mode, with at least some of the preliminary refresh signals being used in producing the location refresh signals; and

selection circuitry coupled to the self refresh circuitry and the memory array for selecting memory locations within the memory array to be refreshed in response to the location refresh signals.



anticipated for the same reasons stated with respect to claim 30 (Br6-7). This does not constitute a separate argument for patentability. Id. ("Merely pointing out differences in what the claims cover is not an argument as to why the claims are separately patentable."). However, we address these claims separately because they are broader, or at least different, than argued claim 30. Appellant makes an argument as to claims 44 and 48 (Br7; RBr4-5); thus, we consider claim 44 and 48 separately. The dependent claims are not separately argued and, thus, stand or fall together with the independent claim from which they directly or indirectly depend.

#### Anticipation

Appellant discloses that the self refresh test mode controller 170 "monitors and/or controls various blocks and internal signals on conductors between blocks in semiconductor device 110" (emphasis added) (specification, p. 11, lines 9-11). One of the four functions of controller 170 is "the ability to monitor internal signals while in the self-refresh mode" (specification, p. 8, line 28; p. 12, line 25); that is, "merely monitoring at least some of the

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refresh signals" (specification, p. 9, line 8). One type of signal that may be analyzed and acted upon by controller 170 or transmitted through controller 170 to conductors connected to a remote testing device is "bits from refresh counter 166" (specification, p. 13, lines 1-3 & 4). The refresh address test circuit 30 in Kang receives and analyzes (monitors) bits from refresh address counter 24 and outputs the result of this analysis on the address test signal line to data output buffer 28 for output to an external device. The refresh address test circuit 30 in Kang does not "control" internal refresh operations. In analyzing the claims, we keep in mind that Kang monitors internal signals, but does not perform any control, and look for such distinguishing language in the claims.

Claim 30

We do not agree with most of the Examiner's reading of claim 30 onto Kang. We agree that control signal generator 20 could be the claimed "interface allowing connection with an external device." The Examiner finds "self refresh circuitry" to read on "&&&, &&&, & generating circuitry, 22, 24" (EA4, three places) and "preliminary refresh circuitry" to be "&&&,"

###, &" (EA4). Elements 22 and 24 do form "self refresh circuitry." However, refresh control signal element 22 only generates the MRFSH signal and element 24 only generates internal address signals  $Q_0-Q_{n-1}$ ; they do not generate ###, ###, & signals as stated by the Examiner. The internal address signals  $Q_0-Q_{n-1}$  from the refresh address counter 24 to the row address buffer 17 are "preliminary refresh signals," see specification, p. 12, lines 16-19, but the Examiner does not make this finding. The Examiner finds that "location refresh signals" read on MRFSH and  $Q_0-Q_{n-1}$  (EA4, two places in claim). However, MRFSH and  $Q_0-Q_{n-1}$  are properly "preliminary refresh signals" and the signals at the output of the row decoder can be considered "location refresh signals," see specification, p. 12, lines 19-21. We agree that refresh address test circuit 30 receives (indirectly) control signals from the interface (control signal generator 20).

Importantly, the Examiner fails to address the most significant, distinguishing limitation of claim 30: "a self refresh test mode controller . . . for receiving control signals from the interface and, in response thereto, modifying self refreshing operations of the semiconductor device while

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it's in the self refresh test mode" (emphasis added).

Appellant argues (Br6; see also arguments at RBr4):

Kang fails to disclose a self refresh test mode controller, or any other circuitry, that modifies self refreshing operations during a self refresh test mode in response to control signals received from an external device, as required by Appellant's claim 30. Instead, Kang discloses a refresh control circuit 22 and refresh address counter 24 that ignore signals from external devices during self refresh. (See Kang, col. 4, lns. 29-39). Therefore, claim 30 is not anticipated by Kang.

The Examiner responds that nothing at column 4, lines 29-39, discloses or suggests that elements 22 and 24 ignore signals from external devices during self refresh (EA5), without responding to the argument about modifying self refreshing operations.

It is implicit in Kang that the self refresh operation mode is not affected by external signals until the self refresh operation mode has been completed. The Examiner has not offered any explanation of what operation can be influenced by an external signal during the self refresh operation. In any case, however, claim 30 recites "in response [to the control signals], modifying self refreshing operations of the semiconductor device while it's in the self refresh test mode." This does not require modifying

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operations under continuous control of the control signals in the self refresh mode as implied by Appellant, but only requires modification in "response thereto"; the control signals could just trigger a modified operation to take place during the refresh operation.

The real issue is whether the refresh address test circuit 30 in Kang in any way "modif[ies] self refreshing operations of the semiconductor device while it's in the self refresh test mode." We find that it does not. Element 30 only monitors operations of the refresh address counter 24 for the purpose of "determining whether all internal refresh addresses corresponding to a complete self-refresh cycle are completely generated" (col. 2, lines 28-30). While element 30 produces an output address test signal to data output buffer 28, this is in no way for "modifying self refreshing operations." Accordingly, the Examiner erred in finding claim 30 to be anticipated by Kang. The anticipation rejection of claim 30 is reversed.

Claims 1-5 and 9-29

Claim 1 recites "an interface for receiving self refresh test control signals from an external device; . . . a self

refresh test mode controller coupled to the interface for outputting internal test control signals in response to the self refresh test control signals during a self refresh test mode of the semiconductor device; self refresh circuitry coupled to the self refresh test mode controller for producing refresh signals . . . in response to the internal test control signals during the self refresh test mode . . ." (emphasis added). Thus, claim 1 requires more than just monitoring the refresh operation as taught by Kang. Kang does not disclose that the refresh address test circuit 30 produces internal test control signals that are used to produce internal refresh signals. Thus, the rejection of claim 1, and its dependent claims 2-5 and 9-29, is reversed.

Claims 31-33

Claim 31 recites "an interface allowing connection with an external device; . . . a self refresh test mode controller . . . for receiving control signals from the interface and, in response thereto, modifying performance of the semiconductor device while it's in the self refresh test mode" (emphasis added). Thus, claim 31 requires more than just monitoring the refresh operation as taught by Kang. The refresh address test

circuit 30 in Kang only monitors whether a complete cycle of internal refresh address signals has been generated and does not perform the function of "modifying performance of the semiconductor device while it's in the self refresh test mode." The rejection of claim 31, and its dependent claims 32 and 33, is reversed.

Claims 36 and 38-43

Claim 36 recites "an external testing device; and a semiconductor device including: an interface for connection to the external testing device; . . . and a self refresh test mode controller . . . for receiving self refresh test control signals from the external testing device through the interface, for controlling self refresh operations of the self refresh circuitry in response thereto . . ." (emphasis added). Thus, claim 36 requires more than just monitoring the refresh operation as taught by Kang. The rejection of claim 36, and its dependent claims 38-43, is reversed.

Claims 44-46

Claim 44 recites a method including the steps of "providing self refresh test control signals from an external

testing device for controlling a self refresh test mode within the semiconductor device; producing refresh signals . . . in response to the self refresh test control signals . . ."

(emphasis added). Thus, claim 44 requires more than just monitoring the refresh operation as taught by Kang. The refresh address test circuit 30 in Kang does not produce refresh signals. The rejection of claim 44, and its dependent claims 45 and 46, is reversed.

Claim 47

Claim 47 recites "a self refresh test mode controller . . . for controlling operation of at least one of the timer, the buffer, and the decoder in outputting the self refresh timing signals, holding the row addresses, and refreshing selected rows in the array in response to self refresh test mode control signals received from an external testing device" (emphasis added). Kang does not disclose controlling internal self refresh operations in response to test mode control signals from an external testing device, much less the specific operations claimed. The rejection of claim 47 is reversed.

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Claims 48-51

Claim 48 is a method which includes the step of "controlling the self refreshing of the semiconductor memory by providing self refresh test mode control signals to the memory from a testing device external to the memory during the self refresh test mode of the memory" (emphasis added). Kang does not disclose "controlling the self refreshing"; Kang only monitors whether a complete cycle of the internal refresh address signals has been generated. Kang also does not disclose controlling of any type by providing external "control signals . . . during the self refresh test mode of the memory" (emphasis added). Once a self refresh operation mode is begun in Kang, the system ignores external signals. The rejection of claim 48, and its dependent claims 49-51, is reversed.

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CONCLUSION

The rejection of claims 1-5, 9-33, 36, and 38-51 is reversed.

REVERSED

LEE E. BARRETT	)	
Administrative	Patent Judge	)
	)	
	)	
	)	
	)	BOARD OF PATENT
JOSEPH F. RUGGIERO	)	APPEALS
Administrative Patent Judge	)	AND
	)	INTERFERENCES
	)	
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