

The opinion in support of the decision being entered today: (1) was not written for publication in a law journal; and (2) is not binding precedent of the Board.

Paper 23

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES

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*Ex parte* BERNARD CADET

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Appeal 1999-1286  
Application 08/567,950<sup>1</sup>

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HEARD: February 20, 2002

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Before: LIEBERMAN, JEFFREY T. SMITH, and NAGUMO, Administrative Patent Judges.

NAGUMO, Administrative Patent Judge.

**Decision on appeal under 35 U.S.C. § 134**

The appeal is from a decision of a primary examiner rejecting claims 1–6 and 16–23. Claims 7–15 have been withdrawn from consideration and are not on appeal.

We affirm in part.

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<sup>1</sup> Application for patent filed December 6, 1995. Appellant claim the benefit of priority under 35 U.S.C. § 119 based on French application no. 94-15151, filed December 9, 1994. According to Appellant, the real party in interest is STMicroelectronics, S.A., of France. (Brief at 1.)

**A. Findings of fact**

The record supports the following findings by at least a preponderance of the evidence.<sup>2</sup>

The invention

Appellant's invention relates to methods of testing integrated circuits on a wafer and destructively marking any defective circuits by laser-irradiating each circuit to be destroyed at a plurality of locations. (Specification at 4; claim 1.) According to Appellant, the claimed methods avoid the problems inherent in marking circuits with ink, such as large ink-spot size, non-uniform marking and the need for subsequent re-marking, misidentification and non-destruction of bad circuits, smudges and inadvertent making and destruction of good circuits, inadvertent marking and contamination of the supporting platform. (*Id.* at 2–3.) In particular, Appellant states that by simultaneously marking and destroying each circuit in a plurality of locations, the circuit is rendered useless more effectively than destruction at a single location. (*Id.* at 4, fifth paragraph.) According to Appellant, the multiple loci of destruction also inhibit fraudulent use of defective circuits. (*Id.*)

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<sup>2</sup> To the extent these findings of fact discuss legal issues, they may be treated as conclusions of law.

The claims

Claims 1, 5, and 17 are representative:

1. A method for physically marking, on a silicon wafer, a surface of an integrated circuit deemed to be defective during a testing step so as to modify a visual appearance of the surface, the method comprising steps of:
  - identifying a defective integrated circuit; and
  - marking the defective integrated circuit at a plurality of locations by exposing the surface of the defective integrated circuit to laser radiation of sufficient magnitude such that the defective integrated circuit will not operate.
  
5. The method according to claim 1, wherein the laser radiation is focused in such a way that a marking diameter at one of the plurality of locations is different than a marking diameter at at least one other of the plurality of locations.
  
17. A method of inspecting a plurality of integrated circuits on a silicon wafer, the method comprising steps of:
  - testing the plurality of integrated circuits;
  - identifying defective integrated circuits; and
  - exposing a surface of each of the defective integrated circuits to laser radiation of sufficient magnitude such that the defective integrated circuit will not operate, the step of exposing including a step of creating a mark on the surface of each of the defective integrated circuits at a plurality of locations.

The prior art

The examiner has relied on the following prior art in support of the rejections:

Abe<sup>3</sup>, Japanese patent publication 63-237,431, published October 3, 1988.

Shils et al. (Shils), U.S. Patent No. 4,510,673, issued April 16, 1985.

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<sup>3</sup> A USPTO translation is of record, a copy of which accompanies this decision.

Hidaka<sup>4</sup>, Japanese patent publication 3-237,738, published October 23, 1991.

The examiner's rejections

Rejection 1. The examiner has rejected claims 5 and 6 as lacking an adequate written description in the specification as filed of the subject matter claimed.

Rejection 2. The examiner has rejected claims 1–4, 16–20, and 23 as unpatentable under 35 U.S.C. § 103(a) over the combined teachings of Abe and Shils.

Rejection 3. The examiner has rejected claims 5, 6, 21, and 22 as unpatentable under 35 U.S.C. § 103(a) over the combined teachings of Abe, Shils, and Hidaka.

We refer the reader to Appellant's brief and reply brief and to the examiner's answer for a full exposition of their respective positions. (We decline to address Appellant's "Request to Reopen Prosecution" (Reply Brief at 1–2) as moot in view of our decision. In any event, such a request should have been made by way of petition to the Technology Center Director. (MPEP § 1002.02(c)-8 (8th Ed., August 2001.))

**B. Discussion**

Rejection 1

Claim 5 requires that the marking diameter at (at least) one marked location differ from the marking diameter at another marked location. Claim 6 depends on claim 5 and specifies a range of marking diameters. The examiner argues that although the specification describes a variable beam diameter, there is no written description of a

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<sup>4</sup> A USPTO translation is of record, a copy of which accompanies this decision.

method that includes changing the diameter of the marking beam while marking a plurality of locations on the same circuit. (Answer at 5.) Appellant argues that the present claim is supported by original specification at page 8, third through fifth paragraphs, describing optics and methods to change the focus size by either moving the focusing lens or changing the relative positions of the circuit and the collimation device, in combination with original claim 5, which recited “the radiation is focused in such a way that a marking diameter is variable. (Brief at 18–19.) Appellant argues that claim 5 as amended is appropriate “because there is a description in the original specification (including claim 5) directed both to varying the diameter of the mark and to marking at a plurality of locations.” (Brief at 19, ll.18–19.)

While Appellant is correct that the original specification describes both varying the diameter of the mark and marking at a plurality of locations, the examiner is also correct that the combination of these two possibilities is not expressly described as a distinct process invented by Appellant. Thus, we need to consider the original specification, including the original claims as well as the written disclosure and the drawings, to determine whether that evidence describes “*the invention*, with all its claimed limitations, not that which makes it obvious.” *Lockwood v. American Airlines, Inc.*, 107 F.3d 1565, 1572, 41 USPQ2d 1961, 1966 (Fed. Cir. 1997) (*quoting Vas-Cath Inc. v. Mahurkar*, 935 F.2d 1555, 1563–64, 19 USPQ2d 1111, 1117 (Fed. Cir. 1991)). As the *Lockwood* court emphasized, “[a]lthough the exact terms need not be used *in*

*haec verba*, . . . the specification must contain an equivalent description of the claimed subject matter. A description which renders obvious the invention for which an earlier filing date is sought is not sufficient.” *Lockwood*, 107 F.3d at 1572, 41 USPQ2d at 1966.

Claims 1 and 5 as originally filed read as follows:

1. A method for physically marking, on a silicon wafer, integrated circuits deemed to be defective during a testing step so as to modify a visual appearance of a surface of these circuits, wherein the marking is done by exposure of the surface of the circuits to a laser radiation.
5. A method according to claim 1, wherein the laser radiation is focused in such a way that a marking diameter is variable.

The combined claim thus reads:

A method for physically marking, on a silicon wafer, integrated circuits deemed to be defective during a testing step so as to modify a visual appearance of a surface of these circuits, wherein the marking is done by exposure of the surface of the circuits to a laser radiation, wherein the laser radiation is focused in such a way that a marking diameter is variable.

This claim, while it may encompass variable focusing of the laser to create marks of different sizes on the same defective integrated circuit, does not expressly describe such a marking method. We therefore turn to the specification and drawings to determine whether they provide a written description of the now-claimed method.

The specification at page 8, full paragraphs three through five, describe methods of changing the size of the laser beam at the integrated circuit:

This collimation device 9 will comprise, for example, a convergent lens to focus the beam 6 if it is desired to mark circuits with a surface area smaller than the diameter of beam 6.

it is also possible to provide for modifying the marking diameter of the circuits by modifying the position of the wayer with respect to the focal plane of the lens:

— either by providing for means to shift this convergent lens in the collimation device 9,

— or by modifying the relative positions of the platform 2 and of the collimation device 9, which is more complicated from the control point of view. . . .

\* \* \* \*

Preferably, the vertical translation of the platform 2 will be used

. . . .

We agree with the examiner that this passage does not expressly describe a method wherein the spot size of the laser beam is varied from spot to spot while marking a single defective integrated circuit. We have reviewed the remainder of the specification, but find no written description that adequately supports Appellant's position. At page 4, Appellant states, "[t]his is why, in an alternative version, the defective chip is marked at several places, for example with a geometrical figure" (emphasis added). At page 11, Appellant describes the factors that affect time it takes to mark the circuit:

"If the marking diameter is smaller, the time of exposure to the beam 7 could be reduced in order to have an identical melting depth. It is also possible, in this same example, to keep an identical exposure time and change the lens 15 to reduce the transmission coefficient of this lens.

Depending on the nature of the surface layers of the circuits, for marking diameters that vary from 300 to 1000 microns and assuming that the exposure time is in the range of 1 millisecond . . .

Of course, to appreciate the total amount of time taken to mark the circuit, it is necessary to take account of the laser recharging time

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between two successive exposures. On the whole, following the above-mentioned assumptions, the marking of the circuit will last about 100 milliseconds.

Conspicuous by its absence is any discussion in any of these passages of a method of varying the focus of the marking laser beam while marking a single integrated circuit in multiple places. Moreover, the drawings are devoid of any indication that such a method was contemplated when the application was filed. Accordingly, because we find that the preponderance of substantial evidence supports the examiner's position that there is an inadequate written description of the method claimed in claims 5 and 6, we affirm this rejection.

#### Rejections 2 and 3

The critical limitation in claim 1 is: "marking the defective integrated circuit at a plurality of locations by exposing the surface of the defective integrated circuit to laser radiation of sufficient magnitude such that the defective integrated circuit will not operate" (emphasis added). The corresponding critical limitation in claim 17 is: "exposing a surface of each of the defective integrated circuits to laser radiation of sufficient magnitude such that the defective integrated circuit will not operate, the step of exposing including a step of creating a mark on the surface of each of the defective integrated circuits at a plurality of locations" (emphasis added.) Thus, the claims require destructive laser marking of the defective integrated circuit(s) at a plurality of locations.

The examiner concedes that Abe does not describe marking the defective circuits at a plurality of locations. (Answer at 5.) To remedy this deficiency, the examiner relies on Shils, which teaches marking at a plurality of locations in order to write various information on the circuit to inform subsequent failure analysis. (*Id.*, citing Shils at col. 4, ll.40–60, col. 5, ll.1–20, and col. 6, ll.25–30.) Appellant objects that Shils teaches away from destructive marking, because Shils teaches that the marking should be done on the back of the chip, such that the marking does not impinge on chip real estate. (Brief at 8–9, citing Shils at col. 2, ll.57–60.)

On review of Shils in its entirety, we agree with Appellant that Shils is concerned exclusively with non-destructive marking, and thus provides no reason, suggestion, teaching, or motivation for the combination with the teachings of Abe regarding destructive marking proposed by the examiner. Accordingly, we hold that the examiner has not established a *prima facie* case of obviousness based on the combined teachings of Abe and Shils, and we reverse rejection 2.

The examiner relies in rejection 3 on Hidaka for teachings of focusing the radiation to control a mark diameter. (Answer at 7.) Because Hidaka does not cure the deficiency of Abe or Shils to teach or suggest multiple sites of destructive marking on each defective integrated circuit, we also reverse rejection 3.

**C. Decision**

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Upon consideration of the appeal, and solely for the reasons given, Rejection 1 is affirmed, and rejections 2 and 3 are reversed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a).

**AFFIRMED IN PART**

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| PAUL LIEBERMAN              | ) |                 |
| Administrative Patent Judge | ) |                 |
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| JEFFREY T. SMITH            | ) | BOARD OF PATENT |
| Administrative Patent Judge | ) | APPEALS AND     |
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| MARK NAGUMO                 | ) |                 |
| Administrative Patent Judge | ) |                 |

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