

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 13

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES

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Ex parte STEVE COOPER

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Appeal No. 1999-0294  
Application No. 08/727,256

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ON BRIEF

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Before KRASS, LALL, and BARRY, Administrative Patent Judges.  
KRASS, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 1-23, all of the pending claims.

The invention is directed to testing the detection and

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correction capabilities of error checking and correction (ECC)  
memory controllers.

Representative independent claim 1 is reproduced as  
follows:

1. A method of verifying error checking and correction  
("ECC") capabilities of a memory controller electrically  
connected to a processor via a bus, said memory controller  
controlling access to a memory device, the method comprising:

disabling said ECC capabilities of said memory  
controller;

while said ECC capabilities of said memory controller are  
disabled, writing a test pattern and a first ECC code to a  
selected location in said memory device, said first ECC code  
corresponding to a natural state of said bus and said test  
pattern being at least one bit different than a pattern  
corresponding to said first ECC code, thereby inducing a  
memory error;

subsequent to said writing, enabling said ECC  
capabilities of said memory controller;

subsequent to said enabling, reading data stored at said  
selected memory location using said memory controller.

The examiner relies on the following references:

Solomon et al. (Solomon)	5,305,326	Apr. 19, 1994
Arroyo et al. (Arroyo)	5,502,732	Mar. 26, 1996

Claims 1-23 stand rejected under 35 U.S.C. 103 as

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unpatentable over Arroyo in view of Solomon.

Reference is made to the brief and answer for the respective positions of appellant and the examiner.

OPINION

We reverse.

The primary reference to Arroyo was cited in the instant specification as being indicative of systems that require the memory controller to be modified to include specialized hardware for testing the ECC logic embedded therein. As pointed out in the specification, page 3, these systems were deemed, by appellant, to be deficient in failing to provide a universal system for testing the ECC capabilities of unmodified ECC memory controllers.

It is the examiner's position that Arroyo discloses a method of verifying ECC capabilities of a memory controller wherein the memory controller controls access to a memory

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device and data transfers into and out of the memory; and writes a test pattern and a first ECC code to a selected location in a memory device, with the test pattern being at least one bit different than a pattern corresponding to the first ECC code, thus inducing a memory error.

The examiner recognizes that Arroyo clearly does not show the features of disabling the ECC capabilities of the memory controller and does not show the enabling of the ECC capabilities of the memory controller. Therefore, the examiner turns to Solomon for the teaching of a user data/parity matching operation in an I/O control processor being performed under command of a host computer and the examiner concludes therefrom that it would have been obvious to modify the method of Arroyo to include the step of providing a command to the components of Arroyo's controller to control the use of components in the controller. The examiner's rationale is that Arroyo suggests that the ECC logic will be implemented in hardware on the memory controller, with the hardware having ECC test components being utilized only during a read operation [Paper No. 4-pages 5-6].

We do not find that the examiner has established a prima

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facie case of obviousness with regard to the instant claimed subject matter.

Each of the independent claims 1, 9, 16 and 23 requires, in one form or another, the disabling of ECC capabilities, writing a test pattern and a first ECC code during the time the ECC capabilities are disabled, enabling the ECC capabilities subsequent to writing the test pattern, and then reading data stored in memory using the memory controller, subsequent to the enabling. The examiner admits that Arroyo does not disable the ECC capabilities and does not then enable the ECC capabilities subsequent to writing a test pattern, as claimed.

The writing of a test pattern must take place subsequent to disabling the ECC capabilities, according to the dictates of the instant claimed invention. We find nothing in Arroyo remotely related to such a claimed feature, and the examiner has pointed to nothing. The examiner attempts to explain this, at page 4 of the answer, by referring to a write and read operation in Arroyo and concluding that the artisan would have realized that Arroyo's ECC generator 41 would have been disabled during the write operation and would have been

enabled during the read operation. The examiner bases this belief on Arroyo's disclosure of the ECC generator being used only when the reading operation is performed [answer-pages 4-5].

To whatever extent the examiner statement may be accurate in the sense of the ECC in Arroyo being "in use" or "not in use," during certain times during the processing in Arroyo, this is not the same as the "disabling" and "enabling" of ECC capabilities, as claimed in the instant application. The instant claims require that ECC capabilities are disabled. That means that even if the ECC capabilities would normally be invoked at some point, they cannot be because the ECC capabilities are disabled. It is more than a matter of the ECC generator simply not being used at a particular time because, in the instant claimed invention, if the ECC capabilities were not "disabled," as claimed, then the subsequent writing of the test pattern may cause the ECC capabilities to be invoked. However, the instant claimed invention specifically requires the step of disabling the ECC capabilities of the memory controller before the subsequent writing of a test pattern and a first ECC code to a selected

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memory location in memory, with the first ECC code corresponding "to a natural state" of the bus. Since the test pattern is at least one bit different than a pattern corresponding to the first ECC code, a memory error is induced. Only after this happens does the instant claimed invention permit the subsequent enabling of the ECC capabilities of the memory controller again.

We do not find these very specifically claimed steps in Arroyo, nor does it appear that Arroyo ever disables the ECC generator at any time. We find nothing in the Solomon reference which remedies this deficiency of Arroyo.

Accordingly, the examiner's decision rejecting claims 1-23 under 35 U.S.C. 103 is reversed.

REVERSED

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ERROL A. KRASS	)	
Administrative Patent Judge	)	
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PARSHOTAM S. LALL	)	BOARD OF PATENT
Administrative Patent Judge	)	APPEALS AND
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