

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 24

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES

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Ex parte FRANK C. GOVER, FRANK E. LEVINE, BRET R. OLSZEWSKI,  
CHARLES P. ROTH, EDWARD H. WELBON, and CHARLES WRIGHT

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Appeal No. 1999-0288  
Application No. 08/538,071

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ON BRIEF

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Before THOMAS, HAIRSTON, and LEVY, Administrative Patent Judges.  
LEVY, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134 from the examiner's final rejection of claims 6, 8-11, 14-18, 20-25, 28-31, and 33-40, which are all of the claims pending in this application.

BACKGROUND

Appellants' invention relates to a method and system for selecting and distinguishing an event sequence using an effective address in a processing system. An understanding of the

invention can be derived from a reading of exemplary claim 6,  
which is reproduced as follows:

6. A method for providing a match on a selected event in performance monitoring of a processing system, the processing system including at least one performance monitor counter (PMC), the method comprising the steps of:

(a) initializing the at least one PMC; and

(b) controlling counting in the at least one PMC based upon the nth occurrence of a match to a specified address, where n is greater or equal to one, the match being based upon the specified address being associated with a specific process identified by a bit in a machine state register.

The prior art references of record relied upon by the examiner in rejecting the appealed claims are:

Wibecan	5,537,541	Jul. 16, 1996 (filed Aug. 16, 1994)
Gover et al. (Gover)	5,557,548	Sep. 17, 1996 (filed Dec. 9, 1994)

Brantley, et al. (Brantley), "RP3 Performance Monitoring Hardware", Instrumentation for Future Parallel Computing Systems, Ass. For Computing Machinery, Inc., (1989), pages 186-198

Claims 6, 8-11, 14-18, 20-25, 28-31, and 33-40 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Wibecan in view of Brantley.

Claims 8-11, 14-18, 20-25, 28-31, 33-36, 38, and 39<sup>1</sup> stand rejected under 35 U.S.C. § 103(a) as unpatentable over Gover in view of Wibecan.

Rather than reiterate the conflicting viewpoints advanced by the examiner and appellants regarding the above-noted rejections, we make reference to the examiner's answer (Paper No. 16, mailed March 31, 1998) and the final rejection (Paper No. 6, mailed April 3, 1997) for the examiner's complete reasoning in support of the rejections, and to appellants' brief (Paper No. 15, filed February 2, 1998) and reply brief (Paper No. 20, filed June 1, 1998) for appellants' arguments thereagainst. Only those arguments actually made by appellants have been considered in this decision. Arguments which appellants could have made but chose not to make in the brief have not been considered. See 37 CFR 1.192(a).

#### OPINION

In reaching our decision in this appeal, we have carefully considered the subject matter on appeal, the rejections advanced by the examiner, and the evidence of obviousness relied upon by

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<sup>1</sup> The rejection of claims 37 and 40 under this ground has been withdrawn by the examiner (answer, page 4).

the examiner as support for the rejections. We have, likewise, reviewed and taken into consideration, in reaching our decision, appellants' arguments set forth in the briefs along with the examiner's rationale in support of the rejections and arguments in rebuttal set forth in the examiner's answer.

It is our view, after consideration of the record before us, that the evidence relied upon and the level of skill in the particular art would not have suggested to one of ordinary skill in the art the invention as set forth in claims 6, 8-11, 14-18, 20-25, 28-31, and 33-40. Accordingly, we reverse, for the reasons set forth by appellants, and add the following comments.

In rejecting claims under 35 U.S.C. § 103, it is incumbent upon the examiner to establish a factual basis to support the legal conclusion of obviousness. See In re Fine, 837 F.2d 1071, 1073, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). In so doing, the examiner is expected to make the factual determinations set forth in Graham v. John Deere Co., 383 U.S. 1, 17, 148 USPQ 459, 467 (1966), and to provide a reason why one having ordinary skill in the pertinent art would have been led to modify the prior art or to combine prior art references to arrive at the claimed invention. Such reason must stem from some teaching, suggestion or implication in the prior art as a whole or knowledge generally

available to one having ordinary skill in the art. Uniroyal, Inc. v. Rudkin-Wiley Corp., 837 F.2d 1044, 1051, 5 USPQ2d 1434, 1438 (Fed. Cir. 1988); Ashland Oil, Inc. v. Delta Resins & Refractories, Inc., 776 F.2d 281, 293, 227 USPQ 657, 664 (Fed. Cir. 1985); ACS Hosp. Sys., Inc. v. Montefiore Hosp., 732 F.2d 1572, 1577, 221 USPQ 929, 933 (Fed. Cir. 1984). These showings by the examiner are an essential part of complying with the burden of presenting a prima facie case of obviousness. Note In re Oetiker, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992). If that burden is met, the burden then shifts to the applicant to overcome the prima facie case with argument and/or evidence. Obviousness is then determined on the basis of the evidence as a whole. See id.; In re Hedges, 783 F.2d 1038, 1039, 228 USPQ 685, 686 (Fed. Cir. 1986); In re Piasecki, 745 F.2d 1468, 1472, 223 USPQ 785, 788 (Fed. Cir. 1984); and In re Rinehart, 531 F.2d 1048, 1052, 189 USPQ 143, 147 (CCPA 1976).

We consider first the rejection of claims 6, 8-11, 14-18, 20-25, 28-31, and 33-40 under 35 U.S.C. § 103(a) based on the teachings of Wibecan and Brantley.

The examiner's position (final rejection, page 3) is that with respect to claim 6, "Wibecan does not specifically state the monitoring of specific addresses being referenced." To overcome

this deficiency in Wibecan, the examiner turns to Brantley for a teaching of monitoring events including the number of times a specific address is accessed. The examiner asserts (final rejection, page 3) that it would have been obvious to allow Wibecan's system to control the counting of events such as specific address references, as taught by Brantley because it would allow Wibecan's system to measure the performance of accesses to specific addresses, which will give a user a chance to adjust any parameters or configurations of the system in order to receive better performance from the data processing system.

The examiner further asserts (final rejection, page 4) that Wibecan does not show the use of the performance monitor bit being located in a machine state register. The examiner takes the position (final rejection, page 4) that "it would have been obvious to one of ordinary skill in the art to realize that the enablement of a processing system to recognize which mode or process it is operating in, such as user or supervisor mode, are usually located in a register which is accessible to the processing systems other elements. This ensures that certain processes can not be executed while in certain modes" and that (pages 4 and 5) "it would have found it obvious to place the process recognition bit (flags etc.) in a state register which

would be accessible by the elements of the monitoring system (including software) because it would ensure that the specif[ic] process, along with the events associated with the process, are identified correctly, in order to enable the counters correctly for performance monitoring of those events and processes."

With respect to independent claim 8, the examiner asserts (final rejection, page 5) that "Wibecan does not specifically show a control register, rather control routines which control the operation of the counters." To overcome this deficiency in Wibecan, the examiner turns to Brantley for a teaching of a register which controls the operation of the counting functions. The examiner asserts (id.) that "[i]t would have been obvious to one ordinary skill in the art to utilize a hardware based register to house the controlling indicators for the counting operations performed by Wibecan's counting functions, because it would allow Wibecan's system to have a hardware based performance monitoring option, which would complement the software based monitoring functions which operate in a similar manner. This would allow a user to control the counters using a control register, via setting bits in hardware register, rather than doing so in a data structure in a software routine, which gives a user versatility in controlling the monitoring session."

The examiner asserts (final rejection, page 6) that "Wibecan does not specifically show determining a logic level for a bit in a machine state register, and determining the logic levels for a bit set of a second MMCR." The examiner (id.) once again notes that Brantley teaches the use of a register which controls the operation of the counting operations, and argues that "[i]t would have been obvious to one [of] ordinary skill in the art to utilize a hardware based register to house the controlling indicators for the counting operations performed by Wibecan's counting functions, because it would allow Wibecan's system to have a hardware based performance monitoring option, which would complement the software based monitoring functions which operate in a similar manner. This would allow a user to control the counters using a control register, via setting bits in hardware register, rather than doing so in a data structure in a software routine, which gives a user versatility in controlling the monitoring session.... [o]ne of ordinary skill in the art would have recognized this relationship and incorporated the varying ways of controlling the counters in Wibecan's system in order to give the system additional versatility in controlling the counting services provided by the monitoring system. Although

Wibecan does not specifically state the at [sic; that] this bit it [sic; is] in a machine state register, it would have been obvious to one of ordinary skill in the art to realize that the enablement of a processing system to recognize which mode or process it is operating in, such as user or supervisor mode, are usually located in a register which is accessible to the processing systems other elements." The examiner additionally repeats the argument from claim 6 that the modification would have been obvious because it would ensure that the specific process, along with the events associated with the process, are identified correctly, in order to enable the counters correctly for performance monitoring of the events and processes.

With respect to the lack of a teaching or suggestion of a second MMCR in Wibecan and Brantley, the examiner argues (final rejection, pages 7 and 8) that:

It would have been obvious to one of ordinary skill in the art to allow the combined system of Wibecan and Brantley to include the use of multiple ones of control registers because it would enable the system the incorporate the versatility of controlling a plurality of counters with these control registers, thus allowing the adjustment and "control" of these registers to be altered more readily by the system.

The examiner adds (id.) that "it would have been obvious to check the bit set of those registers during normal operation because, as claimed by the applicant, such a process step has no net effect on any of the monitoring procedures claimed."

With respect to independent claim 17, the examiner presents similar arguments (final rejection, pages 10-12) as were presented with respect to independent claims 6 and 8.

With respect to independent claims 22, 31, and 36, and 37, the examiner (final rejection, page 7) refers to independent claims 8 and 17.

With respect to independent claim 38, the examiner (final rejection, page 17) refers to claim 8, and adds that it would have been obvious to store the routines of Wibecan on a computer readable medium.

With respect to independent claims 39 and 40, the examiner (id.) refers to claims 6, 8, and 17, and again adds that it would have been obvious to store the routines on a computer readable medium.

Appellants assert (brief, page 13) that "Wibecan in view of Brantley does not render [independent] Claims 6, 8, 17, 22, 31,,36, 37, 38, 29, or 40 obvious." Appellants argue (brief, page 14) to the effect that it would not have been obvious to

provide Wibecan with a hardware-based register as taught by Brantley because Wibecan teaches (col. 2, lines 31-34) that its interface should be independent of the hardware and software of the system. Appellants argue (id.) that Wibecan uses data structures to define how the performance monitoring logic of the system is utilized, and that to relocate the information supplied by these data structures from memory to control registers, eliminates the system independence. It is further argued (id.) that there is nothing in Wibecan that teaches or suggests the use of monitor mode control registers (MMCRs) and a machine state register to perform performance monitoring based upon an effective address in a specific process. As pointed out by appellants (id.) Brantley's suggestion to count the number of times that a specific address is accessed is controlled by a single status register in the performance monitor chip.

Further (brief, pages 14 and 15), because Brantley suggests that the counting of the number of times an instruction occurs may be achieved by a single status register, appellants fail to see how the recited use of two control registers in conjunction with the machine status register is taught or suggested by Brantley, and that even the combination of the single status

register of Brantley with Wibecan would not teach or suggest the claimed invention.

Appellants further assert (brief, page 15) that the examiner admits that Wibecan does not specifically state the monitoring of specific addresses being referenced, nor does Wibecan teach that a bit within the machine state register is used to select the specific process to be monitored.

Appellants (brief, pages 15 and 16) argue that:

In Wibecan, the processes, i.e., application programs, capable of being monitoring must be identified as such by an input argument to a bit set routine to allow associating and setting of a performance monitoring enabled bit with the process (col. 6, lines 51-62). Thus, a controlling process uses a bit set routine to associate a bit with a process to allow monitoring of the process. But, as admitted, there is nothing to teach or suggest that a specific address within a specific process is monitored. Thus, there is nothing that teaches or suggests that a machine state register should be used for the performance monitoring enabled bit to help ensure that the specific address is monitored only within the specific process.

Appellants further argue (reply brief, pages 2 and 3) that even if the teachings of Brantley and Wibecan were combined, there is no teaching or suggestion of using multiple control registers, including the machine state register as set forth in the claimed monitoring scheme.

It is lastly asserted (reply brief, page 4) that

[T]he "status register" of Brantley is identified as part of the performance monitor chip (see page 195), which is shown as a separate element from the processor prototype and thus does not teach or suggest the use of a machine state register . . . . So, again, even the combination of Brantley with Wibecan does not teach, show, or suggest Appellant's recited system and utilization of a machine state register in performance monitoring, including to identify a selected event/specific address within a specific process.

The examiner responds (answer, pages 4 and 5) that with respect to allowing Wibecan's system to utilize a register to aid in control functions, that allowing a register to store this bit would not be detrimental to Wibecan's system because it is suggested by Wibecan's disclosure that the Processor-Memory Element (PME) is utilized to control the monitored process, and that allowing this bit to be located in a register would have been an obvious implementation of well known techniques already practiced in the art, as shown by Brantley. With respect to appellants' argument that Wibecan, Brantley and Gover do not show the use of MMCRs or machine status registers to perform performance monitoring based upon an effective address in a specific process, the examiner takes the position (answer, page 6) that appellants' claims seem to lack this limitation as well.

As per the use of a state register to house the PME bit controlling the specific process, the examiner asserts (answer, page 9) that such a variation would not affect the system's ability to perform the monitoring functions described above. The examiner adds that allowing a state register to store this PME bit or information related to the control of the monitoring process, as shown by Brantley, would not be detrimental to Wibecan's system because it is clearly suggested by Wibecan's disclosure that the PME is utilized to control the specific process to be monitored.

From our review of Wibecan and Brantley, we find that as admitted by the examiner (final rejection, page 4) Wibecan does not disclose a performance monitoring bit in a machine state register, and that neither Wibecan nor Brantley discloses a second MMCR. Although Brantley discloses the use of a Performance Monitor Chip (PMC) in each Processor-Memory Element (PME); that there are up to 500 PMEs, and that each PMC (page 195) includes, inter alia, a status register which controls the type of data to be collected, the frequency of collection, as well as providing status about the data collection, we find that Brantley does not teach or suggest a match on a selected event in performance monitoring of a processing system where the match is

based upon the specific address associated with a specific process identified by a bit in a machine state register, as recited in claim 6. In addition, because each of the up to 500 Processor-Memory Elements contains a Performance Monitoring Chip, which includes a status register, we find no suggestion that the status register in Brantley is a machine state register. Moreover, with respect to the examiner's assertion (final rejection, pages 4 and 5) that it would have been obvious to place the process recognition bit in a machine state register because it would ensure that the specific process, along with the events associated with the process, are identified correctly, in order to enable the counters correctly for performance monitoring of those events and processes, we find no recognition of any problem in Wibecan or Brantley with respect to incorrect identification of events within a process, that would suggest placing a process recognition bit within a machine state register.

As stated, supra, with respect to appellants' assertion that Wibecan, Brantley, and Gover do not show the use of MMCRs or machine status registers to perform performance monitoring based upon an effective address in a specific process, the examiner takes the position (answer, page 6) that appellants' claims seem

to lack this limitation as well. With respect to the examiner's position, we observe that independent claim 8, like independent claim 6, similarly recites determining the logic levels for at least one bit of a machine state register and determining the logic levels for a bit set of a second MMCR. Independent claim 17 similarly recites a plurality of MMCRs as well as the set of logic conditions including a chosen logic level for a performance monitor bit of a machine state register to mark a specific process for counting. Independent claim 22 similarly recites determining a logic level for at least one bit of a machine state register and determining logic levels for a second bit of a second MMCR. Independent claim 31 similarly recites the set of logic conditions including a chosen logic level for a performance monitor bit of a machine state register to mark a specific process for counting. Independent claim 36 similarly recites controlling counting upon the selected event being associated with a specific process and for triggering counting when the selected event is matched based upon a logic level of a bit within a machine state register within the processing system. Independent claim 37 similarly recites controlling counting based upon the effective address being associated with a specific process and for triggering counting when the effective address is

matched based upon a logic level of a bit within a machine state register within the processing system. Independent claim 38 similarly recites determining a logic level for at least one bit of a machine state register and determining logic levels of a bit set of a second MMCR. Independent claim 39 similarly recites triggering counting when the selected event is matched based upon a logic level of a bit within a machine state register within the processing system. Independent claim 40 similarly recites triggering counting when the effective address is matched based upon a logic level of a bit within a machine state register within the processing system.

Thus, we find that even if the teachings of Wibecan and Brantley were combined, that appellants' claims would still not be met, because the prior art references to Wibecan and Brantley do not teach or suggest the claim limitations set forth, supra, as the prior art would not have suggested the use of a performance monitoring bit in a machine state register, nor the claimed second MMCR.

The examiner bears the initial burden of establishing a prima facie case of obviousness. The extensive arguments of the examiner, even if we agreed with him from our own experience and background knowledge of the art, are not a substitute for

evidence on the record. In order to sustain the examiner's rejection under 35 U.S.C. § 103(a), we would have to resort to speculation or unfounded assumptions to supply the deficiencies in the factual basis of the rejection. The examiner may not resort to speculation or unfounded assumptions to supply deficiencies in establishing a factual basis. See In re Warner, 379 F.2d 1011, 1017, 154 USPQ 173, 178 (CCPA 1967). Stated differently, the subjective opinion of the examiner as to what is or is not obvious, without evidence in support thereof, does not provide a factual basis upon which the legal conclusion of obviousness can be reached. Simply put, more evidence is needed to convince us of the obviousness of the subject matter of the claims on appeal, than for the examiner to rely upon the examiner's own arguments. Although decided subsequent to the mailing of the examiner's answer, our reviewing court has made clear in In re Lee, 277 F.3d 1338, 61 USPQ2d 1430 (Fed. Cir. 2002), and In re Zurko, 111 F.3d 887, 42 USPQ2d 1476 (Fed. Cir. 2001) that rejections must be supported by substantial evidence in the administrative record and that where the record is lacking in evidence, this Board cannot and should not resort to unfounded speculation. From all of the above, we therefore find that the examiner has failed to establish a prima facie case of

obviousness of the claimed invention set forth in claims 6, 8-11, 14-18, 20-25, 28-31, and 33-40. Accordingly, the rejection of claims 6, 8-11, 14-18, 20-25, 28-31, and 33-40 under 35 U.S.C. § 103(a) as unpatentable over Wibecan in view of Brantley is reversed.

We turn next to the rejection of claims 8-11, 14-18, 20-25, 28-31, 33-36, 38, and 39 under 35 U.S.C. § 103(a) as unpatentable over Gover in view of Wibecan. As correctly noted by the examiner (final rejection, page 19), Gover teaches the use of plural MMCRs as well as accessing a second MMCR to check its logical contents. However, as admitted by the examiner (id.) "Gover does not show the determining of a bit in a machine state register" and that (final rejection, page 22) that "Gover does not show the use of a performance monitor bit, to mark specific process for counting, in a state register to aid in controlling the counting of events." Accordingly, we reverse the rejection of claims 8-11, 14-18, 20-25, 28-31, 33-36, 38, and 39 because Gover does not make up for the deficiencies of Wibecan, and the examiner's arguments are not a substitute for evidence in the record.

CONCLUSION

To summarize, the decision of the examiner to reject claims 6, 8-11, 14-18, 20-25, 28-31, and 33-40 under 35 U.S.C. § 103(a) is reversed.

REVERSED

JAMES D. THOMAS	)	
Administrative Patent Judge	)	
	)	
	)	BOARD OF PATENT
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	)	APPEALS AND
KENNETH W. HAIRSTON	)	
Administrative Patent Judge	)	INTERFERENCES
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