

The opinion in support of the remand being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 16

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte MARC A. AUSLANDER and LARRY W. LOEN

Appeal No. 1999-0041
Application No. 08/475,669

ON BRIEF

Before DIXON, BARRY, and LEVY, Administrative Patent Judges.
BARRY, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134 from the rejection of claims 2-5, 18, and 19. We reverse.

BACKGROUND

The appellants' invention relates to endian-oriented computers. Big endian and little endian are two common schemes for organizing data within the memory of a computer. The former scheme stores the most significant byte of a word

Appeal No. 1999-0041
Application 08/475,669

at the lowest memory address; the latter scheme, at the highest memory address.

While the big endian scheme would store the hexadecimal number A02B as A02B, for example, the little endian scheme would store it as 2BA0. Apple Macintosh computers use big endian; IBM personal computers (PCs), little endian.

Compatibility is needed between different types of computers. For example, users of IBM PCs cannot generally share computer programs and data with users of Apple Macintosh computers, and vice versa. Heretofore, bi-endian computers have been used in an attempt to deal with the endian problem. Such a computer can be made to execute either big endian tasks or little endian tasks, but not both types of tasks together. Switching the computer's endian mode requires special software that executes very close to start-up. When the computer is started, it is "told" whether it will be running in a big endian mode or a little endian mode. Thereafter, it executes all tasks in the specified endian.

Appeal No. 1999-0041
Application 08/475,669

The appellants' invention enhances a conventional bi-endian computer to include mixed-endian mechanisms that allow the computer to change its endian mode dynamically. The mixed-endian computer can change its endian mode on a task by task basis if necessary. The mechanisms automatically format data in the scheme expected by the running task, either big endian or little endian. The mechanisms also format big and little endian instructions such that they can execute on the same computer. The mechanisms also include two memory management mechanisms, a single aliased memory management mechanism and a double aliased memory management mechanism. Each memory management mechanism provides cross-endian data sharing.

Claims 2 and 19, which are representative for our purposes, follow:

2. A computer system, said computer system comprising:

a conventional bi-endian processor, said processor being used to execute a plurality of tasks, said tasks including big endian tasks and little endian tasks;

memory, said memory being divided into a plurality of storage aggregates, said plurality of storage aggregates containing data, said data including big endian data and little endian data, said plurality of storage aggregates including markings, said markings indicating whether said storage aggregates contain data formatted as big endian data or contain data formatted as little endian data, said memory comprising big endian programs and little endian programs, said big endian programs executing as said big endian tasks and said little endian programs executing as said little endian tasks, said tasks executing on a task-for-task basis directly on said conventional biendian [sic] processor;

a memory management mechanism, said memory management mechanism using said markings to allow said big endian programs to share said big endian data with said little endian programs.

19. A computer-implemented method for sharing data between big endian programs and little endian programs, said big endian programs executing as big endian tasks, said little endian programs executing as little endian tasks, said big endian tasks and said little endian tasks executing a processor on a task-for-task basis, said method comprising the steps of:

attempting to access data contained in memory, said data being contained in a storage aggregate within said memory, said storage aggregate being marked to indicate a particular endian format type, said attempting step being performed by a task of a particular endian type;

determining whether said data's particular endian type is the same as that of said task;

Appeal No. 1999-0041
Application 08/475,669

double word reflecting said data when said data's particular endian type is found not to be the same as that of said task; and

accessing said data.

The prior art applied in rejecting the claims follows:

Undy et al. (Undy), A Low Cost Graphics and Multimedia Workstation Chip Set, IEEE Micro, Apr. 1994, pp. 10-22

James, Multiplexed Buses: The Endian Wars Continue, IEEE Micro, June 1990, pp. 9-21.

Claims 2-5, 18, and 19 stand rejected under 35 U.S.C. § 103 as being obvious over Undy in view of James. Rather than reiterate the arguments of the appellants or examiner in toto, we refer the reader to the brief and answer for the respective details thereof.

OPINION

In deciding this appeal, we considered the subject matter on appeal and the rejection of the examiner. Furthermore, we duly considered the arguments and evidence of the appellants and examiner. After considering the record, we are persuaded

Appeal No. 1999-0041
Application 08/475,669

that the examiner erred in rejecting claims 2-5, 18, and 19.
Accordingly, we reverse.

We begin by noting the following principles from In re Rijckaert, 9 F.3d 1531, 1532, 28 USPQ2d 1955, 1956 (Fed. Cir. 1993).

In rejecting claims under 35 U.S.C. § 103, the examiner bears the initial burden of presenting a prima facie case of obviousness. In re Oetiker, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992).... "A prima facie case of obviousness is established when the teachings from the prior art itself would appear to have suggested the claimed subject matter to a person of ordinary skill in the art." In re Bell, 991 F.2d 781, 782, 26 USPQ2d 1529, 1531 (Fed. Cir. 1993) (quoting In re Rinehart, 531 F.2d 1048, 1051, 189 USPQ 143, 147 (CCPA 1976)).

With these principles in mind, we consider the examiner's rejection and the appellants' arguments regarding the following claims:

- claims 2-5 and 18
- claim 19.

I. Claims 2-5 and 18

The examiner asserts, "[t]he 'processor being used to execute big endian tasks and little endian tasks' is taught at

Appeal No. 1999-0041
Application 08/475,669

Undy, Page 17, Left Column, especially after the combination with James." (Examiner's Answer at 5.) The appellants argue, "the asserted Undy-James combination cannot fairly be said to teach disclose or suggest a mechanism that allows tasks to execute on a task for task basis directly on said conventional bi-endian processor." (Appeal Br. at 5.)

"`[T]he main purpose of the examination, to which every application is subjected, is to try to make sure that what each claim defines is patentable. [T]he name of the game is the claim" In re Hiniker Co., 150 F.3d 1362, 1369, 47 USPQ2d 1523, 1529 (Fed. Cir. 1998)(quoting Giles S. Rich, The Extent of the Protection and Interpretation of Claims--American Perspectives, 21 Int'l Rev. Indus. Prop. & Copyright L. 497, 499, 501 (1990)). Here, claims 2-5 and 18 specify in pertinent part the following limitations: "a conventional bi-endian processor, said processor being used to execute a plurality of tasks, said tasks including big endian tasks and little endian tasks; . . . said tasks executing on a task-for-task basis directly on said conventional biendian [sic] processor" Accordingly,

Appeal No. 1999-0041
Application 08/475,669

claims 2-5 and 18 require executing big endian tasks and little endian tasks on a task-for-task basis directly on a conventional, bi-endian processor.

The examiner fails to show a teaching or suggestion of the limitations in the prior art of record. "Obviousness may not be established using hindsight or in view of the teachings or suggestions of the inventor." Para-Ordnance Mfg. v. SGS Importers Int'l, 73 F.3d 1085, 1087, 37 USPQ2d 1237, 1239 (Fed. Cir. 1995)(citing W.L. Gore & Assocs., Inc. v. Garlock, Inc., 721 F.2d 1540, 1551, 1553, 220 USPQ 303, 311, 312-13 (Fed. Cir. 1983)). "It is impermissible to use the claimed invention as an instruction manual or 'template' to piece together the teachings of the prior art so that the claimed invention is rendered obvious." In re Fritch, 972 F.2d 1260, 1266, 23 USPQ2d 1780, 1784 (Fed. Cir. 1992) (citing In re Gorman, 933 F.2d 982, 987, 18 USPQ2d 1885, 1888 (Fed. Cir. 1991)). "The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." Id. at 1266, 23 USPQ2d at

Appeal No. 1999-0041
Application 08/475,669

1784 (citing In re Gordon, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984)).

Here, although Undy's Hummingbird processor "supports both big-endian addressing, which all previous PA-RISC processors implement, and little-endian addressing[,]" p. 17, col. 1, the processor is neither conventional nor bi-endian. To the contrary, it is a modification of a conventional, mono-endian PA-RISC processor. Regarding the modified nature of the reference's processor, the examiner admits "the processor taught by Undy is a modified version of the Hewlett-Packard PA-RISC processor" (Examiner's Answer at 8.) He further admits of "the bi-endian modification of Undy to the 'conventional' Hewlett-Packard PA-RISC processor" (Id. at 9.) For its part, the reference describes the modification as "add[ing] a mode bit to the PA-RISC processor architecture that selects between big- and little-endian byte addressing." P. 17, col. 1. Regarding the mono-endian nature of Undy's processor, James lists "the PA-RISC processor," p. 14, col. 2, as one of several "big-endian processors" (Id.) Relying on James to teach "a mechanism (and the concept of specifying

Appeal No. 1999-0041
Application 08/475,669

data as a particular endian type) that enables systems of different endian types to share data[,]” (Examiner's Answer at 4), the examiner fails to allege, let alone show, that the reference cures the deficiency of Undy.

Because Undy's Hummingbird processor is a modification of a conventional, mono-endian processor, we are not persuaded that teachings from the prior art would have suggested the limitations of “a conventional bi-endian processor, said processor being used to execute a plurality of tasks, said tasks including big endian tasks and little endian tasks; ... said tasks executing on a task-for-task basis directly on said conventional biendian [sic] processor” Therefore, we reverse the rejection of claims 2-5 and 18 as being obvious over Undy in view of James. We proceed to claim 19.

II. Claim 19

Appeal No. 1999-0041
Application 08/475,669

The examiner asserts, "[f]or 'double word reflecting,' please see James, Page 12, 'Glossary of Terms' and Figures 8-10." (Examiner's Answer at 7.) The appellants argue, "James, then, cannot fairly be said to teach, disclose, or suggest double word reflection." (Appeal Br. at 6.)

Claims 19 specifies in pertinent part the following limitations: "attempting to access data contained in memory, ... said attempting step being performed by a task of a particular endian type; double word reflecting said data when said data's particular endian type is found not to be the same as that of said task" Accordingly, the claim requires double word reflecting data when the data's particular endian type is found not to be the same as that of a task attempting to access the data.

The examiner fails to show a teaching or suggestion of the limitations in the prior art of record. Here, neither the Glossary of Terms nor the Figures 8-10 relied on by the examiner mention, let alone teach double word reflecting data. Furthermore, the description of the Figures merely explains

Appeal No. 1999-0041
Application 08/475,669

the difference between the big endian and little endian formats. P. 14. Relying on Undy to teach other features, (Examiner's Answer at 6-7), the examiner fails to allege, let alone show, that the reference cures the deficiency of James.

Because James' Glossary and Figures 8-10 fail to mention double word reflecting, we are not persuaded that teachings from the prior art would have suggested the limitations of "attempting to access data contained in memory, ... said attempting step being performed by a task of a particular endian type; double word reflecting said data when said data's particular endian type is found not to be the same as that of said task" Therefore, we reverse the rejection of claim 19 as being obvious over Undy in view of James.

Appeal No. 1999-0041
Application 08/475,669

CONCLUSION

In summary, the rejection of claims 2-5, 18, and 19 under § 103 is reversed.

REVERSED

JOSEPH L. DIXON)	
Administrative Patent Judge)	
)	
)	
)	
)	BOARD OF PATENT
LANCE LEONARD BARRY)	APPEALS
Administrative Patent Judge)	AND
)	INTERFERENCES
)	
)	
)	
STUART S. LEVY)	
Administrative Patent Judge)	

LLB/gjh

Appeal No. 1999-0041
Application 08/475,669

STEVEN W. ROTH
IBM CORPORATION
DEPT. 917
3605 HIGHWAY 52 NORTH
ROCHESTER, MN 55901

Appeal No. 1999-0041
Application 08/475,669

APPEAL NO. 1999-0041 - JUDGE BARRY
APPLICATION NO. 08/475,669

APJ BARRY

APJ LEVY

APJ DIXON

Prepared By: APJ BARRY

DRAFT SUBMITTED: 20 Mar 02

GJH

FINAL TYPED:

Team 3:

I typed most of this opinion.

Please check spelling, cites, and quotes.

Do NOT change matters of form or style.