

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 35

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte RONALD J. CHAPMAN, ARIEL B. CHRISTENSEN,
CARL E. JONES and SUSHAMA M. PARANJAPE

Appeal No. 1999-0011
Application No. 08/428,812

ON BRIEF

Before JERRY SMITH, RUGGIERO, and LALL, Administrative Patent Judges.

LALL, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134 from the final rejection¹ of claims 1 to 14, which constitute all the pending claims in the application.

¹An amendment after final rejection was filed as paper number 25, and its entry was approved by the Examiner, see paper number 26.

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The invention is related to an improved multi-bit error correction system. The inventive error correction system performs a fast error correcting operation on individual bits within multi-bit modules. In the specific implementation, the invention uses Hamming code decoders, m modules for a $n \times m$ bit data word, with each module having m bits. The error bits of each module are combined to form a set of parity bits. Syndrome bits are generated from the parity bits and used to locate errors in the bits. Finally, errors in the bits are corrected in a conventional manner to provide corrected data bits. Thus, the invention provides a high speed error detection and correction technique for data containing multi-bit words.

The invention is further illustrative by the following claim.

Claim 1. An improved multi-bit error correction system comprising:

first means for providing an n times m bit data word and
second means for correcting multiple bits in said data word[,] said second means including m parallel one bit Hamming code decoders.

The examiner relies on the following references:

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Bossen et al. (Bossen)	3,582,878	Jun 01, 1971
Price et al. (Price)	5,418,796	May 23, 1995

Claims 1 to 10 and 12 to 14 stand rejected under the second paragraph of 35 U.S.C. § 112. Claims 1 to 4 stand rejected under 35 U.S.C. § 103 as being unpatentable over Bossen, while claims 5 to 14 stand rejected under 35 U.S.C. § 103 as being unpatentable over Bossen and Price.

Rather than repeat in toto the positions and the arguments of Appellants and the Examiner, we make reference to the Brief and the Answer for their respective positions.

OPINION

We have considered the rejection advanced by the Examiner. We have, likewise, reviewed Appellants' arguments against the rejections as set forth in the Brief.

We affirm-in-part.

REJECTION UNDER 35 U.S.C. § 112

The second paragraph of 35 U.S.C. § 112 requires claims to set out and circumscribe a particular area with a reasonable degree of precision and particularity. In re

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Johnson, 558 F.2d 1008, 1015, 194 USPQ 187, 193 (CCPA 1977).

In making this determination, the definiteness of the language employed in the claims must be analyzed, not in a vacuum, but always in light of the teachings of the prior art and of the particular application disclosure as it would be interpreted by one possessing the ordinary level of skill in the pertinent art. Id.

The Examiner's focus during examination of claims for compliance with the requirement for definiteness of 35 U.S.C. § 112, second paragraph, is whether the claims meet the threshold requirements of clarity and precision, not whether more suitable language or modes of expression are available. Some latitude in the manner of expression and the aptness of terms is permitted even though the claim language is not as precise as the Examiner might desire. If the scope of the invention sought to be patented cannot be determined from the language of the claims with a reasonable degree of certainty, a rejection of the claims under 35 U.S.C. § 112, second paragraph, is appropriate.

Here, the Examiner cites one example of the claims being vague and indefinite, where he alleges that the term "one

bit... decoders" is misleading. See Examiner's Answer at page 4. The Examiner states that "[it] is not clear whether or not one bit of data is input to the decoder for decoding thereof. If it is the case, it is not clear how a decoder can decode a single bit." Id. Appellants make a reference to page 8, lines 7 to 12 of the Specification for an explanation of the one bit decoder. See Brief at page 8. Appellants conclude that, id.

An n-bit decoder is a decoder that is n bits wide. Thus, an n-bit decoder is capable of processing n bits of data at a time, or within a given clock cycle. A one bit decoder is capable of processing one bit of data at a time, or within a given clock cycle. A one bit decoder is capable of processing one bit at a time. As discussed above, each decoder of [Hamming code decoders] receives one bit at a time. Thus, each decoder is a one bit decoder. Consequently, when read in light of the specification, the term "one bit decoder" is clear and definite.

According to the guidelines above, some latitude in the manner of expression and aptness of terms is permitted even though the claim language is not as precise as the examiner might desire.

Here the scope of the invention which is being sought to be patented can be determined from the language of the claims

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in the light of the Specification. Therefore, we cannot sustain rejections of claims 1 to 10 and 12 to 14 under 35 U.S.C. § 112, second paragraph.

In rejecting a claim under 35 U.S.C. § 103, an Examiner is under a burden to make out a prima facie case of obviousness. If that burden is met, the burden of going forward then shifts to the Applicants to overcome the prima facie case with argument and/or evidence. Obviousness is then determined on the basis of the evidence as a whole and the relative persuasiveness of the arguments. See In re Oetiker, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992); In re Hedges, 783 F.2d 1038, 1039, 228 USPQ 685, 686 (Fed. Cir. 1986); In re Piasecki, 745 F.2d 1468, 1472, 223 USPQ 785, 788 (Fed. Cir. 1984); and In re Rinehart, 531 F.2d 1048, 1052, 189 USPQ 143, 147 (CCPA 1976).

We are further guided by the disclosure of our reviewing court that the limitations from the disclosure are not to be imported into the claims. In re Lunderberg, 244 F.2d 543, 113 USPQ 530 (CCPA 1957); In re Queener, 796 F.2d 461, 230 USPQ 438 (Fed. Cir. 1986). We also note that the arguments not made separately for any individual claim or claims are

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considered waived. See 37 CFR § 1.192 (a) and (c). In re Baxter Travenol Labs., 952 F.2d 388, 391, 21 USPQ 2d 1281, 1285 (Fed. Cir. 1991) ("It is not the function of this court to examine the claims in greater detail than argued by an Appellant, looking for nonobvious distinctions over the prior art."); In re Wiechert, 370 F.2d 927, 936, 152 USPQ 247, 254 (CCPA 1967) ("This court has uniformly followed the sound rule that an issue raised below which is not argued in that court, even if it has been properly brought here by reason of appeal is regarded as abandoned and will not be considered. It is our function as a court to decide disputed issues, not to create them.")

At the outset, we note the grouping of claims elected by Appellants at page 5 of the Brief. Claims 1 to 7 constitute group 1, claims 8 to 10 constitute group 2, claim 11 constitutes group 3 and claims 12 to 14 constitute group 4. We discuss each group separately.

Claims 1 to 7

These claims have been rejected under 35 U.S.C. § 103 over Bossen at page 5 of the Answer. We take claim 1 as representative of the first group. According to the Examiner,

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Bossen shows all the claimed elements except that it does not explicitly show m one bit Hamming code decoders. The Examiner argues that Bossen, however, suggests five EX-OR gates (17), each is used for each i -th bit of a column of the array. The Examiner concludes that "[i]t would have been obvious to one skilled in the art at the time the invention was made to use the X-OR gates as decoders." Appellants argue, Brief at page 9, that "[a]lthough Bossen does disclose using a decoder having EX-OR gates, Bossen neither teaches nor suggests the use of m parallel one bit Hamming code decoders. . . . A Hamming decoder is not merely a collection of EX-OR gates. A Hamming decoder also does not generate copies of each data bit from the data bits and check bits and compare these copies [as those in Bossen]. . . . In addition, a Hamming decoder combines specific combinations of inputs to decode a data word. No particular combination of inputs is implied from the use of EX-OR gates alone".

We agree with Appellants that the use of EX-OR gates by Bossen does not necessarily imply a Hamming decoder. However, Bossen does show parallel decoder means for error detecting and correcting of an $n \times m$ bit data word. See Figures 6 and

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7. Furthermore, Bossen recognizes the problem of time delays in error detection and correction, the same problem which Appellants are solving in their invention. See column 1, lines 15 to 18. Bossen's system is also designed to provide a new and improved multiple bit correcting system to avoid the time delays. It is applicable to data transmission and storage and especially to parallel data processing systems such as digital computer memories, data paths and other important paths that require a high degree of protection against the introduction of errors. See column 1, lines 27 to 33. Bossen also discloses that the use of Hamming codes was well known, see column 1, lines 8 to 13. Therefore, it would have been obvious to an artisan, for the solution of the problem of time delays in error checking and correcting, to replace the parallel decoders of Bossen with Hamming code decoders. Thus, we agree with the Examiner's overall statement of the rejection that, as claimed, the recited limitations of claim 1 are obvious over Bossen. Therefore we sustain the rejection of claim 1 and its group claims 2 to 7 over Bossen.

Claim 8 to 10

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These claims are rejected over Bossen and Price. We take claim 8 as the representative of this group. The Examiner asserts, Answer at page 6, that these claims are also rejected under the same rationale applied against claims 1 to 7. Appellants' argue, Brief at page 11, that "[a]s discussed with respect to claim 1, Bossen discloses using EX-OR gates to generate independent copies of each data bit from the data bit and checkbits. In contrast, claim 8 recites the use of 'm parallel one bit decoders . . . [used in conjunction with] Hamming error detecting and correction codes' As discussed above, Hamming decoding includes parity generation, syndrome generation, error location, and error correction. A Hamming decoder also combines specific combinations of inputs to decode a data word. Consequently, Bossen neither teaches nor suggests the present invention as recited in claim 8." Appellants further assert that even though Price discloses the use of a syndrome generator and a syndrome decoder, Price is concerned with providing two levels of error detection and correction. According to Appellants, there is no mention in Price of parallel one bit decoders using Hamming decoder detecting and correcting codes in either level. We agree with

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the Appellants' position. In our view, whereas it was known to use Hamming decoders in general for error correction and error checking, the specifics claimed in claim 8, have not been shown by the Examiner to be met by the combination of Bossen and Price. Therefore, the Examiner has not established a prima facie case of obviousness. Therefore we do not sustain the rejection of claim 8 over Bossen and Price. Since claims 9 and 10 depend on claim 8 and contain at least the same limitations as claim 8, we do not sustain the rejection of claims 9 and 10 over Bossen and Price.

Claim 11

The examiner has rejected claim 11 over Bossen and Price. The examiner rejects claim 11 on the same basis as claim 8, at page 6 of the Answer. Appellants argues, Brief at page 13 that "Bossen does not divide a data word into modules and use a bit from each module to form a parity bit. Moreover, Bossen does not locate or correct the errors using Hamming error detecting and correcting code." Moreover, Appellants argue, id., that "there is no indication that Price divides the data word into modules and uses a particular bit in each module to form a parity bit. Thus, neither Price nor Bossen teach or

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suggest dividing a bit word into modules and using the *i*th bit from each module to form a set of parity bits. Consequently, Bossen in combination with Price neither teaches nor suggests the invention as recited in independent claim 11." We agree with Appellants. We are of the view that the Examiner has not established a prima facie case in rejecting claim 11 as the Examiner's suggested combination does not meet the claimed limitation of "using said syndrome bits to locate multiple errors in said bits in said data word in accordance with a Hamming error detecting and correcting code and provide an indication of said located errors; and correcting said multiple errors in said bits in accordance with said Hamming error detecting and correcting code to provide corrected data bits." Therefore, we do not sustain the rejection of claim 11 over Bossen and Price.

Claims 12 to 14

The examiner has rejected claim 12 over Bossen and Price at page 7 of the Examiners' Answer. First we note that, the Examiner discusses a syndrome generator, however, we find that the syndrome generator is not recited in claim 12. However, we consider the rejection of claim 12 as it pertains to the

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recited limitations. Appellants argue, Brief at page 14, that "[b]ecause claim 12 recites error correction means including m parallel one bit decoders that correct errors in accordance with a Hamming error detecting and correcting code, all of the arguments with respect to claims 1 and 8 apply to claim 12 with equal force. Consequently, Bossen in combination with Price does not render claim 12 obvious under 35 U.S.C. § 103." We agree with the Appellants' position. The examiner has not shown how the combination meets the claimed limitation of "second means for detecting multiple errors in each of said modules in accordance with a Hamming error detecting and correcting code; and third means, including m parallel one bit decoders, for correcting multiple errors in each of said modules in accordance with said Hamming error detecting and correcting code." The examiner has not pointed out where these specific teachings are shown in the combination of Bossen and Price. In our view, the examiner has not established a prima facie case of obviousness in the rejection of claim 12. Therefore, we do not sustain the rejection of claim 12 and its dependent claims 13 and 14.

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In summary we have not sustained the rejection of claims 1 to 10 and 12 to 14 under 35 U.S.C. § 112 second paragraph. We have sustained under 35 U.S.C. § 103 the rejection of claims 1 to 4 over Bossen, and of claims 5 to 7 over Bossen and Price. However, we have not sustained the rejection of claims 8 to 14 under 35 U.S.C. § 103 over Bossen and Price.

Accordingly the decision of the Examiner rejecting claims 1 to 14 is affirmed-in-part.

No period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED IN PART

JERRY SMITH)	
Administrative Patent Judge)	
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)	BOARD OF PATENT
JOSEPH F. RUGGIERO)	APPEALS
Administrative Patent Judge)	AND
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PARSHOTAM S. LALL)	

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APJ JERRY SMITH

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DECISION: AFFIRMED IN PART
Send Reference(s): Yes No
or Translation (s)
Panel Change: Yes No
Index Sheet-2901 Rejection(s):

Prepared: May 20, 2002

Draft Final

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