

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 17

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte SHAHIN HEDAYAT
and SURENDRA MANDAVA

Appeal No. 1998-3331
Application No. 08/852,842

ON BRIEF

Before KRASS, BARRETT, and BARRY, Administrative Patent Judges.
BARRY, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134 from the rejection of claims 1, 2, 4-17, 19, and 20. We reverse.

BACKGROUND

The invention at issue in this appeal is a multiprocessor architecture for digital signal processing. A digital signal processor (DSP) is typically a chip optimized to handle certain types of mathematical and control algorithms. Digital filtering is one type of algorithm run on such a DSP.

Figure 2 of the appellants' specification shows a conventional multiprocessor system. The system comprises a plurality of processors 70 having their own instruction and data streams from corresponding memories 80. Each processor can execute its own job instruction stream independently of the other processors when no interaction with another processor is required. An implementation in which one of the processors assigns some of its tasks to another processor, however, requires synchronization between the processors. Such synchronization is usually accomplished using memory-based locking. Specifically, only one access to any memory location can occur in any memory cycle. As a result, substantial bottlenecks are created during communications between the processors.

In contrast, Figure 3 of the specification shows the appellants' multiprocessor architecture. A main DSP 100 resides on a main DSP chip; an auxiliary DSP 200 resides on a filter processor chip. The main and auxiliary DSPs share data memory 300; both DSPs can access all memory in the data space. Although the main DSP's program memory 102 and the auxiliary

DSP's program memory 202 are physically separate, residing on separate chips, the program memory space is set up so that the addresses of the auxiliary DSP's program memory fall within the memory address space of the main DSP. Consequently, the main DSP can write not only to the data memory but can also write to the auxiliary DSP's program memory 202. In contrast, the auxiliary DSP reads instructions only from its own program memory 202. Sharing the data memory and mapping the auxiliary DSP's program memory to the main DSP's program memory reduce communication bottlenecks.

Claim 1, which is representative for our purposes, follows:

1. A multiprocessor computer system, comprising:

a main digital signal processor (DSP);

at least one auxiliary DSP interacting with said main DSP for executing digital signal processing operations;

a data memory shared by said main DSP and one or more auxiliary DSPs,

a main DSP program memory storing program data of said main DSP and processing instructions to be executed by said auxiliary DSP; and

a separate auxiliary DSP program memory mapped into the memory space of said main DSP for storing said processing instructions.

The prior art applied in rejecting the claims follows:

Intrater et al. (Intrater)	5,491,828	Feb. 13, 1996
Diamondstein et al. (Diamondstein)	5,432,804	July 11, 1995.

Claims 1, 2, 4-17, and 19-20 stand rejected under 35 U.S.C. § 103 as being obvious over Intrater in view of Diamondstein. Rather than reiterate the arguments of the appellants or examiner in toto, we refer the reader to the brief and answer for the respective details thereof.

OPINION

In deciding this appeal, we considered the subject matter on appeal and the rejection of the examiner. Furthermore, we duly considered the arguments and evidence of the appellants and examiner. After considering the record, we are persuaded

that the examiner erred in rejecting claims 1, 2, 4-17, 19, and 20. Accordingly, we reverse.

We begin by noting the following principles from In re Rijckaert, 9 F.3d 1531, 1532, 28 USPQ2d 1955, 1956 (Fed. Cir. 1993).

In rejecting claims under 35 U.S.C. Section 103, the examiner bears the initial burden of presenting a prima facie case of obviousness. In re Oetiker, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992).... "A prima facie case of obviousness is established when the teachings from the prior art itself would appear to have suggested the claimed subject matter to a person of ordinary skill in the art." In re Bell, 991 F.2d 781, 782, 26 USPQ2d 1529, 1531 (Fed. Cir. 1993) (quoting In re Rinehart, 531 F.2d 1048, 1051, 189 USPQ 143, 147 (CCPA 1976)).

With these principles in mind, we consider the examiner's rejection and the appellants' argument.

The examiner asserts, "Intrater et al. taught the invention substantially as claimed as claimed including a data processing system comprising: a core processor (18); an auxiliary DSP (16) [sic]; a shared data memory (col. 47, lines 38- 49); a main program memory (16, col.2, lines 55-65) and an

auxiliary program memory (28, col. 16, lines 61-65)."

(Examiner's Answer at 4.) The appellants argue that the memory architecture of the claims "is not shown by either of the references applied by the Examiner." (Appeal Br. at 6.)

"`[T]he main purpose of the examination, to which every application is subjected, is to try to make sure that what each claim defines is patentable. [T]he name of the game is the claim'" In re Hiniker Co., 150 F.3d 1362, 1369, 47 USPQ2d 1523, 1529 (Fed. Cir. 1998)(quoting Giles S. Rich, The Extent of the Protection and Interpretation of Claims--American Perspectives, 21 Int'l Rev. Indus. Prop. & Copyright L. 497, 499, 501 (1990)). Here, claims 1, 2, and 4-10 specify in pertinent part the following limitations: "a data memory shared by said main DSP and one or more auxiliary DSPs, a main DSP program memory storing program data of said main DSP and processing instructions to be executed by said auxiliary DSP; and a separate auxiliary DSP program memory mapped into the memory space of said main DSP for storing said processing instructions." Similarly, claims 11-20 specify in pertinent part the following limitations: "a main DSP program

memory, and an auxiliary DSP with an auxiliary DSP program memory wherein said auxiliary DSP program memory being mapped to said main DSP program memory space, a method of digital signal processing, comprising the steps of: (a) controlling said main DSP to download processing instructions from said main DSP memory to said auxiliary DSP memory ... and (c) controlling said auxiliary DSP to carry out operations to execute said processing instructions." Accordingly, claims 1, 2, 4-17, and 19-20 require storing processing instructions for an auxiliary DSP in a main DSP memory and downloading the instructions from the main DSP memory to an auxiliary DSP memory.

The examiner fails to show a teaching or suggestion of the limitations in the prior art of record. "Obviousness may not be established using hindsight or in view of the teachings or suggestions of the inventor." Para-Ordnance Mfg. v. SGS Importers Int'l, 73 F.3d 1085, 1087, 37 USPQ2d 1237, 1239 (Fed. Cir. 1995)(citing W.L. Gore & Assocs., Inc. v. Garlock, Inc., 721 F.2d 1540, 1551, 1553, 220 USPQ 303, 311, 312-13 (Fed. Cir. 1983)). "It is impermissible to use the claimed

invention as an instruction manual or 'template' to piece together the teachings of the prior art so that the claimed invention is rendered obvious." In re Fritch, 972 F.2d 1260, 1266, 23 USPQ2d 1780, 1784 (Fed. Cir. 1992) (citing In re Gorman, 933 F.2d 982, 987, 18 USPQ2d 1885, 1888 (Fed. Cir. 1991)). "The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." Id. 972 F.2d at 1266, 23 USPQ2d at 1784 (citing In re Gordon, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984)).

Here, the examiner interprets Intrater's ROM 16 as a main program memory and the reference's DSPM RAM 28 as an auxiliary program memory as aforementioned. For its part, Intrater teaches that "[p]rograms and data are stored in the ROM **16** and RAM modules **26**, **28**[,] " col. 7, ll. 25-26, and that the DSPM "RAM **28** is used by the DSPM **12** for fetching commands to be executed

and for reading or writing data that is needed in the course of program execution." Col. 16, ll. 44-48. The examiner has not shown, however, that the programs stored in the ROM are for the DSPM or that the programs are downloaded from the ROM to the DSPM RAM. Relying on Diamondstein only to "teach[] the application of a core processor to digital processors which 'includes microprocessors, microcontrollers, and digital signal processors (DSP)' (col. 2, lines 50-60)[,]" (Examiner's Answer at 5), the examiner fails to allege, let alone show, that the reference cures the deficiency of Intrater.

Because the examiner has not shown that the programs stored in the ROM are for the DSPM or that the programs are downloaded from the ROM to the DSPM RAM, we are not persuaded that teachings from the prior art would have suggested the limitations of "a data memory shared by said main DSP and one or more auxiliary DSPs, a main DSP program memory storing program data of said main DSP and processing instructions to be executed by said auxiliary DSP; and a separate auxiliary DSP program memory mapped into the memory space of said main DSP for storing said processing

instructions" or "a main DSP program memory, and an auxiliary DSP with an auxiliary DSP program memory wherein said auxiliary DSP program memory being mapped to said main DSP program memory space, a method of digital signal processing, comprising the steps of: (a) controlling said main DSP to download processing instructions from said main DSP memory to said auxiliary DSP memory ... and (c) controlling said auxiliary DSP to carry out operations to execute said processing instructions." Therefore, we reverse the rejection of claims 1, 2, 4-17, and 19-20 as being obvious over Intrater in view of Diamondstein.

CONCLUSION

In summary, the rejection of claims 1, 2, 4-17, 19, and 20 under § 103 is reversed.

REVERSED

ERROL A. KRASS)	
Administrative Patent Judge)	
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)	BOARD OF PATENT
LEE E. BARRETT)	APPEALS
Administrative Patent Judge)	AND
)	INTERFERENCES
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LANCE LEONARD BARRY)	
Administrative Patent Judge)	

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