

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 14

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte VLADIMIR KOIFMAN,
YACHIN AFEK,
and
SERGIO LIBERMAN

Appeal No. 1998-2874
Application No. 08/568,718

ON BRIEF

Before HAIRSTON, JERRY SMITH, and BLANKENSHIP, Administrative Patent Judges.

HAIRSTON, Administrative Patent Judge.

DECISION ON APPEAL

This is an appeal from the final rejection of claims 1 through 10 and 12.

The disclosed invention relates to a noise cancellation method and circuit for use with a digital-to-analog converter.

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Claim 1 is illustrative of the claimed invention, and it reads as follows:

1. A noise cancellation circuit for use with a digital signal, comprising:

a plurality of equally weighted cells for receiving the digital signal and for providing an analogue output signal in dependence upon the value of the received digital signal; and switching means for dynamically switching a number of the plurality of cells according to a sequencing scheme, wherein the sequencing scheme comprises a first sequence arranged to switch each of the plurality of cells in a sequential order an equal number of times, and a second sequence arranged to randomly define, using a random number generator, one of the plurality of cells as a starting position for the first sequence, such that low frequency tone generation within the analogue output signal is substantially eliminated.

The references relied on by the examiner are:

van de Plassche 1976	3,982,172	Sep. 21,
van de Plassche 1978	4,125,803	Nov. 14,
Jackson 1993	5,221,926	Jun. 22,

Claims 1 through 10 and 12 stand rejected under 35 U.S.C. § 103 as being unpatentable over the admitted prior art or either of the van de Plassche patents in view of Jackson.

Reference is made to the brief and the answer for the

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respective positions of the appellants and the examiner.

OPINION

The obviousness rejection of claims 1 through 10 and 12 is reversed.

We agree with the examiner (Answer, page 3) that "[t]he admitted prior art and the Van de Plassche patents teach a number of equally weighted dynamic elements, such as current sources, for receiving the digital signal and providing an analog output signal in response, and switching means dynamically switching a number of the plurality of elements (cells) according to a first sequencing scheme, which switches each of the plurality of cells in a sequential order (see page 1 of the Specification . . .)." We also agree with the examiner (Answer, page 4) that:

The patent to Jackson teaches, *inter alia*, a dynamic element matching or "round robin" scheme of component switching which begins each conversion with the cell immediately subsequent to the last cell used in the preceding conversion. Jackson also teaches that "[a]nother known nonlinearity correction technique in digital-to-analog converters, such as capacitor array converters, is to randomize the switching order of the capacitors in the capacitor array" (Jackson, col. 2, lines 5-8). Jackson thus teaches, within the same patent document, the approaches both of selecting the next cell in a predetermined order and selecting the next

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cell in a random order.

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In view of the teachings of the admitted prior art, the van de Plassche patents and Jackson, the examiner concludes (Answer, page 4) that "the person having ordinary skill in the art would have been motivated to synthesize the two approaches disclosed by Jackson, i.e., to switch a number of contiguous conversion cells according to the digital value to be converted, having selected the cell from which to begin using a random number generator, because Jackson teaches that both the 'round robin' approach and the random approach reduce the effects of nonequal component values (see col. 2, line 9, and col. 6, line 68), thus reducing (cancelling) noise."

Although we agree with the examiner that Jackson discloses two different approaches that can be used in the digital-to-analog conversion process, we do not, however, agree with the examiner that the skilled artisan would have known from the teachings of record to combine the two distinctly different approaches as appellants have done in their disclosed and claimed invention. Appellants have correctly argued (Brief, page 5) that "[t]here is no suggestion or even a hint of a suggestion about sequentially

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switching the cells in a sequential order an equal number of times, where the starting position for the sequencing is defined using a random number generator, as claimed in claims 1 and 6" (Emphasis added). In summary, we agree with appellants' argument (Brief, pages 5 and 6) that the examiner has not met his burden of presenting a prima facie case of obviousness.

DECISION

The decision of the examiner rejecting claims 1 through 10 and 12 under 35 U.S.C. § 103 is reversed.

REVERSED

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KENNETH W. HAIRSTON)	
Administrative Patent Judge)	
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JERRY SMITH)	
Administrative Patent Judge)	APPEALS AND
)	
)	INTERFERENCES
)	
HOWARD B. BLANKENSHIP)	
Administrative Patent Judge)	

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KWH:hh

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