

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 44

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte MARK A. LYSINGER

Appeal No. 1998-2712
Application No. 08/478,429

ON BRIEF

Before THOMAS, KRASS, and JERRY SMITH, Administrative Patent Judges.

KRASS, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 1 and 3-16. We note that while the claims appearing in the appendix of the principal brief indicate that claim 4 depends from claim 2, claim 2 has been canceled.

The invention is directed to a content addressable memory (CAM). More particularly, in order to save on the added expense of a comparison circuit in each cell

of the memory array, the instant invention provides a counter and decoder in order to step through contents of the memory one row at a time. The contents of each row are then sequentially supplied to a single comparator to be compared to an input value held in a register. Each time a match is found, the row address of the matching memory row is stored in a stack.

Representative independent claim 1 is reproduced as follows:

1. A content addressable memory, comprising:

a random access memory, organized as a plurality of rows having a preselected number of bits, each row selectable by a row address;

a counter for sequentially generating row addresses to be presented to the random access memory;

a register for storing an input value to be compared to the rows of said memory, said register having a number of bits equal to the number of bits in each random access memory row;

a single comparator for comparing, in sequence, each selected row with the value stored in said register, wherein said comparator compares a row and the value stored in said register in a single step, and for generating a signal indicative of whether a match occurs; and

means connected to said comparator for storing the row addresses generated by the counter for each row which causes a signal indicative of a match to be generated.

The examiner relies on the following references:

Phelps	4,532,606	Jul. 30, 1985
Szczepanek	4,959,811	Sep. 25, 1990
		[filed Nov. 03, 1986]

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Claims 1 and 3-16 stand rejected under 35 U.S.C. § 103 as unpatentable over Szczepanek and Phelps, taken together. Claim 15 stands rejected under 35 U.S.C. §§ 102/103 as anticipated by or, in the alternative, obvious over, Phelps.

Reference is made to the briefs and answer for the respective positions of appellant and the examiner.

OPINION

Turning first to the alternative rejection under 35 U.S.C. §§ 102/103, the examiner contends that Phelps shows a CAM where there are N memory cells per row in the RAM and M in the CAM that are all accessed and compared at the same time due to the common access gate features 51 and 52. It is contended that Phelps teaches a memory to be accessed and compared one row at a time and that Phelps' latch reads on the claimed register. The examiner further contends that it is *inherent* "that all memory arrays and rows and bits in the memory array has '...an identifying address,' otherwise the data could not be accessed and thus would be worthless" [answer-page 3]. The step of "storing the identifying address" is common to all CAMs, contends the examiner. The examiner concludes by indicating that if Phelps' latch is not a "register," as claimed, then it would have been obvious, within the meaning of 35 U.S.C. § 103, to substitute any equivalent type of register for the latch.

With regard to the rejection of claims 1 and 3-16 under 35 U.S.C. § 103, we refer to pages 4-6 of the answer for the examiner's explanation of the rejection.

For his part, appellant contends that there are at least three limitations in the claims which distinguish over the applied prior art:

1. Neither Sczcepanek nor Phelps discloses or suggests a register for storing an input value which has the same number of bits as each memory row.
2. Neither Sczcepanek nor Phelps discloses or suggests a *single* comparator for sequentially comparing an input value to each memory row.
3. Neither Sczcepanek nor Phelps discloses or suggests a means for storing *each* row address in the memory containing data matching the input value.

With regard to the second alleged difference concerning a *single* comparator, it is not entirely clear how appellant's comparator is a *single* comparator, distinct from the comparators of the prior art. It is true that Phelps, for example, includes a comparator in each CAM cell while appellant's comparator (element 20 in Figure 1) is more of a distinct element. However, even appellant's *single* comparator appears to be a series of comparators since each bit in a row must be separately, albeit simultaneously, compared. Accordingly, we are not persuaded by appellant's *single* comparator argument as a distinguishing difference over the applied prior art. Additionally, we note

that independent claim 15 does not even require a *single* comparator or comparison.

With regard to the first alleged difference concerning a register for storing an input value with the same number of bits as each memory row, we disagree for the reasons set forth in our previous decision of December 15, 1993, in Appeal No. 93-3880. At pages 4-5 of that decision, we explained that while Szczepanek contains the statement that the “length of a group of data being considerably less than that of a row” [column 4, lines 57-58], this is but one example set forth by Szczepanek. Since column 4, lines 61-62, of the reference states that “[a]lternatively a group may be larger or smaller than 1 byte,” this would have suggested to the artisan that the input value may very well be the same length as the length of a row in memory. In fact, if one is comparing an input value with a row in memory, the artisan would have found it preferable to compare values of the same length.

With regard to the third alleged difference concerning a means for storing each row address in the memory containing data matching the input value, we agree with appellant that neither Szczepanek nor Phelps teaches or suggests this limitation and, even assuming, arguendo, that the references are combinable, this claimed limitation is not met.

The examiner’s response to this third argument is to point to page 6, lines 2-8, of our earlier decision. We stated thereat that the artisan would have understood that a

match result would have been useless without a way of determining the location of the matched data in memory and, therefore, the artisan would have been led to store the value of a counter keeping track of the shifting operation of Szczepanek in order to identify the location of the match.

The instant claims have been amended from those in the earlier case. In that case, independent claim 1 called for a means connected to the comparator “for storing signals indicative of the occurrence of a match” with dependent claim 2 limiting the storing means to store, “for each indicated match, a counter value identifying which row contained the match.” Each one of the instant claims on appeal recites that the means connected to the comparator is “for storing the row addresses generated by the counter for each row which causes a signal indicative of a match to be generated” or “for storing the identifying row address for each row for which a match occurs between the input signal and any rows of said array” or that “for each row which matches the input value, storing the identifying row address of such row.” Thus, unlike the previous claims, the instant claims all recite and require, more specifically, that a “row address” is stored for each row that matches an input value. We find nothing in either of the applied references, or in a combination thereof, that is suggestive of storing a “row address” of a row when it is determined that a match has been generated by the comparison operation.

In short, we adopt appellant's position, at page 10 of the principal brief, wherein appellant argues that

neither *Szczepanek* nor *Phelps* disclose or suggest [sic, discloses or suggests] use of a memory means for storing the row addresses of each memory row containing data matching the input value. *Szczepanek*, upon finding a match, immediately gates the address of the bit onto the address/data bus. *Phelps* uses a single match line to initiate a shuffle of the matching memory row to the first row in the array. Both *Szczepanek* and *Phelps* assume that only one match will be found in the memory contents. Neither suggest [sic, suggests] providing a means for storing the row addresses of multiple matches.

Accordingly, the examiner's decision rejecting claim 15 under 35 U.S.C.

§§ 102/103 over Phelps and claims 1 and 3-16 under 35 U.S.C. § 103 over Szczepanek and Phelps is reversed.

REVERSED

JAMES D. THOMAS)	
Administrative Patent Judge)	
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)	BOARD OF PATENT
ERROL A. KRASS)	APPEALS
Administrative Patent Judge)	AND
)	INTERFERENCES
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JERRY SMITH)	
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