

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

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| (90/003,191) | Paper No. 77 |
| (90/003,240) | Paper No. 77 |
| (90/003,430) | Paper No. 75 |
| (90/003,874) | Paper No. 75 |

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte SGS-THOMSON MICROELECTRONICS INC.

Appeal No. 98-2447
Reexamination Control No. 90/003,191¹

HEARD: June 23, 1999

¹ Reexaminations ordered for Control Nos. 90/003,191 on September 10, 1993, 90/003,240 on November 1, 1993, 90/003,430 on May 12, 1994 and 90/003,874 on July 5, 1995 for Reexamination of Patent No. 4,553,314, issued November 19, 1985; which is based on Application No. 06/431,527, filed September 30, 1982; which is a division of Application No. 06/351,726, filed February 24, 1982, now abandoned; which is a continuation of Application No. 06/100,606, filed December 5, 1979, now abandoned; which is a division of Application No. 06/002,426, filed January 10, 1979, now abandoned; which is a continuation of Application No. 05/762,398, filed January 26, 1977, now abandoned.

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Before KIMLIN, KRASS and KRATZ, Administrative Patent Judges.

KIMLIN, Administrative Patent Judge.

DECISION ON APPEAL

This is an appeal from the final rejection of claims 1-5 in the merged reexamination proceeding for Control Nos. 90/003,191, 90/003,240, 90/003,430 and 90/003,874. The patent that is subject to this reexamination is U.S. Patent No. 4,553,314 to Chan et al. The examiner has confirmed the patentability of claims 6-15. Claim 1 is illustrative:

1. A method for making a portion of a semiconductor device comprising the steps of:

(a) forming an oxide insulating layer on a surface of a semiconductor substrate,

(b) forming a polysilicon layer on a selected portion of the oxide insulating layer,

(c) selectively etching away portions of the oxide insulating layer using the polysilicon layer as a mask, thereby exposing a surface portion of the substrate previously covered by the oxide insulating layer, and thereby incidentally partially undercutting the polysilicon layer by lateral etching of portions of the oxide insulating layer under a peripheral edge of the polysilicon layer such that the depth of the undercutting is equal to or greater than the thickness of the oxide insulating layer,

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(d) diffusing dopants into the substrate through the exposed substrate portion, and

(e) exposing the substrate to an oxidizing ambient simultaneously to oxidize both the peripheral edge of the polysilicon layer and the exposed substrate surface portion adjoining the lateral undercut region, such that the lateral undercut region is filled by a substrate oxide component and a peripheral edge polysilicon layer oxide component as both oxide components expand and grow in response to the oxidizing ambient.

In the rejection of the appealed claims, the examiner relies upon the following references:

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| Anzai et al. (Anzai) | 3,906,620 | Sep. 23, 1975 |
| Shappir | 3,921,283 | Nov. 25, 1975 |
| Kikuchi (Japanese Kokai patent) | 51-39835 | Oct. 29, 1976 |

J.T. Clemens et al. (Clemens), "Impurity Diffusion in SiO₂ Layers and Related Effects on the MOS Properties of the Si-Gate Technology," Electrochemical Society Spring Meeting Extended Abstracts 125-27 (1974).

T. Agatsuma et al. (Agatsuma), Characterization of Threshold Voltage in P Channel Si Gate Mosfet, Electrochemical Society Spring Meeting Extended Abstracts 415-16 (1975).

Appellant's claimed invention is directed to a method for making a portion of a semiconductor device. The method entails, inter alia, the selected etching of portions of an oxide insulating layer that results in an undesirable

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undercutting of the polysilicon layer which is situated above the oxide insulating layer. Subsequent to diffusing dopants into the substrate, the substrate is exposed to an oxidizing ambient that oxidizes both the peripheral edge of the polysilicon layer and the exposed substrate for the purpose of filling the undercut region with an oxide component. According to appellant, the present invention prevents short circuit problems caused by lateral etching of oxide under a peripheral edge of a polysilicon layer (page 2 of principal brief).

Appellant submits at page 6 of the principal brief that appealed claims 1-5 do not stand or fall together. However, the ARGUMENT section of appellant's brief presents a separate argument only for claim 2. Accordingly, claims 3-5 stand or fall together with claim 1. In re Nielson, 816 F.2d 1567, 1572, 2 USPQ2d 1525, 1528 (Fed. Cir. 1987). See also 37 CFR § 1.192(c)(7) and (c)(8) (1997).

Appealed claims 1-5 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Kikuchi. Claims 1-5 also

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stand rejected under 35 U.S.C. § 102(b) as being anticipated by Shappir. In addition, the appealed claims stand rejected under 35 U.S.C. § 103 as being unpatentable over Kikuchi in combination with Anzai. The examiner has withdrawn the rejection of claims 1-5 under 35 U.S.C. §§ 102 and 103 over Anzai, considered alone.

We have thoroughly reviewed the respective positions advanced by appellant and the examiner, including the extensive declaration evidence presented by appellant. In so doing, we agree with appellant that the § 102 rejection of the appealed claims over Kikuchi and the § 103 rejection over Kikuchi in view of Anzai are not sustainable. However, we will sustain the examiner's rejection of the appealed claims under § 102 over Shappir. Our reasoning follows.

We consider first the rejection of the appealed claims under § 102 over Kikuchi. It is axiomatic that to support a rejection under 35 U.S.C. § 102 a reference must provide a description of all the claimed features. In the present case, the appealed claims require a diffusion of dopants into the substrate before the step of exposing the substrate to an

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oxidizing ambient. However, as appreciated by the examiner, Kikuchi does not disclose such a diffusion step before the thermal oxidation step. The examiner concedes at page 16 of the Answer that "[a]dmittedly, the substrate is doped before the oxidation step is performed in the method of Chan et al. [appellant], whereas the substrate is essentially undoped in the method of Kikuchi." While the examiner further states at page 16 of the Answer that "this difference is not deemed to affect the profile of the regrown oxide which is grown to a thickness at least equal to that of the original gate oxide in both methods," the accuracy of this assertion by the examiner is irrelevant to the § 102 rejection. Manifestly, the lack of a description in Kikuchi of the claimed method steps mandates our reversal of the examiner's rejection.

We now turn to the rejection of the appealed claims under 35 U.S.C. § 103 over the collective teachings of Kikuchi and Anzai. The examiner appreciates that Kikuchi fails to disclose the claimed method of diffusing dopants into the substrate before exposing the substrate to an oxidizing ambient, but the examiner cites Anzai for teaching the

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diffusion of boron into a silicon substrate to form source and drain regions before oxidation of the device to form an oxide layer. Based on the reference teachings, the examiner concludes that:

In light of the teachings of Anzai et al., it would have been obvious to one of ordinary skill in the art that the source/drain diffusion step used to form the source and drain regions in the transistor of Kikuchi could have been performed prior to the thermal oxidation step. [Page 9 of Answer].

Although we admit there is an initial appeal to the examiner's reasoning, appellant has rebutted the examiner's rejection with the Fourth Supplemental Declaration of Dr. Fair, one who has placed on this record considerable credentials of expertise in the art. The Fair Declaration provides scientific reasoning why one of ordinary skill in the art would not have modified the Kikuchi process in such a way that the diffusion step is performed before the thermal oxidation. In particular, Dr. Fair explains that it was well known that the boron concentration at the silicon surface has to be maintained very high in order to make good ohmic contact between metal and silicon for source and drain contacts, and

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"[i]t was also well known that thermal oxidation following a boron diffusion step would have dramatically decreased the boron surface concentration due to redistribution phenomena, including most significantly the phenomenon of segregation" (paragraph 4 of Declaration).

In the face of this weighty testimony by one of considerable skill in the art of making semiconductor devices, the examiner remained silent, merely noting the entry of the Reply Brief. Consequently, in the absence of an effective refutation of the scientific rationale articulated in the Fourth Supplemental Declaration of Dr. Fair, we find that the evidence of nonobviousness presented by appellant outweighs the evidence of obviousness relied upon by the examiner.

The rejection of the appealed claims under 35 U.S.C. § 102 over Shappir is another matter. Appellant does not dispute that Shappir discloses a method for making a portion of a semiconductor device comprising the claimed steps of (a) forming an oxide insulating layer on a surface of a semiconductor substrate, (b) forming a polysilicon layer on a selected portion of the oxide insulating layer, (c)

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selectively etching away portions of the oxide insulating layer using the polysilicon layer as a mask, thereby exposing a surface portion of the substrate previously covered by the oxide insulating layer, (d) diffusing dopants into the substrate through the exposed substrate portion, and (e) exposing the substrate to an oxidizing ambient simultaneously to oxidize both the peripheral edge of the polysilicon layer and the exposed substrate surface portion. It is appellant's position that the reference does not disclose that the selective etching of the oxide insulating layer performs the incidental partial undercutting of the polysilicon layer by lateral etching of portions of the oxide insulating layer under a peripheral edge of the polysilicon layer, and that the exposure of the substrate to an oxidizing ambient effectively fills the lateral undercut region with an oxide component. Appellant contends that since Shappir is silent regarding any incidental partial undercutting of the polysilicon layer and subsequent filling of the undercut region by the thermal oxidation step, it cannot be concluded that Shappir inherently anticipates the claimed method.

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It is well settled that when a claimed process reasonably appears to be substantially the same as a process disclosed by the prior art, the burden is on the applicant to prove with objective evidence that the process of the prior art does not necessarily or inherently possess characteristics attributed to the claimed process. In re Spada, 911 F.2d 705, 708, 15 USPQ2d 1655, 1658 (Fed. Cir. 1990); In re Best, 562 F.2d 1252, 1255, 195 USPQ 430, 433 (CCPA 1977). In the present case, we find sufficient correspondence between the method disclosed by Shappir and appellant's method for making a portion of a semiconductor device to conclude that the examiner has met her burden of establishing a prima facie case of inherency which effectively places upon appellant the burden of proving that the Shappir process does not necessarily achieve the claimed effects. In particular, as pointed out by the examiner, the thermal oxidation step of Shappir produces an oxide layer of 0.1 micron thick, which is the same thickness as the underlying oxide insulating layer. Based on this disclosure, the examiner makes the factual determination that "although

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Shappir does not expressly state that oxide layer 39 will fill the undercut, since oxide layer 39 is formed to the same thickness as gate insulating layer 36, it must necessarily fill the undercut" (page 23 of Answer). Since we find no refutation of the examiner's reasoning in the principal or reply briefs on appeal, we will accept the examiner's finding as unchallenged fact. In re Fox, 471 F.2d 1405, 1407, 176 USPQ 340, 341 (CCPA 1973); In re Kunzmann, 326 F.2d 424, 425 n.3, 140 USPQ 235, 236 n.3 (1964). Also, we note that appellant has pointed to no particular differences in operating parameters between the thermal oxidations of the present invention and Shappir. In addition, appellant has not demonstrated, nor even asserted, that the claimed filling in of the undercut regions is only effected by thermal oxidation when the process is performed within a certain set of operating conditions, such that it cannot be reasonably concluded that any thermal oxidation of a layer to the same thickness as the gate insulating layer would necessarily fill in the undercut areas.

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Also, we note that there is really no dispute that the etching step of Shappir produces an undercut region in the oxide insulating layer. Like appellant, Shappir employs a buffered HF solution to perform the etching step. In the way of an acknowledgment that the etching step of Shappir would necessarily produce an undercut region, appellant states at page 29 of the principal brief that "Shappir's etching step's use of a buffered solution of HF would appear to inherently introduce an undercut at the edges of the p-channel transistor gate electrode 18. (Col. 9, lines 24-29)." Further, at page 22 of the reply brief, appellant concedes that "[t]he undercut would inherently occur using etching with a buffered HF solution."

Appellant maintains at page 30 of the principal brief that Shappir cannot be considered to inherently anticipate the claimed invention because the reference method would at most fill in the undercut in the p-channel region but not in the n-channel region. However, we fully agree with the examiner that this argument is not germane to the claimed subject matter. The appealed claims are not limited to filling the

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undercut of both the n-channel and p-channel regions but, rather, are sufficiently broad to encompass the performance of the claimed steps in only the p-channel region. We find that such breadth is highlighted by the claim recitation of "[a] method for making a portion of a semiconductor device" (emphasis added). As explained by the examiner at page 19 of the Answer, the appealed claims "are not limited to the fabrication of a p-channel or an n-channel transistor," and claimed step (d) "does not specify any particular conductivity type."

Appellant also points out that Shappir attaches no significance to utilizing thermal oxidation rather than pyrolytic deposition in forming the oxide layer 39, and "one first would have had to select the thermal oxidation option for forming the oxide layer 39 with no compelling reason disclosed in Shappir for doing so" (page 30 of principal brief). However, inasmuch as Shappir discloses only two options for forming the oxide layer, and it is well established on this record that thermal oxidation was a conventional technique in the art for depositing such an oxide

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layer, we are satisfied that Shappir provides a description of thermal oxidation within the meaning of 35 U.S.C. § 102.

Appellant also contends at page 31 of the principal brief that "it is evident that Shappir does not even succeed to prevent undercuts at the edges of the p-channel transistor gates because oxide layer 39 does not appear in the final device structure of Figure 2." According to appellant, the reasonable interpretation of the reference is that oxide layer 39 is stripped away by a removal step that would leave undercut gates in place at all transistor sites in the device. However, assuming that this is the case, we concur with the examiner that such argument is also not germane to the claimed subject matter. By virtue of the "comprising" language of the appealed claims, the claims presently under consideration do not preclude any subsequent removal of the thermally-deposited layer after step (e). Moreover, even if the term "comprising" is replaced with the term "consisting of," we are of the opinion that Shappir describes all the claimed steps "for making a portion of a semiconductor device" (emphasis added). Accordingly, we find all appellant's arguments and declaration

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evidence regarding the reintroduction of an undercut region after Shappir's thermal deposition to be irrelevant to the claimed subject matter presently on appeal.

Appellant further maintains at page 32 of the principal brief that "[c]laim 1 recites a method for making 'a semiconductor device,' and Shappir's intermediate structure relied upon by the Examiner is not a semiconductor device in any rational interpretation of the claim language." However, appellant inaccurately quotes claim 1 which actually recites "[a] method for making a portion of a semiconductor device" (emphasis added). Furthermore, as noted by the examiner, the appealed claims are not so limited as reciting that the product of the claimed steps is a completed device. Indeed, appealed claim 2 evidences that further processing is performed on the product of claim 1. In our view, the appealed claims define nothing more than a series of steps performed in the making of a portion of a semiconductor device and, we might add, our view would not be different even if the language "a portion of" was not present in the appealed claims.

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Regarding separately argued claim 2, appellant maintains that the redundant oxide layer of claim 2 is distinct from that disclosed in Shappir because "[t]he 'redundant' oxide layer of Claim 2 corresponds to layer 98 in Figure 24 of the '314 patent" (page 22 of Reply Brief). Again, appellant's argument is not germane to the claimed subject matter which fails to limit the recited redundant oxide layer to layer 98 in the patent specification.

In conclusion, the examiner's rejection of the appealed claims under 35 U.S.C. § 102(b) over Kikuchi is reversed, as is the examiner's rejection under 35 U.S.C. § 103 over the combined teachings of Kikuchi and Anzai. However, based on the foregoing and the reasons well-stated by the examiner, the examiner's rejection of the appealed claims under 35 U.S.C. § 102(b) over Shappir is sustained. Accordingly, the examiner's decision rejecting the appealed claims is affirmed.

Further proceedings in this case may be taken in accordance with 35 U.S.C. §§ 141 to 145 and 306, and 37 CFR §§ 1.301 to 1.304. Note also 37 CFR § 1.197(b). If the patent owner fails to continue prosecution, the reexamination

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proceeding will be terminated, and a certificate under
35 U.S.C. § 307 and 37 CFR § 1.570 will be issued canceling
the patent claim(s), the rejection of which has been affirmed.

AFFIRMED

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| EDWARD C. KIMLIN |) | |
| Administrative Patent Judge |) | |
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| ERROL A. KRASS |) | BOARD OF PATENT |
| Administrative Patent Judge |) | APPEALS AND |
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| PETER F. KRATZ |) | |
| Administrative Patent Judge |) | |

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