THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 15

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte KURT H. WEINER

Appeal No. 1998-1615
Application No. 08/548,928

ON BRIEF

Before JOHN D. SMITH, HANLON and PAK, Administrative Patent Judges.

HANLON, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on an appeal under 35 U.S.C. § 134 from the final rejection of claims 1-19, all of the claims pending in the application. The claims on appeal are directed to a method for producing a silicon doping test structure. Claims 1, 8 and 17 are representative and read as follows:

1. In a method for fabricating a silicon doping test structure having at least one contact therein, the improvement comprising:

providing a patterned overlayer of laser light reflective material having holes in alignment with said at least one contact and with regions of the silicon to be doped.

8. A process for producing a device structure for real-time testing of silicon doping, comprising:
forming a device on a silicon wafer which includes at least one contact,
depositing an oxide layer on the thus formed device,
depositing an overlayer of laser light reflective material on the oxide layer,
patterning the layer of laser light reflective material to form openings in at least the underlying silicon regions to be doped, and
doping the silicon regions, and
annealing the thus doped silicon regions using pulsed laser energy.

17. A process for improving silicon doping test structures, including:
providing an undoped silicon device having at least one ohmic contact therein having an aluminum surface;
depositing an oxide layer over the silicon device;
depositing an aluminum overlayer on the oxide layer,
patterning the overlayer to open up holes to the at least one contact and to critical silicon regions to be doped; and
doping and annealing the silicon regions.

The references relied upon by the examiner are:

Sasaki	4,646,426	Mar. 3, 1987
Ishida et al. (Ishida)	5,316,969	May 31, 1994

The following rejections are at issue in this appeal:

(1) Claims 1-5 and 17 are rejected under 35 U.S.C. § 102(b) as being anticipated by Sasaki.

(2) Claims 6-16, 18 and 19 are rejected under 35 U.S.C. § 103 as being unpatentable over Sasaki and Ishida.

Discussion

The claims on appeal are directed to a method for producing a silicon doping test structure. Claim 1 recites an improvement in a method for making a silicon doping test structure having at least one contact which comprises the step of providing a patterned overlayer of a laser light reflective material having holes in alignment with the contact and with regions of the silicon to be doped. The processes of claims 8 and 17 include the steps of providing an undoped silicon device having at least one contact, depositing an oxide layer on the silicon device, depositing a laser light reflective material overlayer on the oxide layer, and patterning the overlayer to form openings in at least the underlying silicon regions to be doped. According to appellant, the silicon doping test structure monitors uniformity during silicon doping, provides means for determining uniformity of both junction depth and impurity dose in a silicon wafer, and enables measurement, in real time, of the active impurity dose and junction depth of doped junctions. See Specification, p. 2.

Sasaki discloses a method for producing a MOS FET type semiconductor device comprising the following steps (col. 3, line 9-col. 4, line 36; Figures 2 and 3):

(1) Oxidizing a silicon semiconductor substrate 11 by a conventional thermal oxidation method using a silicon nitride layer mask to form a field insulating layer 12 of silicon dioxide;

(2) Removing the mask and oxidizing the silicon substrate 11 by the conventional thermal oxidation method to form a gate insulating layer 13 of silicon dioxide;

(3) Forming an aluminum layer on the gate insulating layer 13 and on the field insulating

layer 12 by a conventional vapor depositing method;

(4) Selectively removing the aluminum layer by a photoetching method to form a gate electrode 14;

(5) Introducing donor impurities into the silicon substrate 11 through the gate insulating layer 13 by a conventional ion-implantation method to form doped regions 15 and 16;

(6) Annealing the doped regions 15 and 16 with a laser beam;

(7) Forming an insulating layer 17 of, for example, phosphosilicate glass, by a conventional chemical vapor deposition method;

(8) Selectively etching the insulating layer 17 and the gate insulating layer 13 by a photoetching method to form contact holes on the doped regions 15 and 16 and on the gate electrode 14;

(9) Forming a conductive layer of, for example, aluminum, on the insulating layer 17 by a vapor deposition method; and

(10) Patterning the conductive layer by a photoetching method to form interconnection lines for drain, gate and source 18a, 18b and 18c.

Ishida discloses a method for forming shallow junctions in semiconductor devices using gas immersion laser doping. Specifically, the method includes the following steps:

(1) masking the surface of a semiconductor wafer with a reflective material such as aluminum;

(2) immersing the semiconductor wafer in an atmosphere containing a dopant; and

(3) irradiating the semiconductor wafer with a laser beam.

Appellant argues that "Sasaki is totally devoid of any teaching relating to a silicon doping test

structure" (Brief, pp. 8-9). However, the examiner urges that (Answer, p. 5):

> Sasaki shows doped regions having a particular resistivity and annealing the device to vary the resistivity. Sasaki uses laser energy, heating and annealing to try to attain the optimal resistivity desired for the intended process; hence, a testing structure has been disclosed.

The examiner's position is not persuasive. To the extent that the semiconductor device of Sasaki includes doped regions having varying degrees of resistivity, the examiner has failed to establish that the device of Sasaki is a "silicon doping test structure" as claimed. See In re Oetiker, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992) (the examiner bears the initial burden of establishing a prima facie case of unpatentability).

Additionally, each of claims 1, 8 and 17 requires a silicon doping test structure comprising "at least one contact." The examiner has failed to address this limitation. On the other hand, appellant appears to interpret Sasaki as suggesting that at least gate electrode 14 of Figure 5 is "a contact" and aluminum layers 18a, 18b and 18c constitute the "overlayer of laser light reflective material" as claimed. See Brief, p. 9; compare Answer, p. 5, lines 10-18.

Interpreting Sasaki as proposed by appellant, the teachings of Sasaki fail to suggest the following steps (emphasis added):

(a) "providing a patterned overlayer of laser light reflective material having holes in alignment with said at least one contact and with regions of the silicon to be doped" (claim 1);

(b) "patterning the layer of laser light reflective material to form openings in at least the underlying silicon regions to be doped" (claim 8); and

(c) "patterning the [aluminum] overlayer to open up holes to the at least one contact and to critical silicon regions to be doped" (claim 17).

In contrast to the claimed invention, the silicon regions of Sasaki have already been doped at the time the aluminum overlayer is patterned to form interconnection lines 18a, 18b and 18c (Figure 5). See col. 3, lines 26-31. The teachings of Ishida fail to cure the deficiencies of Sasaki.

For the reasons set forth above, the decision of the examiner is reversed.

REVERSED

JOHN D. SMITH Administrative Patent Judge	)
ADRIENE LEPIANE HANLON Administrative Patent Judge	) BOARD OF PATENT) APPEALS) AND) INTERFERENCES
CHUNG K. PAK Administrative Patent Judge	)

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