

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 39

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte GEORGE B. TUMA, WADE B. TUMA and ROBERT E. WARNE

Appeal No. 1998-1119
Application No. 08/482,924

ON BRIEF

Before THOMAS, HAIRSTON, and KRASS, Administrative Patent Judges.

HAIRSTON, Administrative Patent Judge.

DECISION ON APPEAL

This is an appeal from the final rejection of claims 63 and 77 through 81. In a submission under 37 CFR § 1.129(a), claims 63 and 79 through 81 were amended.

The disclosed invention relates to a method for correcting single bit hard errors in a stored digital data word of "n" bits.

Claim 81 is illustrative of the claimed invention, and it reads as follows:

81. A method for correcting single bit hard errors in a stored digital data word of "n" bits, where n is a selected integer, comprising the steps of:

a) storing only said digital data word and a parity bit, said digital data word being stored in a selected storage location of a memory in response to a write command from a system including said memory;

b) reading said stored digital data word from said selected storage location of said memory in response to a read command from said system wherein said read command is issued subsequent to said write command and after said write command is completed;

c) inverting said read digital data word upon detection of an error in said read digital data word;

d) writing said inverted digital data word to said selected storage location in said memory;

e) reading said inverted digital data word from said selected storage location in said memory immediately after said writing; and

f) inverting said inverted digital data word retrieved from said selected location in said memory to obtain said digital word without an error.

The references relied on by the examiner are:

Knauft et al. (Knauft)	3,768,071	Oct. 23,
1973		
Burghard et al. (Burghard)	4,117,458	Sept. 26,
1978		

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Claims 63 and 77 through 81 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Burghard in view of Knauft.

Reference is made to the brief and the answer for the respective positions of the appellants and the examiner.

OPINION

The obviousness rejection of claims 63 and 77 through 81 is reversed.

The prior art portion of Burghard (column 1, lines 18 through 28) discloses that it is known to store parity bits with data bits. The integrity of the data bits is determined by generating a set of parity bits from the recovered data bits and comparing the new parity bits with the previously encoded parity bits. If the new parity bits are identical to the previously encoded parity bits, then error free data is recovered. In the preferred embodiment of Burghard (column 5, lines 33 through 42), a previously encoded word is retrieved from memory and decoded to provide a new set of parity bits. The new parity bits are compared with the parity bits retrieved from memory and, if there is complete agreement, the data is assumed to be error free. If the two sets of parity

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bits do not agree, then the data is subjected to error correction.

In the error detection scheme disclosed by Knauft, a stored word is read immediately after it is stored (Abstract). According to Knauft (column 3, lines 20 through 26), each word that is stored is accompanied by a parity bit and a marking bit which indicates whether the word was stored in inverted form or not. "When the word is read later on, it is again inverted by virtue of the marking in the additional storage element to retrieve the original correct information supplied" (Abstract).

Based upon the teachings of Burghard and Knauft, the examiner is of the opinion (answer, page 5) that "it would have been obvious to a person of ordinary skill in the art to correct Burghard's parity bit detected error by Knauft's method as suggested by both of them so that error free data can be obtained from defective memory locations."

Appellants argue (brief, page 17) that:

Thus, Applicants store only a parity bit and the corresponding digital data word. As noted above, Burghard stores multiple parity bits and so teaches away.

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Moreover, as noted above, Knauft also teaches a completely different storage process and the use of multiple bits, a parity bit and a marking bit.

Appellants argue (brief, page 14) that "[t]he only commonality in the two references is that both use multiple bits to correct memory errors." According to appellants, the disclosed and claimed invention only uses a single parity bit that is stored with the data word (brief, page 8). Another argument made by appellants is that the motivation presented by the examiner for making the modification to Burghard "does not explain how to selectively choose process steps from Knauft and interpose those process steps on Burghard that stores multiple parity bits and not a marking bit and a parity bit" (brief, page 15). Finally, appellants argue (brief, page 15) that "the only motivation or basis for the modifications to the references suggested by the Examiner is Applicants' specification."

We agree with appellants' arguments. The examiner has failed to set forth a convincing line of reasoning for finding that the specifically recited steps in the claims on appeal would have been obvious over the teachings of Burghard and Knauft. Even if the disparate teachings of the references are

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combined, the combined teachings of the references would still require the storage of more than one other bit (e.g., parity/marking) with the data word. In short, the examiner has failed to present a prima facie case of obviousness.

DECISION

The decision of the examiner rejecting claims 63 and 77 through 81 under 35 U.S.C. § 103(a) is reversed.

REVERSED

JAMES D. THOMAS)	
Administrative Patent Judge)	
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)	BOARD OF PATENT
KENNETH W. HAIRSTON)	APPEALS
Administrative Patent Judge)	AND
)	INTERFERENCES
)	
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DECISION: REVERSED
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OB/HD GAU

PALM / ACTS 2 / BOOK
DISK (FOIA) / REPORT