

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 37

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte YU-LAM HO

Appeal No. 1998-1069
Application No. 08/259,575

ON BRIEF

Before HAIRSTON, BARRETT, and FLEMING, Administrative Patent Judges.

FLEMING, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 54 and 56-61,¹ all of the claims ending in the present application. Claims 1-53 and 55 have been canceled.

The invention relates to a method of fabricating a MOS device (specification, page 4, lines 3-7). A first well of a

¹ At section 4 of the Supplemental Examiner's Answer the Examiner noted that the amendment after final rejection filed on June 14, 1996, as Paper No. 25, was entered. As this amendment canceled claim 55, the rejection at issue thus includes only claims 54 and 56-61.

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first conductivity type (n-type) (figure 6, item 19) and a second well of a second conductivity type (p-type) (figure 6, item 25) have exposed surfaces on a semiconductor substrate (figure 6, item 11). These two wells are formed at implant energies between about 150 and 400 keV (figures 1B and 1G). An oxide layer (figure 6, item 35') is provided contiguous to the exposed surfaces of the first and second wells, and a first gate structure (figure 6, item 71B) and a second gate structure (figure 6, item 71A) are provided contiguous to the oxide layer and overlying central portions of the first and second wells.

A first LDD implant is performed with ions of the first conductivity type (n-) having ion kinetic energy of at least about 70 keV and an ion dose in the range of about 5×10^{12} - 5×10^{13} atoms/cm² (specification, page 14, lines 13-15) concurrently in the first and second wells, such that portions of the second well that do not underlie the second gate structure are converted to a first LDD layer of a first conductivity type (figure 6C).

The second well and the second gate structure are then protected from ion implantation (figure 6E). A second LDD

implant is performed with ions of a second conductivity type (p-) having ion kinetic energies of at least about 70 keV and an ion dose in the range of about 7×10^{12} - 5×10^{14} atoms/cm²

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(specification, page 14, lines 27-32). The second LDD implant is conducted in the first well such that portions of the first well that do not underlie the first gate structure are converted to second LDD layers of a second conductivity type. Separate implants are then performed in the first and second wells with ions having ion kinetic energy of at least about 40-180 keV and an ion dose in the range of 10^{15} - 10^{16} atoms/cm² to form completed sources and drains in the first and second wells (specification, page 15, lines 4-7; figures 6J and 6L)

Independent claim 54 is reproduced as follows:

54. A method of fabricating a device on a semiconductor substrate, the method comprising the following steps:

providing a first well of a first conductivity type and a second well of a second conductivity type that is opposite the first conductivity type, both the first and second wells having exposed surfaces on the semiconductor substrate, the first and second wells being formed at implant energies between about 150 and 400 keV;

providing an oxide layer on the exposed surfaces of the first and second wells;

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providing a first gate structure and a second gate structure on the oxide layer and overlying central portions of the first and second wells, respectively;

performing a first LDD implant with ions of the first conductivity type having an ion kinetic energies of at least about 70 keV and having a first ion dose in the range of about $5 \times 10^{12} - 5 \times 10^{13}$ atoms/cm², said step of performing the first LDD implant being conducted concurrently in the first and second wells such that portions of the second well that do not underlie the second gate structure are converted to first LDD layers of the first conductivity type;

protecting the second well and the second gate structure from ion implantation;

performing a second LDD implant with ions of the second conductivity type having ion kinetic energies of at least about 70 keV and having a second ion dose in the range of about $7 \times 10^{12} - 5 \times 10^{14}$ atoms/cm², said step of performing the second LDD implant being conducted in the first well such that portions of the first well that do not underlie the first gate structure are converted to second LDD layers of the second conductivity type; and

performing separate implants in the first and second wells with ions having ion kinetic energies in the range 40 - 180 keV and having an ion does in the range $10^{15} - 10^{16}$ atoms/cm² to form completed sources and drains in the first and second wells.

The Examiner relies on the following references:

Schwabe et al. (Schwabe) 25, 1985	4,525,378	Jun.
Hsu et al. (Hsu) 1990	4,927,777	May 22,

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Bergonzoni 1991	4,997,782	Mar. 5,
Yamane et al. (Yamane) 1991	5,036,019	Jul. 30,
Ichikawa 1995	5,399,514	Mar. 21,

(filed Apr. 22, 1991)

Claims 54 and 56-61 stand rejected under 35 U.S.C. § 103 as being unpatentable over Schwabe, Bergonzoni, Hsu, Ichikawa and Yamane.²

Rather than reiterate the arguments of Appellant and the Examiner, reference is made to the Brief,³ the Examiner's

² At page 4 of the Examiner's Answer, the Examiner withdrew the final rejection of claims 54-61 under 35 U.S.C. § 112, first paragraph and second paragraph, and the rejection of claim 58 under 35 U.S.C. § 112, fourth paragraph.

³ The Brief was received October 16, 1996

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Answer,⁴ and the Supplemental Examiner's Answer⁵ for the respective details thereof.⁶

OPINION

We will not sustain the rejection of claims 54 and 56-61 under 35 U.S.C. § 103.

The Examiner has failed to set forth a *prima facie* case. It is the burden of the Examiner to establish why one having

⁴ The Examiner's Answer was mailed December 11, 1996.

⁵ The Supplemental Examiner's Answer was mailed March 30, 2001.

At section 4 of the Supplemental Examiner's Answer, the Examiner noted that the amendment after final rejection (Paper No. 25) was entered. This amendment added further limitations to independent claim 54 and dependent claim 61. Appellant has not responded to the Supplemental Examiner's Answer and has presented no arguments as to these additional claim limitations.

Contrary to the Examiner's assertion at section 7 of the supplemental answer, the copy of the appealed claims contained in the Appendix to the brief is not correct as the Examiner has now entered the aforesaid amendment after final. Furthermore, as this amendment canceled claim 55, the rejection at issue can only include claims 54 and 56-61.

⁶ The Reply Brief received February 18, 1997 was not entered, as set forth in the Examiner's letter mailed April 22, 1997. Appellant did not petition to request entry of the Reply Brief. Accordingly, the Reply Brief has not been considered.

ordinary skill in the art would have been led to the claimed invention by the express teachings or suggestions found in the prior art, or by implications contained in such teachings or suggestions. *In re Sernaker*, 702 F.2d 989, 995, 217 USPQ 1, 6 (Fed. Cir. 1983).

On page 9 the brief,⁷ Appellant asserts that the Examiner has formulated the rejection by arbitrarily picking and choosing snippets from each of the five references for hindsight reconstruction of the claimed invention. Appellant notes that while each of the references includes one or more elements in common with the claimed invention, each reference also has elements that are antithetical to the claimed invention, and are completely incongruent with the claimed invention and may just as easily be extracted from the references.

In particular, Appellant notes⁸ that Schwabe does not show a process for creating source and drain regions having LDD tip regions extending from main source and drain regions, and

⁷ Section 2

⁸ Brief, page 10, section 4

therefore cannot show a step of performing a first LDD implant simultaneously in both n-well and p-well regions and a second LDD implant in the first well, such that portions of the first well that do not underlie the gate structure are converted to second LDD layers of a second conductivity type.

As regards the Bergonzoni reference, Appellant asserts⁹ that this reference does not provide a separate step of forming a p-well, and that the source and drain junction implants, as well as the n-well implants, are produced under undefined conditions.

In review of the disclosure of Hsu, Appellant asserts¹⁰ that this reference does not show a step of performing a first LDD implant simultaneously in both n-well and p-well regions, and that no p-well is formed. Appellant also notes that the source and drain implants, and the n-well are formed under undefined conditions.

⁹ Brief, pages 10-11, section 4.2

¹⁰ Brief, page 11, section 4.3

In regard to Ichikawa, Appellant notes¹¹ that this reference does not show a step of performing a first LDD implant simultaneously in both n-well and p-well regions, and the LDD implants are performed at lower energies than required to realize the benefits of the claimed invention.

In review of the disclosure of Yamane, Appellant asserts¹² that the structures formed by the process of Yamane do not have LDDs, and the regions of opposite conductivity type define a structure that is not relevant to the claimed invention. Thus, Appellant posits that this reference does not show a process for creating source and drain regions having LDD tip regions extending from main source and drain regions, and it fails to suggest any implant conditions for comparison against the claims.

As an example of an alternative process gleaned from the references, Appellant provides¹³ one in which no p-well is implanted (as in Bergonzoni, Hsu, and Schwabe), no LDD implant

¹¹ Brief, page 12, section 4.4

¹² Brief, page 12, section 4.5

¹³ Brief, page 13, section 5

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is performed (Schwabe and Yamane), and a first LDD implant is not performed simultaneously in both the NMOS and PMOS regions (as in Schwabe, Ichikawa and Hsu).

In regard to the references wherein no conditions for implants are provided, Appellant notes that it would be equally likely that an artisan would choose other conditions.

Finally, Appellant argues that the cited art fails to teach the desirability of employing relatively high LDD implant energies to overcome problems associated with high channel current densities, and the necessity of forming well regions at high energies to allow LDD implants to be subsequently performed at high energies.

It is the Examiner's position¹⁴ that the methods of Schwabe, Bergonzoni, Hsu, Ichikawa and Yamane individually form CMOS devices, "but taken collectively would suggest to those of ordinary skill in the art that a CMOS device as disclosed by the claimed invention could be formed."

Specifically, the Examiner finds that Schwabe discloses a method of making a semiconductor device that includes forming

¹⁴ Examiner's Answer, page 5; Supplemental Examiner's Answer, page 4

an n-type first well 8 by implanting ions at 160 keV, forming a p-type second well 5 by implanting ions at 160 keV, forming an oxide layer 3 & 7a, and forming first and second gate structures 17. The Examiner then states¹⁵ that Schwabe does not disclose forming first and second gate structures from polysilicon, performing a first LDD implant concurrently into the first and second wells, forming sidewalls, and performing separate implants at 40-180 keV at a dose in the range of 10^{15} - 10^{16} atoms/cm².

The Examiner then adds¹⁶ Bergonzoni's disclosure of forming first and second gate structures 6 from polysilicon, performing a first LDD implant concurrently into the regions where the first and second CMOS transistors are to be formed, and forming sidewalls 8. The Examiner argues that although Bergonzoni does not disclose forming an NMOS device within a p-type well, forming the NMOS device within a p-type well

¹⁵ Final rejection, page 6

¹⁶ Final rejection, page 7

instead of a p-type substrate would have been well known in the art, as it is depicted in figure 7 of Schwabe.

The Examiner then points to Hsu for the teaching of performing the first and second LDD implants at a dosage on the order of 10^{15} - 10^{14} atoms/cm², at implantation energies of 50-170 keV, and at implantation energies of 50-120 keV, and that the use of implant specifications would have been well known to one in the art.

The Examiner then points to Ichikawa's teaching that performing separate implants at 40-[1]80 [sic] keV at a dose in the range of 10^{15} - 10^{16} atoms/cm² would have been well known to one in the art, and as a result the claim implantation energies are *prima facie* obvious based on process optimization as determined through routine experimentation.

In response to Appellant's assertion that Schwabe does not show a process for creating source and drain regions having LDD tip regions extending from main source and drain regions, the Examiner notes¹⁷ Appellant's admission that "a partial solution to the hot electron effect, known in the

¹⁷ Answer, page 5

prior art, is the provision of a lightly doped drain (LDD) structure." Moreover, the Examiner asserts that Bergonzoni's method would have suggested to one of ordinary skill in the art that a CMOS device having an LDD structure could be formed by modifying the method of Schwabe et al.

As regards the issue of ion kinetic energies of Bergonzoni being 60 keV, which is less than the claimed "at least about 70 keV," the Examiner posits that neither Appellant's specification nor any additional evidence suggests to one in the art that 70 keV is critical to the claimed invention. The Examiner thereby finds¹⁸ that the claimed kinetic energy is deemed to be ***prima facie*** obvious based on process optimization as determined through routine experimentation by one of ordinary skill in the art.

In response to Appellant's arguments that Bergonzoni does not show that a p-well is formed, and that in the process of Hsu no p-well is formed, the Examiner points to Schwabe's teaching of the suitability of forming an NMOS transistor

¹⁸ Answer, page 7

within p-well 5 and a PMOS transistor within n-well 8. The Examiner then finds that the combination of Bergonzoni and Hsu, by modifying the method of Schwabe, would have suggested that the formation of a CMOS device having an LDD-type NMOS transistor in a p-well, and an LDD-type PMOS transistor in an n-well, would have been within the ordinary skill of one in the art.

In response to Appellant's assertion that Hsu does not show a step of performing a first LDD implant simultaneously in both n-well and p-well regions, the Examiner points¹⁹ to Bergonzoni's teaching of simultaneous implantation and finds that one of ordinary skill in the art would have been motivated to modify the method of Schwabe using the method of Bergonzoni to form a CMOS device by means of a single additional masking step.

As regards Appellant's assertion that Hsu fails to define conditions for implanting source and drain junctions and the n-well, the Examiner points²⁰ to Ichikawa and finds that it

¹⁹ Answer, page 8

²⁰ Answer, pages 8-9

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would have suggested to one of ordinary skill in the art that the combination of Schwabe and Bergonzoni could be modified by performing separate ion implantations at kinetic energies of 40-180 keV and at implantation dosages in the range of 10^{15} - 10^{16} atoms/cm² to form source and drain junctions 312, 313.

In response to Appellant's assertion that Ichikawa fails to disclose certain steps of the claimed invention, the Examiner states that this reference has been included merely to show that the claimed ion kinetic energies for forming source and drain junctions would have been within the ordinary skill of one in the art.

Finally, the Examiner notes Appellant's assertion that Yamane does not show a process for creating source and drain regions having LDD tip regions extending from main source and drain regions, and fails to suggest any implant conditions for comparison against the claims. In response, the Examiner asserts that Yamane suggests to one skilled in the art that source and drain junctions could be formed using the process steps of forming pattern mask 6 over polysilicon layer 5a, etching polysilicon layer 5a using the pattern mask 6, and performing the first LDD implant while pattern mask 6 is

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present. The Examiner then finds that to prevent ions from reaching gate 5 during the implantation process one skilled in the art would have been motivated to modify the method of Schwabe using the method of Yamane et al.

The Federal Circuit states that "[t]he mere fact that the prior art may be modified in the manner suggested by Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." *In re Fritch*, 972 F.2d 1260, 1266 n.14, 23 USPQ2d 1780, 1783-84 n. 14 (Fed. Cir. 1992), citing *In re Gordon*, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984). However, "[o]bviousness may not be established using hindsight or in view of the teachings or suggestions of the invention." *Para-Ordnance Mfg. v. SGS Importers Int'l*, 73 F.3d at 1087, 37 USPQ2d at 1239, citing *W. L. Gore & Assocs., Inc. v. Garlock, Inc.* 721 F.2d at 1551, 1553, 220 USPQ at 311, 312-13.

We agree with Appellant that the Examiner has failed to set forth a **prima facie** case. The Examiner must establish why one having ordinary skill in the art would have been led to

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the claimed invention by the express teachings or suggestions found in the prior art, or by implications contained in such teachings or suggestions. Except for the Bergonzoni teaching of simultaneous implantation and the motivation to modify the method of Schwabe being to form a CMOS device by means of a single additional masking step, the references of record fail to provide express teachings or suggestions to make the combinations suggested by the Examiner.

We agree with Appellant that while each of the references includes one or more elements in common with the claimed invention, each reference also has elements that are antithetical to the claimed invention, and are completely incongruent with the claimed invention and may just as easily be extracted from the references. The references are directed to a differing method of making MOS devices. The Examiner has apparently selected differing process steps and conditions from each of these references without guidance from express teachings or suggestions in these references.

For example, the Examiner states²¹ that Hsu has been included in the rejection merely to show that ion kinetic energies for an LDD tip implantation process would have been well known to one of ordinary skill in the art, and Ichikawa has been included merely to show that the claimed ion kinetic energies for forming source and drain junctions would have been within the ordinary skill of one in the art. However these references do not disclose that their ion kinetic energies provide improved results, or any other specific reason to incorporate such ion energies in other CMOS fabrication techniques. In addition, Schwabe does not indicate any reason for one to desire ion kinetic energies other than those disclosed by Schwabe. Therefore, the Examiner has selected ion kinetic energies from each of Hsu and Ichikawa without guidance from teachings or suggestions from any of the references.

Our reviewing court requires the PTO to make specific findings on a suggestion to combine prior art references. *In re Dembiczak*, 175 F.3d 994, 1000-01, 50 USPQ2d 1614, 1617-19

²¹ Answer, pages 8 and 9

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(Fed. Cir. 1999). In this regard, we note that the Examiner has made, *inter alia*, the following findings directly related to claim limitations which require more than one reference to obviate(emphasis added):

1) Forming the NMOS device within a p-type well, instead of a p-type substrate would have been well known in the art, as it is depicted in figure 7 of Schwabe;

2) The use of implant specifications would have been well known to one in the art;

3) In view of Ichikawa's teaching, performing separate implants at 40-[1]80 [sic] keV at a dose in the range of 10^{15} - 10^{16} atoms/cm² would have been well known to one in the art, and as a result the claim implantation energies are prima facie obvious based on process optimization as determined through routine experimentation;

4)The claimed kinetic energy is deemed to be prima facie obvious based on process optimization as determined through routine experimentation by one of ordinary skill in the art;

5) The combination of Bergonzoni and Hsu, by modifying the method of Schwabe, would have suggested that the formation of a CMOS device having an LDD-type NMOS transistor in a p-well and an LDD-type PMOS transistor in an n-well would have been within the ordinary skill of one in the art.

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These findings are inadequate as they are conclusory statements based on a conglomeration of the references without reasons for the combinations being provided by the references.

Therefore, we will not sustain the rejection of claims 54 and 56-61 under 35 U.S.C. § 103 as being unpatentable over Schwabe, Bergonzoni, Hsu, Ichikawa and Yamane.

Accordingly, the Examiner's decision is reversed.

REVERSED

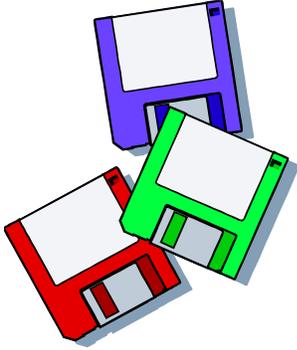
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LEE E. BARRETT)	APPEALS
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DECISION: REVERSED

Prepared: September 20, 2002

Draft Final

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