

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

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Paper No. 41

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES

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Ex parte NAOTO INOUE,  
KENJI AOKI,  
and TAKASHI HOSAKA

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Appeal No. 1998-0970  
Application 07/995,325<sup>1</sup>

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ON BRIEF

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Before JERRY SMITH, BARRETT, and FLEMING, Administrative Patent Judges.

BARRETT, Administrative Patent Judge.

DECISION ON APPEAL

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<sup>1</sup> Application for patent filed December 28, 1992, entitled "Method Of Producing Semiconductor Device," which is a continuation of Application 07/558,459, filed July 27, 1990, now abandoned, which claims the foreign filing priority benefit under 35 U.S.C. § 119 of Japanese Applications 1-194748 and 1-194752, both filed July 27, 1989, and Japanese Application 1-318551, filed December 6, 1989.

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This is a decision on appeal under 35 U.S.C. § 134 from the final rejection of claims 12-15, 20, 22, and 23.

We reverse.

#### BACKGROUND

The disclosed invention relates to a method of filling a contact hole in a semiconductor device with an interposed layer of impurity to achieve a reduction in contact resistance with a subsequently deposited lead pattern layer.

Claim 12 is reproduced below.

12. A method of producing a semiconductor device, comprising:

a) forming an impurity diffusion region having a conductivity type in a surface of a semiconductor substrate;

b) forming an insulating film on the surface of the substrate so that the insulating film covers at least part of the impurity diffusion region;

c) forming a photoresist film on the insulating film;

d) patterning the photoresist film to provide the photoresist film with an opening above the impurity diffusion region;

e) etching the insulating film using the patterned photoresist film as a mask to form a contact hole in the insulating film at the location of the opening in order to expose a part of the impurity diffusion region;

f) removing the patterned photoresist film;

g) removing a natural oxide film from a surface of the impurity diffusion region in the contact hole by reducing with a reactive gas at an ambient temperature of 600-1000E C so as to effect gas-phase etching to activate an exposed surface of the impurity diffusion region;

h) applying a gas containing an impurity component which has same conductivity type as that of the impurity diffusion region to the surface of semiconductor substrate and heating the semiconductor substrate at a temperature of 600-900E C to form an impurity film which contains the impurity component and is adsorbed on the activated exposed surface of the impurity diffusion region and in the contact hole;

i) annealing the impurity diffusion region and the impurity film to diffuse the impurity component from the impurity film to a depth into the impurity diffusion region; and

j) filling the contact hole with an electrically conductive layer to produce electrical contact between the impurity diffusion region and the electrically conductive layer via the impurity film.

The Examiner relies on the following prior art:

1966	Griswold	3,247,032	April 19,
1970	Nickl	3,506,508	April 14,
1988	Tsunashima et al. (Tsunashima)	4,791,074	December 13,
1989	Allman et al. (Allman)	4,855,258	August 8,
1987)			(filed October 22,

Gong et al. (Gong), A metal-oxide-silicon field-effect transistor made by means of solid-phase doping, J. Appl. Phys. 65(11), 1 June 1989, pp. 4435-4437.

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Claims 12-15, 20, 22, and 23 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Tsunashima taken in combination with Nickl, Allman, Gong, and Griswold.

We refer to the Final Rejection (Paper No. 22) and the Examiner's Answer (Paper No. 32) (pages referred to as "EA\_\_") for a statement of the Examiner's position, and to the corrected Appeal Brief (Paper No. 36) (pages referred to as "Br\_\_") for Appellants' arguments thereagainst.

#### OPINION

It is noted that Gong is apparently applied only to the rejection of claims 13 and 15.

Tsunashima discloses a method of manufacturing a semiconductor device. Figure 4 of Tsunashima discloses forming an impurity diffusion region 113 (claim 12, step a) and forming an insulating film 114 covering at least part of the impurity diffusion region (claim 12, step b). Tsunashima does not expressly disclose forming a photoresist film (claim 12, step c), patterning the photoresist film (claim 12, step d), etching the insulating film (claim 12, step e), and then removing the pattern photoresist film (claim 12, step f).

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It is assumed that these steps are conventional.<sup>2</sup> Appellants do not argue steps c) to f) as differences and, thus, we do not consider them. See 37 CFR § 1.192(c)(6)(iv) (1994) ("For each rejection under 35 U.S.C. 103, the argument shall specify the errors in the rejection, the specific limitations in the rejected claims which are not described in the prior art relied on in the rejection, and shall explain how such limitations render the claimed subject matter unobvious over the prior art."). Cf. In re Baxter Travenol Labs., 952 F.2d 388, 391, 21 USPQ2d 1281, 1285 (Fed. Cir. 1991) ("It is not the function of this court to examine the claims in greater detail than argued by an appellant, looking for nonobvious distinctions over the prior art."). Perhaps the reason these limitations are not argued is that the admitted prior art of Figures 2(a)-(c) indicates that these steps were conventional. Appellants' invention is said to be the method of filling the contact hole with an interposed layer of boron to reduce the contact resistance (specification, p. 1).

Tsunashima discloses (col. 2, lines 40-47):

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<sup>2</sup> If the steps are conventional, the Examiner's rejection should say so to indicate that the steps have not been ignored.

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The boron layer is deposited on a silicon substrate or in an opening provided in an insulation layer mounted on the silicon substrate by vacuum evaporation, sputtering, CVD (Chemical Vapor Deposition), etc. The deposition of the boron layer should preferably be made after the natural oxide layer settled on the silicon substrate is etched off by dilute fluoric acid or by the argon sputtering process in a vacuum.

The deposited boron is later diffused by heat treatment (annealing) (claim 12, step i) and the contact hole is filled with an electrically conductive aluminum wire layer 118 (claim 12, step j). The purpose of diffusing boron into the silicon or the impurity diffusion region is to ensure good ohmic contact between the p-type impurity layer 113 and the aluminum wire layer 118 (col. 5, lines 3-7), which is the same as Appellants' reason of reducing the contact resistance (specification, p. 1, lines 6-7).

The differences between Tsunashima and the subject matter of claim 12 are that Tsunashima does not disclose:

(1) specifically removing a natural oxide film from a surface of the impurity diffusion (Tsunashima discloses removing a natural oxide layer from the silicon substrate surface, but does not express mention removing the oxide from the surface of the impurity diffusion region); (2) the specific process step of removing the natural oxide film recited in step g);

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and (3) the specific process step of depositing the boron impurity as recited in step h).

As to difference (1), it is implied by the rejection that it would have been obvious to apply the same natural oxide layer removal step to the impurity diffusion region 113. This difference is not argued and, thus, will not be addressed.

As to difference (2), the Examiner finds that Nickl discloses removal of native oxide using etching agents at 900-1300EC and that Allman discloses removal of native oxide by reaction with HCl or H<sub>2</sub> gas at 800-900EC (EA4). The rejection implicitly concludes that it would have been obvious to use the native oxide removal processes of Nickl or Allman in place of the native removal method in Tsunashima.

Appellants argue that Tsunashima does not disclose any temperatures for the surface cleaning processes, but the two processes (etching with dilute fluoric acid or by argon sputtering in a vacuum) can typically be carried out at low temperature and even room temperature (Br6). It is argued that one skilled in the art would have no reason to combine the teachings of Nickl with Tsunashima in any particular manner because Tsunashima discloses removal of the natural

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oxide layer by a low temperature process (Br7). It is argued that Allman is concerned with preparing a substrate surface for deposition of a silicon nitride layer, whose purpose is to mask active regions during the growth of silicon dioxide dielectric to separate the active regions, not to serve as a source of an impurity component (Br8). Thus, the purpose of Allman is said to be so totally different that one skilled in the art would have found no suggestion in Allman to modify the steps in Tsunashima (Br8). It is argued that the references do not relate to efforts to solve a common problem, and therefore the selection of a step from one reference and the conclusion that it could be employed in the method of another reference is based on hindsight (Br10).

The Examiner states it is not necessary for Allman to disclose removing the native oxide for the same purpose as Applicants (EA4). Otherwise, the Examiner does not respond to Appellants' arguments.

In our opinion, it would have been obvious to one of ordinary skill in the art to use other known native oxide removal processes in the art, such as those disclosed in either Nickl or Allman, in place of the disclosed removal

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processes in Tsunashima to achieve the disclosed benefits of those processes. Appellants do not challenge the finding that Nickl and Allman meet the limitations of step g). Those of ordinary skill in the art must be presumed to know something about the art apart from what the references expressly disclose. In re Jacoby, 309 F.2d 513, 516, 135 USPQ 317, 319 (CCPA 1962). Thus, one of ordinary skill would not have considered Tsunashima limited to its express teachings, but would have had the skill to make modifications such as substituting known alternative processes. The fact that Tsunashima discloses two diverse types of removal processes, etching with dilute fluoric acid and argon sputtering in a vacuum, indicates that the removal process step is not critical. Tsunashima does not disclose that the natural oxide removal process should be carried out at low temperatures and, thus, we find that one skilled in the art would not have been led away from using a high temperature process. The fact that Allman deposits silicon nitride after cleaning, instead of a doping material as in Nickl (col. 3, lines 39-43), would not have discouraged one of ordinary skill in the art from using

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the natural oxide removal process of Allman to prepare the surface.

As to difference (3), the Examiner finds that Griswold teaches deposition of impurity films by decomposition of organic compounds at a suitable temperature to be suitable in the process of Tsunashima (citing col. 5, lines 1-20; col. 7, lines 18-22 and 32-36; and col. 8, lines 4-11) and concludes that it would have been "within the scope of one of ordinary skill in the art to employ the recited temperature range when appropriate in view of this teaching" (EA4).

Appellants argue that Tsunashima does not cite any temperatures for the step of depositing a boron layer on the substrate surface and, while the Tsunashima does mention vacuum evaporation, sputtering, CVD, etc., it is known that these processes can also be carried out at low temperature. It is argued that Griswold discloses the deposition of impurity films of organic compounds at 350°C and that the upper limit of the temperature is the temperature at which the radical group begins to break down, but that this upper limit is not specified (Br9).

The Examiner does not respond to these arguments.

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Griswold discloses a method of diffusing an active impurity into a semiconductor body. An impurity, such as boron, is deposited at relatively low temperatures at which no diffusion of the active impurity material into the semiconductor body can occur (col. 3, lines 13-20). Thereafter, a layer of an oxide of a semiconductor material is deposited over the active impurity material at a relatively low temperature such that no diffusion of the previously deposited active impurity atoms occurs during deposition (col. 3, lines 20-28). Subsequently, the semiconductor material having the layers of active impurity and oxide of semiconductor material thereover is subjected to substantially high temperatures to diffuse the active impurity material into the semiconductor body (col. 3, lines 28-33). The oxide of semiconductor contains the deposited boron material in contact with the exposed surface of the semiconductor material and prevents it from escaping into the atmosphere within the diffusion furnace (col. 7, lines 53-57). Griswold discloses "that the temperatures utilized during the method steps of the present process are quite low, namely, 350E C. for the deposition of the impurity material and 600E C. for the

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deposition of the oxide of semiconductor material" (col. 7, lines 13-17), although the temperatures can be as low as 250E C for deposition of the active impurity (col. 7, lines 68-72) and 500E C for depositing the semiconductor material (col. 7, line 75 to col. 8, line 3). Griswold discloses that the upper limit of the temperatures is the temperature at which the radical group begins to break down, because the breakdown of the radical group causes undesirable products of combustion that contaminate the surface of the semiconductor body (col. 8, lines 4-11).

Although we agree with the Examiner that it would have been obvious to one of ordinary skill in the art to use other conventional processes for depositing the boron layer in Tsunashima, including the process taught in Griswold, Griswold does not disclose a high temperature process of depositing the impurity that meets the claim limitations. In fact, Griswold discloses that the impurity should be deposited at relatively low temperatures (350E C) at which no diffusion of the active impurity material into the semiconductor body can occur (col. 3, lines 13-20), which is contrary to the use of high temperatures of 600-1000E C, as claimed. Griswold also

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teaches away from high temperatures because they can cause breakdown of the radical group leading to undesirable products of combustion and contamination of the semiconductor surface. The Examiner's reasoning that it would have been "within the scope of the art to employ the recited temperature range when appropriate" (EA4) fails to deal with these contrary teachings of Griswold and fails to provide any reason for using a high temperature range not disclosed in Griswold. Thus, the Examiner fails to establish a prima facie case of obviousness. Gong discloses depositing a layer of amorphous silicon, a layer of Sb, and a layer of amorphous silicon followed by annealing. While Gong may disclose putting down a layer of silicon before a layer of impurity material, which is relevant to claim 15, step h), it does not disclose the temperature during deposition of the impurity component and, so, does not cure the deficiency of Tsunashima, Nickl, Allman, and Griswold with respect to the step of depositing an impurity component

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in independent claims 12, 14, and 15. Accordingly, the  
rejection of claims 12-15, 20, 22, and 23 is reversed.

REVERSED

JERRY SMITH	)	
Administrative Patent Judge	)	
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	)	
	)	BOARD OF PATENT
LEE E. BARRETT	)	APPEALS
Administrative Patent Judge	)	AND
	)	INTERFERENCES
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MICHAEL R. FLEMING	)	
Administrative Patent Judge	)	

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