Paper No. 25

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

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Ex parte ROBERT K. DEHAVEN
and
JAMES F. WENZEL

_____

Appeal No. 1998-0908
Application 08/506,292

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ON BRIEF

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Before HAIRSTON, BARRETT, and RUGGIERO, Administrative Patent Judges.

RUGGIERO, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on the appeal from the final rejection of claims 57, 58, and 66-83, which are the only claims remaining in the application. Claims 1-56 and 59-65 have been canceled.

distribution wafer (CDW) in Appellants' specification. A face-to-face connection from the product wafer to the stimulus wafer is made through a compliant interconnect media. External connectors and conductors provided on the stimulus wafer transmit and receive test and control information to and from an external tester.

Claim 57 is illustrative of the invention and reads as follows:

57. A method for stimulating a product wafer using a stimulus wafer, the method comprising the steps of:

providing the product wafer wherein the product wafer comprises a plurality of product integrated circuits which are to be stimulated, the product wafer having a selectively exposed top conductive layer of material coupled to the product integrated circuits;

providing the stimulus wafer wherein the stimulus wafer comprises a plurality of stimulus circuits wherein at least one stimulus circuit within the plurality of stimulus circuits corresponds to one product integrated circuit within the plurality of product integrated circuits, the stimulus wafer having a selectively exposed top conductive layer of material coupled to the stimulus circuits; and

positioning a compliant interconnect media between product wafer and the stimulus wafer, the compliant interconnect media coupling the selectively exposed top conductive layer of material

The Examiner relies on the following prior art:

Moriya	4,766,371	Aug. 23, 1988
Kwon et al. (Kwon)	5,070,297	Dec. 03, 1991
King et al. (King '405)	5,140,405	Aug. 18, 1992
Kreiger et al. (Kreiger)	5,210,485	May 11, 1993
Tuckerman et al. (Tuckerman)	5,397,997	Mar. 14, 1995
		(filed May 06, 1993)
King et al. (King '241)	5,440,241	Aug. 08, 1995
		(filed Mar. 06, 1992)
Yamada et al. (Yamada)	5,497,079	Mar. 05, 1996
		(filed Aug. 31, 1993)
Charlton et al. (Charlton)	5,523,696	Jun. 04, 1996
		(filed Dec. 07, 1993)

Claims 57, 58, and 66-71 stand finally rejected under 35 U.S.C. § 112, first paragraph, as being based on an inadequate disclosure. Claims 57, 58, and 66-83 stand finally rejected under 35 U.S.C. § 102(e) as being anticipated by King '405 or King '241. Claims 57, 58, and 66-83 further stand finally rejected under 35 U.S.C. § 103(a) as being unpatentable over King '405 or King '241, in the alternative, in view of Moriya. In a separate 35 U.S.C. § 103(a) rejection, claims 57, 58, and 66-83 stand finally rejected as being unpatentable over King '405 or King '241 in view of Kreiger, Yamada, or Charlton, further in view of Kwon or Tuckerman, and further in view of Moriya. In

Rather than reiterate the arguments of Appellants and the Examiner, reference is made to the Brief (Paper No. 15) and Answer (Paper No. 16) for the respective details thereof.

OPINION

We have carefully considered the subject matter on appeal, the rejections advanced by the Examiner, the arguments in support of the rejections and the evidence of anticipation and obviousness relied upon by the Examiner as support for the prior art rejections. We have, likewise, reviewed and taken into consideration, in reaching our decision, Appellants' arguments set forth in the Brief along with the Examiner's rationale in support of the rejections and arguments in rebuttal set forth in the Examiner's Answer.

It is our view, after consideration of the record before us, that the disclosure in this application describes the claimed invention in a manner which complies with the requirements of the first paragraph of 35 U.S.C. § 112. We are also of the view that the disclosures of King '241 or King '405 do not fully meet the

of skill in the particular art would have suggested to one of ordinary skill in the art the obviousness of the invention as set forth in claims 57, 58, 68-72, 75-80, and 83. We reach the opposite conclusion with respect to the obviousness of the invention set forth in claims 66, 67, 73, 74, 81, and 82. Accordingly, we affirm-in-part.

As to the issue of whether the four additions to the specification in the amendment filed April 28, 1997 (Paper No. 11) are new matter under 35 U.S.C. § 132, we find that the first three additions (after line 12 on page 6, after line 11 on page 12, and after line 7 on page 13) do not directly or indirectly affect the claims before us. The issue of new matter as to these three additions is therefore a petitionable issue under 37 CFR § 1.181 and not an appropriate matter for decision by the Board.

The fourth addition to the specification (after line 19 on page 15) involving the use of voltage and current "limiting" terminology as opposed to the original "blocking" language is, on

Appellants, the terms "blocking" and "limiting" are essentially synonymous as urged by Appellants and, therefore, the addition of "limiting" language to the specification does not constitute new matter. The original disclosure described the operation of current and voltage blocking circuitry 54 and 58 as operating in conjunction with voltage and current monitoring circuitry 56 and 60 to shut down power to integrated circuits under test which experience abnormal current and voltage levels. In our view, the skilled artisan would recognize that the functions of voltage and current "limiting" circuitry would include the turn off or partial turn off of power to affected circuits in accordance with Appellants' original "blocking" disclosure.

We consider next the Examiner's rejection of claims 57, 58, and 66-71 under the "written description" requirement of the first paragraph of 35 U.S.C. § 112. "The function of the description requirement [of the first paragraph of 35 U.S.C. § 112] is to ensure that the inventor has possession, as of the filing date of the application relied on, of the specific subject

initial burden of presenting evidence or reasons why persons skilled in the art would not recognize in an Applicants' disclosure a description of the invention defined by the claims. Wertheim, 541 F.2d at 265, 191 USPQ at 98. After reviewing the arguments of record before us, however, it is our opinion that the Examiner has not provided sufficient reasons or evidence to satisfy such burden.

The Examiner asserts (Answer, page 9) a lack of support in Appellants' original disclosure for the passage ". . . the compliant interconnect media being a contiguous film of dielectric material" in the last three lines of independent claim 57. In the Examiner's view, the textual matter in the specification does not support such claim language and the illustration in Figure 1 is inconclusive since views of other cross-sections of the interconnect material might reveal a series of discontinuities. Our review, however, of the description of the structure of Appellants' compliant interconnect at page 9 of the specification, along with a consideration of Figure 1 of the

rather than segmented across both the product wafer and the stimulus wafer. "It is not necessary that the application describe the claim limitations exactly, . . . but only so clearly that persons of ordinary skill in the art will recognize from the disclosure that Appellants' invented processes included those limitations." Wertheim, 541 F.2d at 262, 191 USPQ at 96, citing In re Smythe, 480 F.2d 1376, 1382, 178 USPQ 279, 284 (CCPA 1973).

In view of the above discussion, it is our conclusion that, under the factual situation presented in the present case, the statutory written description requirement has been satisfied because Appellants were clearly in possession of the invention at the time of filing of the application. Therefore, we do not sustain the rejection of claims 57, 58, and 66-71 under the first paragraph of 35 U.S.C. § 112.

Turning to a discussion of the Examiner's rejection of claims 57, 58, and 66-83 under 35 U.S.C. § 102(e) as being anticipated by King '405 or King '241, we note that anticipation is established only when a single prior art reference discloses,

1440, 1444, 221 USPQ 385, 388 (Fed. Cir.); cert. dismissed, 468 U.S. 1228 (1984); W.L. Gore & Assocs. v. Garlock, Inc., 721 F.2d 1540, 1554, 220 USPQ 303, 313 (Fed. Cir. 1983), cert. denied, 469 U.S. 851 (1984).

With respect to the reliance on King '241 as the basis for the 35 U.S.C. § 102(e) rejection, the Examiner attempts (Answer, page 5) to read the various limitations of the appealed claims on the disclosure of King '241. In the Examiner's view, the testing arrangement of King '241, which includes product wafer 12, compliant interconnect 13, 16, and test wafer 20, meets all of the fundamental limitations of the claims on appeal. Similarly, with respect to King '405, the Examiner makes particular reference to the description beginning at column 5, line 65 of the embodiment illustrated in Figures 8-11. According to the Examiner, this embodiment of King '405 discloses opposing product and test wafers mounted across an elastomer interconnect as claimed by Appellants.

After reviewing the King '241 and King '405 references,

compliant interconnect media have a ". . . plurality of conductive fibers formed therethrough." In contrast, each of the King references utilizes conductive balls or spheres (King '241, column 6, line 18; King '405, Figure 12) to provide a conductive path through the interconnect insulating material. We would also point out that the Examiner has as least impliedly recognized this distinction by applying the Moriya reference to address this deficiency in the 35 U.S.C. § 103(a) rejection discussed infra. Accordingly, since all of the claimed limitations are not disclosed by King '241 or King '405, or inherent therein, the Examiner's 35 U.S.C. § 102(e) rejection of independent claims 57, 72, and 80, as well as claims 58, 66-71, 73-79, and 81-83 dependent thereon, is not sustained.

Turning our consideration to the Examiner's initial 35 U.S.C. § 103(a) rejection of the appealed claims 57, 58, and 66-83 based on the combination of King '241 or King '405 in view of Moriya, we note that as a general proposition in an appeal involving a rejection under 35 U.S.C. § 103, an Examiner is under

evidence as a whole and the relative persuasiveness of the arguments. See In re Oetiker, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992); In re Hedges, 783 F.2d 1038, 1039, 228 USPQ 685, 686 (Fed. Cir. 1986); In re Piasecki, 745 F.2d 1468, 1472, 223 USPQ 785, 788 (Fed. Cir. 1984); and In re Rinehart, 531 F.2d 1048, 1052, 189 USPQ 143, 147 (CCPA 1976).

With respect to independent claim 57, the Examiner proposes to modify either of the King '241 or King '405 references with Moriya, suggesting (Answer, pages 5 and 6) that Moriya corrects any deficiencies in the King references in disclosing a compliant interconnect with conductive fibers. In the Examiner's view (final Office action mailed July 23, 1997, Paper No. 12), the skilled artisan would have found it obvious to use fine wires instead of conductive particles in an interconnect structure to achieve a more reliable contact through the use of solid conductors.

After reviewing the prior art references in light of the arguments of record, it is our view that the Examiner's analysis

Examiner's prima facie case of obviousness. Any arguments which Appellants could have made but elected not to make in the Briefs have not been considered in this decision (note 37 CFR § 1.192).

Appellants' response initially attacks (Brief, pages 12-18) the relevance of the disclosures of the primary King '405 and King '241 references to the claimed subject matter. As to King '405, Appellants' arguments focus on their contention that, in contrast to the "testing" limitations in the appealed claims, King '405 is not concerned with testing at all. With regard to King '241, Appellants' arguments center on the assertion that, although King '241 discloses circuit testing, there is only one wafer involved, in contrast to the claimed two-wafer test system. In making this assertion, Appellants contend that the only wafer disclosed in King '241 is "product" wafer 12, with interconnect element 13 constructed only of passive material with no active circuitry that could support its characterization as a second wafer as claimed.

We do not find either of these arguments of Appellants to be

application are to be given their broadest reasonable interpretation consistent with the specification, and that claim language should be read in light of the specification as it would be interpreted by one of ordinary skill in the art. In re Sneed, 710 F.2d 1544, 1548, 218 USPQ 385, 388 (Fed. Cir. 1983). Moreover, limitations are not to be read into the claims from the specification. In re Van Geuns, 988 F.2d 1181, 1184, 26 USPQ2d 1057, 1059 (Fed. Cir. 1993), citing In re Zletz, 893 F.2d 319, 321, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989). We find no language in the appealed claims which limit them to "testing", rather, Appellants instead have used the terminology "stimulating a product wafer" and "providing the stimulus wafer". In our view, the conductive pads 16 on the interconnecting plate 15 in King '405, which are registered with conductive pads 12 on the die 10 and are interconnected by conductive traces 17 to each other and to I/O connections, clearly serve to "stimulate" the die conductive pads (King '405, column 4, lines 16-35). We would further point out that Appellants' specification (page 5, line

As to King '241, we note that the interconnect member 13 is disclosed as being either a discrete element or an interconnect pattern integrated or formed on top of integrator substrate 20 (King '241, column 5, lies 58-65). King '241 further illustrates, in Figure 3, active circuitry on substrate 20 which includes interconnect pads 60 connected to surface leads 74-82. Given this disclosure, we fail to see what characteristic of substrate 20 in King '241 would justify Appellants' position that it is not a "wafer" as claimed.

We are equally unpersuaded by Appellants' further arguments which (Brief, page 20) attack the Examiner's establishment of proper motivation for the proposed combination of either of the King references with Moriya. Appellants assert that Moriya is concerned with the testing of packaged integrated circuits, in contrast to King '241 which tests on a wafer scale level and King '405 which, in their view, describes no testing at all. Contrary to Appellants' contention, we do not interpret the Examiner's position as suggesting the bodily incorporation of

interconnect teachings of Moriya to the structure of either of the King references, regardless of whether Moriya is concerned with integrated circuit packages or wafer scale technology as with Appellants' claimed invention. "The test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference. . . . Rather, the test is what the combined teachings of those references would have suggested to those of ordinary skill in the art." In re Keller, 642 F.2d 413, 425, 208 USPQ 871, 881 (CCPA 1981). See also In re Sneed, 710 F.2d 1544, 1550, 218 USPQ 385, 389 (Fed. Cir. 1983) and In re Nievelt, 482 F.2d 965, 967, 179 USPQ 224, 226 (CCPA 1973).

For the above reasons, it is our opinion that, since the Examiner's prima facie case of obviousness has not been rebutted by any convincing arguments from Appellants, the Examiner's obviousness rejection of independent claim 57 is sustained.

As to claims 68, 71, 72, 75, 78-80, 83, we also sustain the Examiner's obviousness rejection of these claims based on

set forth in claims 68, 75, and 83. Further, with respect to claims 71, 78, and 79, we find that King '241 provides a clear teaching of the determination of which and how many tested die on a wafer meet a threshold quality value with the subsequent processing of this information to determine whether the product wafer and test wafer are to be integrated as a complete package (King '241, column 5, lines 10-30, Figure 1). Similarly, it is our opinion that, as asserted by the Examiner (Answer, page 5), the temperature cycling operation suggested by King '241 (column 3, lines 18-21) addresses the broadly recited temperature control in claims 72 and 80.

Further, with respect to the Examiner's 35 U.S.C. § 103(a) rejection based on King '241 or King '405 in view of Moriya, we note that, while we found Appellants' arguments to be unpersuasive as to the rejected claims discussed supra, we reach the opposite conclusion with respect to claims 58, 66, 67, 69, 70, 73, 74, 76, 77, 81, and 82. In our view, the temperature cycling operation disclosed by King '241 does not teach or

81, and 82 and the current flow and voltage level limiting circuitry set forth in claims 69 and 70. Accordingly, since all of the claim limitations are not taught or suggested by the applied prior art references, the Examiner's 35 U.S.C. § 103(a) rejection of claims 58, 66, 67, 69, 70, 73, 74, 76, 77, 81, and 82 based on the combination of King '241 or King '405 in view of Moriya is not sustained.

Lastly, we turn to a consideration of the Examiner's separate obviousness rejection of all of the appealed claims based on King '405 or King '241 in view of Kreiger, Yamada, or Charlton, further in view of Kwon or Tuckerman, and further in view of Moriya. Initially, the Examiner proposes to modify the circuitry of King '241 or King '405 by adding the temperature sensing and control teachings of, in the alternative, Kreiger, Charlton, or Yamada. To this combination, the Examiner further adds the teachings of Kwon or Tuckerman, directing particular attention to the disclosure of voltage and current control as related to chip testing. Lastly, the Examiner adds Moriya to the resulting

grouped all of the claims together in making this rejection, the above-mentioned claims contain no temperature control or voltage and current limiting recitations, features for which several of the secondary references were applied. We sustain the rejection of claims 57, 68, 71, 75, 78, 79, and 83, based solely on the combination of King '241 or King '405 in view of Moriya, for all of the reasons discussed supra.[2]

Turning to a consideration of claims 58, 72, 76, 77, and 80 which include limitations directed to temperature control of the product wafer, we sustain the obviousness rejection of these claims as well. In addressing the claim limitations, the Examiner applied the Kreiger, Charlton, and Yamada references, in the alternative, as providing a disclosure of such temperature control features. In the Examiner's line of reasoning (final Office action, Paper No. 12), the quest for increased accuracy in testing would lead the skilled artisan to employ temperature testing as part of the wafer testing procedure.

Our review of the applied prior art references in light of

Examiner's line of reasoning is sufficient to establish a prima facie case of obviousness, thereby shifting the burden to Appellants to provide evidence and/or arguments to rebut the Examiner's position. In evaluating Appellants' response, we note that, in our view, the temperature control teachings of the test circuitry of the Charlton and Yamada references are cumulative to the disclosure of Kreiger, and, accordingly, we will limit our discussion to the Krieger reference. Contrary to Appellants' contention (Brief, pages 22-24) that Kreiger discloses no temperature feedback control loop, we agree with the Examiner (Answer, page 6) that feedback signals from the sensors 78 on the heating element 16 in Kreiger provide feedback control to heater elements 74 to control the temperature testing of the product wafer 12. Further, we find Appellants' argument that Krieger has no temperature testing circuitry resident on a test wafer to be without merit since no such requirement appears in the appealed claims.

We also sustain the Examiner's 35 U.S.C. § 103(a) rejection

of Tuckerman, in particular, the description at column 4, lines 35-46, reveals a disclosure of monitoring and limiting circuitry as claimed. In our view, contrary to Appellants' arguments (Brief, pages 27-28) the disclosed short prevention isolation resistors 206-214 on the test substrate will serve to limit current and voltage to the product wafer as broadly recited in Appellants' claims.

As to claims 66, 67, 73, 74, 81, and 82 directed to communication of clock and reset signals to the product wafer, we find the presently discussed obviousness rejection of the Examiner to be similarly deficient to that discussed previously. As with our earlier discussion, we find no disclosure in any of the additional applied secondary references, and the Examiner has pointed to none, of the clock and reset signals recited in claims 66, 67, 73, 74, 81, and 82 and the current flow and voltage level limiting circuitry set forth in claims 69 and 70. Accordingly, since all of the claim limitations are not taught or suggested by the applied prior art references, the Examiner's separate

35 U.S.C. § 102(e) rejection of claims 57, 58, and 66-83. With regard to the 35 U.S.C. § 103(a) rejection of claims 57, 58, and 66-83 as being unpatentable over King '405 or King '241, in the alternative, in view of Moriya, we have sustained the rejection of claims 57, 68, 71, 72, 75, 78-80, and 83, but have not sustained the rejection of claims 58, 66, 67, 69, 70, 73, 74, 76, 77, 81, and 82. With respect to the separate 35 U.S.C. § 103(a) rejection of claims 57, 58, and 66-83 as being unpatentable over King '405 or King '241 in view of Kreiger, Yamada, or Charlton, further in view of Kwon or Tuckerman, and further in view of Moriya, we have sustained the rejection of claims 57, 58, 68-72, 75-80, and 83, but have not sustained the rejection of claims 66, 67, 73, 74, 81, and 82. Accordingly, the Examiner's decision rejecting claims 57, 58, and 66-83 is affirmed-in-part.[3]

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED-IN-PART

KENNETH W. HAIRSTON Administrative Patent Judge	)	
LEE E. BARRETT Administrative Patent Judge	)	BOARD OF PATENT APPEALS AND INTERFERENCES
JOSEPH F. RUGGIERO Administrative Patent Judge	)	

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Appeal No. 1998-0908
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