

The opinion in support of the decision being entered today was **not** written for publication and is **not** binding precedent of the Board.

Paper No. 29

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte ROBERT H. EKLUND, ROBERT H. HAVEMANN,
and LEO STROTH

Appeal No. 1998-0077
Application No. 08/247,910

ON BRIEF

Before JERRY SMITH, BARRETT, and FLEMING, **Administrative Patent**_Judges.

FLEMING, **Administrative Patent Judge**.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 21-27, 29-40, 43 and 44, all of the claims pending in the present application. Claims 1-20, 28, 41 and 42 have been

anceled.

The invention relates to a method of forming an integrated circuit device including at least one polysilicon resistor. A polysilicon layer is formed, possibly over a field oxide, and then doped to a selected sheet resistance (Specification, page 5, lines 5 through 9; Figure 2). An insulating layer is formed over the polysilicon layer, and patterned and etched to define a resistor body in the underlying polysilicon layer (Specification, page 6, lines 3 through 5; Figure 3). Subsequently, the polysilicon layer is patterned and etched to define first and second heads abutting the resistor body, while simultaneously at least one polysilicon element of a second electronic device (such as a field effect transistor) is formed (Specification, page 6, lines 6 through 8; Figure 4a). First and second resistor contact portions are doped a second time (Specification, page 6, line 19; Figure 4a); sidewall spacers are formed along sidewalls of the insulating layer and the resistor contacts (Specification, page 7, lines 9 and 10; Figures 5a-5c); and finally, silicide regions are formed on the resistor contacts

(Specification, page 7, line 20).

Independent claim 21 is reproduced as follows:

21. A method for fabricating a polysilicon resistor which includes a resistor body portion and at least two contact portions, said method comprising the steps of:

forming a polysilicon layer;

doping said polysilicon layer to obtain a first resistivity;

forming an insulating layer over said polysilicon layer;

removing a portion of said insulating layer such that said resistor body portion of said polysilicon layer remains beneath said insulating layer but said contact portions are exposed;

subsequent to said step of removing a portion of said insulating layer, etching said polysilicon layer to form a resistor which includes said resistor body and said at least two contact portions abutting said resistor body;

performing a second doping step wherein said two contact portions are doped without substantially affecting the doping concentration of said resistor body;

subsequent to said step of forming an insulating layer, forming a sidewall spacer along sidewalls of said resistor body and said at least two contact portions, said sidewall spacer also being formed along a sidewall of said insulating layer formed on said contact portions;

subsequent to said second doping step, forming a silicide region on said contact portions.

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The Examiner relies on the following references:

Brower 1980	4,212,684	Jul. 15,
Winnerl et al. (Winnerl) 7, 1991	5,013,678	May
Hanagasaki 1994	5,304,502	Apr. 19,

Ning, T. H., "Polysilicon Resistor Process For Bipolar and MOS Applications", IBM Technical Disclosure Bulletin, Vol. 23, No. 1, June 1980, pp. 368-70.

Claims 21-27, 29, 30, 32-40, 43 and 44 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Ning, Hanagasaki, Brower, and Winnerl et al. The rejection of claim 31 was withdrawn in the answer.

Rather than reiterate the arguments of Appellants and the Examiner, reference is made to the brief and answer for the respective details thereof.

OPINION

We will not sustain the rejection of claims 21-27, 29, 30, 32-40, 43 and 44 under 35 U.S.C. § 103(a).

The Examiner has failed to set forth a ***prima facie*** case.

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It is the burden of the Examiner to establish why one having ordinary skill in the art would have been led to the claimed invention by the express teachings or suggestions found in the prior art, or by implications contained in such teachings or suggestions. ***In re Sernaker***, 702 F.2d 989, 995, 217 USPQ 1, 6 (Fed. Cir. 1983). "Additionally, when determining obviousness, the claimed invention should be considered as a whole; there is no legally recognizable 'heart' of the invention." ***Para-Ordnance Mfg. v. SGS Importers Int'l, Inc.***, 73 F.3d 1085, 1087, 37 USPQ2d 1237, 1239 (Fed. Cir. 1995), ***cert. denied***, 117 S.Ct. 80 (1996) ***citing W. L. Gore & Assocs., Inc. v. Garlock, Inc.***, 721 F.2d 1540, 1548, 220 USPQ 303, 309 (Fed. Cir. 1983), ***cert. denied***, 469 U.S. 851 (1984).

On pages 5 through 9 of the brief, Appellants argue that Ning, Hanagasaki, Winnerl et al., and Brower fail to teach Appellants' claimed limitations. In particular, Appellants argue that Ning, Hanagasaki, Winnerl et al., and Brower fail to teach removing a portion of the insulating layer so as to expose the contact portions of the polysilicon layer, then

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subsequently etching the polysilicon layer to form a resistor that includes the resistor body and at least two contact portions abutting the resistor body, as claimed in Appellants' claim 21. Appellants further argue that Ning, Hanagasaki, Winnerl et al., and Brower fail to teach, subsequent to the step of removing a portion of the first insulating layer, patterning and etching the polysilicon layer to define first and second contact portions abutting the resistor body and simultaneously forming at least one polysilicon element of a second electronic device, as claimed in Appellants' claim 22. Appellants argue that Ning, Hanagasaki, Winnerl et al., and Brower fail to teach a second doping step of doping the contact portions of the polysilicon resistor prior to patterning and etching the polysilicon layer, as claimed in claims 26 and 34. Finally, Appellants argue that Ning, Hanagasaki, Winnerl et al., and Brower fail to teach the step of doping both n-type and p-type impurities, as claimed in claim 31.

In the answer, the Examiner argues at pages 3 to 5 that the prior art teaches the claimed method and that the combination of Ning, Hanagasaki, Winnerl et al., and Brower is

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proper. In particular, the Examiner alleges on pages 3-4 that Ning teaches simultaneous patterning of the insulating and polycrystalline layers to obtain the polycrystalline layer in the desired final configuration, followed by patterning of the overlaying insulating layer. The Examiner asserts that "it would have been within the scope of one of ordinary skill in the art to pattern [the insulating layer] to obtain the configuration of [the insulating layer] shown in Figure 3c [of Ning] prior to patterning of [the polysilicon layer] because this amounts to essentially a mere reversal of steps."

As pointed out by our reviewing court, we must first determine the scope of the claim. "[T]he name of the game is the claim." *In re Hiniker Co.*, 150 F.3d 1362, 1369, 47 USPQ2d 1523, 1529 (Fed. Cir. 1998).

Turning first to Appellants' claim 21, we note that the claim recites a method for fabricating a polysilicon resistor comprising the steps of: "forming a polysilicon layer; doping said polysilicon layer to obtain a first resistivity; forming an insulating layer over said polysilicon layer; removing a portion of said insulating layer such that said resistor body

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portion of said polysilicon layer remains beneath said insulating layer but said contact portions are exposed; **subsequent to said step of removing a portion of said insulating layer, etching said polysilicon layer to form a resistor which includes said resistor body and said at least two contact portions abutting said resistor body;**" doping the resistor contact portions a second time without affecting the doping concentration of the resistor body; subsequent to the step of forming an insulating layer, forming a sidewall spacer along sidewalls of the resistor body resistor contact portions, and insulating layer; and forming a silicide region on said contact portions. (Emphasis added.)

Thus, Appellants' claim 21 requires etching the polysilicon layer to form a resistor subsequent to the removal of a portion of the insulating layer.

Upon a careful review of Ning, Hanagasaki, Winnerl et al., and Brower, we fail to find that these references teach or suggest the step of etching the polysilicon layer to form a resistor subsequent to the step of removing a portion of the insulating layer. We agree with the Examiner that Ning

teaches patterning the polycrystalline silicon layer followed by patterning of the overlying insulating layer, in contradistinction to the claimed invention. We agree with the Examiner that Hanagasaki teaches the formation of silicide resistor contacts; that Winnerl et al. suggests the formation of sidewall spacers prior to silicide contact formation; and that Ning, Hanagasaki, and Brower together teach doping the resistor contacts. We fail to find, however, that any reference teaches etching the polysilicon layer to form a resistor after removing a portion of the insulating layer such that the resistor body remains beneath the insulating layer but the contact portions are exposed.

Ning teaches at pages 369 and 370 forming layers of polysilicon and insulator, the polysilicon being doped n type by ion implantation (Fig. 3A). Ning then teaches (in Fig. 3B) patterning the polysilicon layer. It is noted that Fig. 3B shows that the insulating layer has been patterned along the same dimensions as the polysilicon layer, so as to overlie the polysilicon layer. Next, Ning teaches (Fig. 3C) patterning the polysilicon resistor region, the resistor contact region being doped n+ by ion implantation. Ning Fig. 3C illustrates,

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without corresponding textual description, patterning and etching of the insulating layer such that the layer covers only the resistor body, exposing the contacts.

Hanagasaki teaches formation of silicide resistor contacts at column 6, line 32 to column 7, line 3. Hanagasaki, however, does not teach patterning and etching an insulating layer followed by patterning and etching a polysilicon layer to form a resistor having such contacts.

Winnerl et al. suggests the formation of sidewall spacers prior to silicide contact formation, at column 3, line 65, to column 4, line 5. Winnerl et al. teaches removing a portion of an insulating layer (see Fig. 2 and column 2, line 67 to column 3, line 5), but such removal does not expose the resistor contact portions. Winnerl et al. subsequently patterns and etches an underlying polysilicon layer (layer 14, Fig. 3, column 3, lines 3-25); but the Winnerl et al. reference lacks a teaching of subsequent doping of the resistor contact portions.

Thus, we fail to find that the combination proposed by the Examiner would have resulted in the claimed invention. Further, Appellants' independent claim 22 contains limitations

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parallel to those contained in claim 21, *i.e.*, etching a portion of the insulating layer to define a resistor body and contact portions in a polysilicon layer, followed by patterning and etching the polysilicon layer to define first and second contact portions. Therefore, we find that the prior art relied upon by the Examiner fails to teach these limitations, for the same reasons specified with respect to claim 21.

Appellants' dependent claims 26 and 34 each depend from one of claims 21 or 22, and therefore define over the prior art of record for the reasons specified above with respect to claims 21 and 22.

The Federal Circuit states that "[t]he mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." ***In re Fritch***, 972 F.2d 1260, 1266 n.14, 23 USPQ2d 1780, 1783-84 n.14 (Fed. Cir. 1992), ***citing In re Gordon***, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984). "Obviousness may not be established using hindsight or in view of the teachings or

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suggestions of the inventor." **Para-Ordinance**, 73 F.3d at 1087,
37 USPQ2d at 1239,

citing W. L. Gore & Assocs., 721 F.2d at 1553, 220 USPQ at
312-13.

Upon a review of the references relied upon by the Examiner, we fail to find any suggestion or reason to etch the polysilicon layer to form a resistor body and contacts after removing a portion of the insulating layer in order to expose those contacts. To the contrary, we find that the Ning teaching would have led those skilled in the art to etch the polysilicon layer before etching the insulating layer above. None of the other references relied upon by the Examiner suggest the desirability of forming an integrated circuit by performing these steps in the order claimed. The Examiner's bald assertion that a "mere reversal of order of steps" renders the claimed invention obvious cannot stand, absent a suggestion of the desirability of so reversing in the prior art. Therefore, we will not sustain the rejection of claims 21-27, 29, 30, 32-40, 43 and 44 under

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35 U.S.C. § 103(a) as being unpatentable over Ning,
Hanagasaki, Winnerl et al., and Brower.

Accordingly, the Examiner's decision is reversed.

REVERSED

JERRY SMITH)	
Administrative Patent Judge)	
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)	
)	BOARD OF PATENT
LEE E. BARRETT))
Administrative Patent Judge)	APPEALS AND
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)	INTERFERENCES
)	
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