

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 20

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte KHORVASH SEFIDVASH

Appeal No. 1997-4221
Application No. 08/255,518

ON BRIEF

Before KRASS, BARRETT, and BARRY, Administrative Patent Judges.

KRASS, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 1 through 3 and 7, all of the claims remaining in the application.

The invention pertains to reliability testing of data being transferred in a computer system. More particularly, the invention concerns an on-the-fly integrity checking system that duplicates data passing through a main system bus and functions concurrently to recognize the size of data blocks being transferred from a sending module to a receiving module. Each word of data transferred is immediately parity checked to indicate the validity or invalidity of the data transfer. No delay is involved in the data transfer operations of the main system bus because the integrity checking system operates on-the-fly independently as an independent module, which does not delay data transfers on the main system bus.

Independent claim 1 is reproduced as follows:

1. A digital system for establishing the integrity of data transfers between a first transmitting module connected by a bus means to a second receiving module, said system comprising:

(a) bus means connecting said first and second modules and enabling the parallel transmission of words of data;

(b) means to determine the size of each block of data being transferred on said bus means;

(c) wherein each said block of data being transferred includes:

(c1) a header portion indicating the size of the data block;

(c2) an original Error Detection Code (OEDC) signature which sets a digital value to the data words in said data block to be transferred;

(d) means to integrity check, concurrently on-the-fly, each said word and each said data block transferred from said first module to said second module without any delay to the data transfer operation, including:

(d1) means to generate an error code value for each data word transferred including:

(d1a) means to accumulate said error code values to form an internally generated resultant Error Detection Code Signature (REDC) after transfer of all the words in said block of data;

(d2) counter means for holding the number of words in the data block being transferred and including:

(d2a) means to reduce the amount in said counter means for each word transferred until reaching a zero count limit for the block size;

(d2b) means to initiate a comparison of said internally generated resultant REDC with said original OEDC after said zero count to see if a match occurs;

(d3) means to transmit an error signal if a match does not occur;

(d4) input register means to momentarily copy, during word transfers, each word being transferred;

(d5) means to determine the parity of each said word being transferred;

(d6) means to signal an error flag should the determined parity of said word be inconsistent.

The examiner relies on the following references:

DeRoo et al. (DeRoo) 1993	5,182,752	Jan. 26,
Tsang et al. (Tsang) 1993	5,243,604	Sep. 7,

Claims 1 through 3 and 7 stand rejected under 35 U.S.C.
103 as unpatentable over Deroo in view of Tsang.

Reference is made to the brief and answer for the respective positions of appellant and the examiner.

OPINION

We reverse as the examiner has clearly not established a prima facie case of obviousness with regard to the instant claimed subject matter.

The examiner applies Deroo against independent claim 1, citing, at page 4 of the answer, various portions of Deroo

which the examiner considers to correspond to the claimed elements. The examiner recognizes, however, that Deroo fails to disclose or suggest the integrity check "concurrently on-the-fly," as claimed. The examiner then turns to Tsang for a teaching of "on-the-fly" error correction and concludes that it would have been obvious to combine Tsang with Deroo "because this allows the next codeword to be sent before the preceding word is actually corrected" [answer-page 5].

Even, assuming, arguendo, that Deroo discloses all that the examiner says it does¹, the examiner's combination of Deroo with Tsang appears to be based on hindsight rather than on anything suggested by either reference. We find no reason, either within the references themselves or within the artisan's knowledge, for an artisan to have been led to modify Deroo in any way by the teachings of Tsang. It is not even clear to us how such a combination would be made even if, somehow, there was a suggestion to make it. The examiner contends, in the

¹We are skeptical about whether Deroo, in fact, discloses all the features contended by the examiner as corresponding to the claimed subject matter.

face of appellant's objection to the combination, that "combining hardware with hardware is not of importance with respect to the rejection" [answer-page 8]. We disagree. Without some suggestion as to how the structures of Deroo and Tsang would be combined, there would have been no reason for the artisan to have done so. It appears to us that appellant is correct when he contends that the examiner is attempting to combine abstract "concepts" rather than practical implementations. From a practical implementation view, there would have been no reason for the artisan to modify Deroo with Tsang and no clear direction as to how such a modification would be made if there were some direction to do so.

Although Tsang does disclose an "on-the-fly" system, there is no indication that it is even the same type of "on-the-fly" system envisioned, and claimed, by appellant. Neither Tsang nor Deroo discloses or suggests data transfers between a first, SCSI Protocol Controller module and a second buffer memory module, as claimed. Moreover, Tsang's on-the-fly error correction system does not appear to integrity check each word and data block transferred from a first to a second module

"without any delay to the data transfer operation," as claimed. Since the encoder/decoder of Tsang is not connected to the bus, in parallel with the modules, as disclosed and suggestively claimed by appellant, it would appear that there would be an inherent delay in any data transfer in Tsang, unlike the instant claimed system. We do not find that the artisan would have found any advantage in attempting to modify the Deroo system with that of Tsang even if such a combination was, somehow, suggested by the prior art which, in our view, the examiner has not shown.

In our view, the examiner has chosen, without any suggestion in the prior art for doing so, bits and pieces of the instant claimed invention from the prior art (the data transfer of Deroo and the "on-the-fly" teaching of Tsang) and thrown these pieces together in a haphazard attempt to meet the instant claim language. 35 U.S.C. 103 requires some reasonable suggestion for combining the teachings of the prior art. We find no such suggestion in the evidence provided by the examiner.

Accordingly, the examiner's decision rejecting claims 1 through 3 and 7 under 35 U.S.C. 103 is reversed.

REVERSED

ERROL A. KRASS)	
Administrative Patent Judge)	
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)	BOARD OF PATENT
LEE E. BARRETT)	APPEALS
Administrative Patent Judge)	AND
)	INTERFERENCES
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