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The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 19

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte SHAHID S. ANSARI

Appeal No. 1997-4069
Application No. 08/282,913

ON BRIEF

Before THOMAS, BARRETT, and BARRY, Administrative Patent Judges.
BARRY, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on the appeal under 35 U.S.C. § 134 from the final rejection of claims 1-21. The appellant filed amendments after final rejection on June 13, 1996, and on July 5, 1996. Although the former was denied entry, the latter was entered. We reverse.

BACKGROUND

When debugging a computer system, a tester must first identify a component that has failed. He can then test the component to pinpoint the cause of the fault. When the faulty component is an integrated circuit (IC), the IC is commonly removed from the system and independently tested on automatic test equipment. Recreating a fault can be difficult, however, when the IC is tested independently. Furthermore, writing software to drive the IC during testing can be slow and laborious.

The invention at issue in this appeal tests an IC die while it is operatively connected to and driven by the actual computer system in which it is used. Such testing can detect faults and errors caused by computer-system level problems such as parasitic capacitance and slight differences in expected voltages.

Claim 1, which is representative for our purposes, follows:

1. A method of testing an integrated circuit in a system level environment using an actual electrical system in which answer the integrated circuit is intended to be used to operate the integrated circuit during the testing, the integrated circuit being part of a module which makes up part of the electrical system and the integrated circuit to be tested being operatively connected to the electrical system when the testing occurs, the method comprising the steps of:

exposing a die in a packaged integrated circuit to be tested;

placing the module that incorporates the exposed die on a test platform and positioning a sensor probe relative to the exposed die such that the sensor probe can directly monitor the die during testing;

operating the electrical system in a manner which exercises the exposed die; and

using the sensor probe to directly monitor the die while the exposed die is being exercised by the operation of the electrical system in which the integrated circuit is intended to be used.

The references relied on in rejecting the claims follow:

Choi et al. (Choi) 1989	4,862,075	Aug. 29,
Baerg et al. (Baerg) 1990	4,980,019	Dec. 25,
Huppenthal 1992	5,162,728	Nov. 10,
Hurley et al. (Hurley) 1995. 1993)	5,475,316	Dec. 12, (Filed Dec. 27,

Claims 1-8 and 14 stand rejected under 35 U.S.C. § 103 as obvious over Choi in view of Baerg. Claims 9-13 stand rejected under 35 U.S.C. § 103 as obvious over Choi in view of Baerg further in view of Huppenthal. Claims 15-17 stand rejected under 35 U.S.C. § 103 as obvious over Choi in view of Baerg further in view of Huppenthal even further in view of Hurley. Claims 18-21 stand rejected under 35 U.S.C. § 103 as obvious over Choi in view of Hurley. Rather than repeat the arguments of the appellant or examiner in toto, we refer the reader to the briefs and answer for the respective details thereof.

OPINION

In reaching our decision in this appeal, we considered the subject matter on appeal and the rejections advanced by the examiner. Furthermore, we duly considered the arguments and evidence of the appellant and examiner. After considering the totality of the record, we are persuaded that the examiner erred in rejecting claims 1-21. Accordingly, we reverse.

We begin by noting the following principles from In re Rijckaert, 9 F.3d 1531, 1532, 28 USPQ2d 1955, 1956 (Fed. Cir. 1993).

In rejecting claims under 35 U.S.C. Section 103, the examiner bears the initial burden of presenting a prima facie case of obviousness. In re Oetiker, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992). Only if that burden is met, does the burden of coming forward with evidence or argument shift to the applicant. Id. "A prima facie case of obviousness is established when the teachings from the prior art itself would appear to have suggested the claimed subject matter to a person of ordinary skill in the art." In re Bell, 991 F.2d 781, 782, 26 USPQ2d 1529, 1531 (Fed. Cir. 1993) (quoting In re Rinehart, 531 F.2d 1048, 1051, 189 USPQ 143, 147 (CCPA 1976)). If the examiner fails to establish a prima facie case, the rejection is improper and will be overturned. In re Fine, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988).

With these principles in mind, we address the obviousness of the following groups of claims:

- claims 1-17
- claims 18-21.

We first address the obviousness of claims 1-17.

Claims 1-17

The appellant argues, "no reasonable combination of the Choi and Baerg patents discloses or reasonably suggests the

testing of an exposed die while the die is being driven or exercised by the **actual system in which the integrated circuit is to be used.**" (Appeal Br. at 7.) The examiner's reply follows.

A person of ordinary skill in the art would [have] be[en] motivated to utilize the teachings of Baerg for testing a die into the test system of Choi to be able to conduct elaborate tests, since Choi already teaches (col. 2, lines 26-68) his test system's adoptability [sic] to various devices including integrated circuits and semiconductor wafers and Baerg provides further motivation for such an inclusion by teaching that for performing elaborate tests, the integrated circuit needs to be evaluated internally requiring exposing the die. (Examiner's Answer at 9.)

At the outset, we note that the examiner's rejections focus on the content of the references. He fails to map the exact and complete language of the claims to the teachings of the references. "[T]he main purpose of the examination, to which every application is subjected, is to try to make sure that what each claim defines is patentable. [T]he name of the game is the claim" In re Hiniker Co., 150 F.3d 1362, 1369, 47 USPQ2d 1523, 1529 (Fed. Cir. 1998) (quoting Giles S. Rich, The Extent of the Protection and Interpretation of

Claims --American Perspectives, 21 Int'l Rev. Indus. Prop. &
Copyright L. 497, 499, 501 (1990)).

Here, claims 1-13 each specify in pertinent part the
following limitations:

testing an integrated circuit in a system level
environment using an actual electrical system in
answer the integrated circuit is intended to be used
to operate the integrated circuit during the
testing, ... the integrated circuit to be tested
being operatively connected to the electrical system
when the testing occurs, the method comprising the
steps of:

...

operating the electrical system in a manner
which exercises the exposed die; and

using the sensor probe to directly monitor the
die while the exposed die is being exercised by the
operation of the electrical system in which the
integrated circuit is intended to be used.

Similarly, claims 14-17 each specify in pertinent part the
following limitations:

a test platform arranged to support a board
level module that carries a multiplicity of
electrically connected components that make up at
least a part of an overall electrical system in
which the integrated circuit is intended to be used,
the platform supporting the board level module such
that the board level module remains operatively
connected to the electrical system during the
testing procedure;

... a designated exposed integrated circuit die that is mounted on and electrically connected within said module and which forms a component in the electrical system; and

a driver suitable for directing the operation of the electrical system in which the integrated circuit die is intended to be used in a manner that exercises the designated die to facilitate testing of the designated die during the operation of the electrical system.

In summary, the claims each recite testing an IC die while the die is connected to and exercised by the actual electrical system in which it is to be used.

The examiner fails to show a teaching or suggestion of the claimed limitations. "Obviousness may not be established using hindsight or in view of the teachings or suggestions of the inventor." Para-Ordnance Mfg. v. SGS Importers Int'l, 73 F.3d 1085, 1087, 37 USPQ2d 1237, 1239 (Fed. Cir. 1995) (citing W.L. Gore & Assocs., Inc. v. Garlock, Inc., 721 F.2d 1540, 1551, 1553, 220 USPQ 303, 311, 312-13 (Fed. Cir. 1983)). "The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." In re Fritch, 972 F.2d 1260, 1266, 23 USPQ2d

1780, 1784 (Fed. Cir. 1992) (citing In re Gordon, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984)). "It is impermissible to use the claimed invention as an instruction manual or 'template' to piece together the teachings of the prior art so that the claimed invention is rendered obvious." Fritch, 972 F.2d 1266, 23 USPQ2d at 1784, (citing In re Gorman, 933 F.2d 982, 987, 18 USPQ2d 1885, 1888 (Fed. Cir. 1991)).

Here, Choi teaches "a high speed test system ... that measures electrical properties of various devices." Col. 2, ll. 49-50. The examiner fails to allege, let alone show, however, that a device being measured by the test system remains connected to and exercised by the actual system in which it is to be used. Rather than remaining connected to the actual system, the reference's device under test (DUT) is received by a socket 15 in an adapter board 13. Col. 4, ll. 3-4. Instead of being exercised by the actual system, moreover, "[a] multiplicity of electronic boards are provided [in Choi] to drive the device under test." Id. at ll. 5-6.

The examiner also fails to allege, let alone show, that Baerg, Huppenthal, or Hurley remedies the defects of Choi. He relies on Baerg merely to suggest that "elaborate tests ... would require exposing the die" (Examiner's Answer at 4.) The examiner relies on Huppenthal only to teach "a wafer prober that moves the wafers into proper position and probes are positioned [sic] to physically and electrically contact the DUT." (Id. at 5.) He relies on Hurley merely to show "an emission microscope to detect and localize in-process and use-related defects in integrated circuits." (Id. at 7.)

For the foregoing reasons, we are not persuaded that teachings from the prior art would appear to have suggested the claimed limitations of testing an IC die while the die is connected to and exercised by the actual electrical system in which it is to be used. The examiner impermissibly relies on the appellant's teachings or suggestions; he has not established a prima facie case of obviousness. Therefore, we reverse the rejections of claims 1-17 under 35 U.S.C. § 103. Next, and last, we address the obviousness of claims 18-21.

Claims 18-21

The appellant makes the following argument.

[N]o reasonable combination of the Choi and Hurley patents disclose or reasonably suggest a module including a printed circuit board having a prober testing opening with an integrated circuit mounted over the prober testing opening such that a sensor probe can access the die through the prober testing opening when the die is exposed and while the die is still electrically connected to the module. (Appeal Br. at 13.)

The examiner's reply follows.

Hurley teaches (col. 5, lines 44-58) a modification such that the actual stage is a hole cut into the vibration isolation table which allows the DUT in its socket to extend into the light tight enclosure. Examiner contends that for [sic] a person having ordinary skill in the art would [have] be[en] motivated [sic] to modify Choi test system to be able to incorporate the emission microscope and the modification stated above. This is because both systems are from the same environment and Hurley's emission microscope provides capabilities for detecting in-process and use-related defects in integrated circuits and provides available interface to ATE tester of the type disclosed by Choi which is motivation ... for the modification stated above. (Examiner's Answer at 12.)

Claims 18-21 each specify in pertinent part the following limitations:

a printed circuit board ... having a prober testing opening formed therein; and

a multiplicity of components mounted on the printed circuit board, ... including an integrated circuit on a silicon die that is mounted over the prober testing opening such that a sensor probe can access the die through said prober testing opening
....

In summary, the claims each recite an IC die mounted over an opening in a printed circuit board (PCB) so that a sensor probe can access the die through the opening.

The examiner fails to show a teaching or suggestion of the claimed limitations. He admits, "Not explicitly disclosed by Choi is an integrated circuit on a silicon die that is mounted over [a] prober [sic] testing opening such that a sensor probe can access the die through testing opening"
(Examiner's Answer at 8.)

Hurley, in turn, teaches "an improved transportable emission microscope for testing semiconductor circuits." Col. 1, ll. 7-8. "A departure from prior art is the direct access of the emission microscope objectives to the die face of the DUT." Col. 7, ll. 38-39. The microscope omits a fixed stage. "Where a stage (the focal plane of the objectives) would

exist, a twelve inch hole is cut through the vibration isolation tabletop." Id. at ll. 1-4. "This allows the DUT 43 in its socket to extend into the light tight enclosure." Col. 5, ll. 46-47.

The examiner fails to show that the hole through the vibration isolation tabletop would have suggested mounting an IC die over an opening in a PCB so that a sensor probe can access the die through the opening. Rather than being mounted on a PCB, the reference's DUT is placed in "[a] test socket or 'daughter board' ... mounted on [a] test head 39" Col. 5, ll. 23-25. The hole on which the examiner relies is not in the test socket/daughter board or in anything on which the DUT is mounted. Instead, the hole is "cut into the vibration isolation table." Id. at ll. 45-46. Rather than permitting a sensor probe to access an IC die, moreover, the examiner admits that the hole "allows the DUT in its socket to extend into the light tight enclosure." (Examiner's Answer at 12.)

For the foregoing reasons, we are not persuaded that teachings from the prior art would appear to have suggested

the claimed limitations of an IC die mounted over an opening in a PCB so that a sensor probe can access the die through the opening. The examiner impermissibly relies on the appellant's teachings or suggestions; he has not established a prima facie case of obviousness. Therefore, we reverse the rejections of claims 18-21 under 35 U.S.C. § 103.

CONCLUSION

To summarize, the rejection of claims 1-21 under 35 U.S.C. § 103 is reversed.

REVERSED

JAMES D. THOMAS)	
Administrative Patent Judge)	
)	
)	
)	
)	BOARD OF PATENT
LEE E. BARRETT)	APPEALS
Administrative Patent Judge)	AND
)	INTERFERENCES
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LANCE LEONARD BARRY)
Administrative Patent Judge)

LLB/sld

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Steve D. Beyer
Hickman & Beyer
P.O. Box 61059
Palo Alto, CA 94306

APPEAL NO. [Appeal No.] - JUDGE BARRY

APPLICATION NO. [Application No.]

APJ BARRY

APJ [APJ # 2]

APJ [APJ # 3]

DECISION: [Outcome]ED

Prepared by: Gloria Henderson

DRAFT TYPED: 23 Jan 01

FINAL TYPED:

Team 3, please note the following instructions:

Do NOT change style of citations.

Do insert full names of all inventors

Do insert reference(s).

Do add a mailing address

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