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The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 20

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte JAMES F. GOEDKEN and RICHARD L. HAMMON

Appeal No. 1997-3839
Application No. 08/120,144

ON Brief

Before THOMAS, BARRETT, and DIXON, **Administrative Patent Judges**.
DIXON, **Administrative Patent Judge**.

DECISION ON APPEAL

This is a decision on appeal from the examiner's final rejection of claims 1-13, which are all of the claims pending in this application.

We REVERSE.

BACKGROUND

The appellants' invention relates to reset recovery in a microprocessor controlled device. An understanding of the invention can be derived from a reading of exemplary claim 1, which is reproduced below.

1. A method for recovering control of a microprocessor controlled device affected by a reset condition, the device having volatile memory containing predetermined data and state information, the method comprising the steps of:

evaluating the volatile memory for the predetermined data;

initializing all locations of the volatile memory when the predetermined data is not present; and

initializing only predetermined locations of the volatile memory when the predetermined data is present.

The prior art references of record relied upon by the examiner in rejecting the appealed claims are:

Nagasawa	4,658,352	Apr. 14, 1987
Hamilton et al. (Hamilton)	4,819,237	Apr. 04, 1989

Claims 1, 3 and 4 stand rejected under 35 U.S.C. § 102 as being unpatentable over Hamilton. Claims 2 and 13 stand rejected under 35 U.S.C. § 103 as being unpatentable over Hamilton. Claims 5-12 stand rejected under 35 U.S.C. § 102 as being unpatentable over Nagasawa.

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Rather than reiterate the conflicting viewpoints advanced by the examiner and the appellants regarding the above-noted rejections, we make reference to the Examiner's Answer (Paper No. 19, mailed Aug. 5, 1997) for the examiner's reasoning in support of the rejections, and to the appellants' Brief (Paper No. 18, filed Oct. 31, 1996) for the appellants' arguments thereagainst.

OPINION

In reaching our decision in this appeal, we have given careful consideration to the appellants' specification and claims, to the applied prior art references, and to the respective positions articulated by the appellants and the examiner. As a consequence of our review, we make the determinations which follow.

CLAIMS 1, 3 AND 4

Appellants argue that “[a]fter evaluating the volatile memory for the predetermined data, the device initializes 'all locations of the volatile memory when the predetermined data is not present', and initializes 'only predetermined locations of the volatile memory when the predetermined data is present.’” (See Brief at page 3.)

Further, appellants argue that “there is no teaching or suggestion that only a portion of the volatile memory is initialized [in Hamilton].” (See Brief at page 4.) We agree with appellants.

Furthermore, the examiner has not provided clear correspondence in the specification to support the position maintained by the examiner that Hamilton clearly anticipates the language in claim 1. From our review of Hamilton and by closely reviewing the portions of Hamilton cited by the examiner (see Answer at page 4), we find that Hamilton teaches a verification of integrity of the volatile memory after a reset mode/condition is indicated, and if the data is corrupted, the memory is initialized. If the data is not corrupted, the memory is not initialized. (See Summary of the Invention at col. 2.) We do not find any clear support for the examiner's statement that "Hamilton et al. teach the feature of initializing only a portion of a volatile memory." (See Answer at page 3.) The examiner relies upon a reset condition initializing the memory and if the validity of the memory is valid then the memory is initialized "as-is" to meet the language of claim 1. (See Answer at page 4.) We disagree with the examiner. The examiner's interpretation of the "initializing" limitation is inconsistent. Inaction with respect to the memory is not the same function as initializing portions of the memory as recited in the language of claim 1. Therefore, we will not sustain the rejection of independent claim 1 and its dependent claims 2-4.

CLAIMS 5-12

Before addressing the examiner's rejections based upon prior art, it is an essential prerequisite that the claimed subject matter be fully understood. Analysis of

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whether a claim is patentable over the prior art under 35 U.S.C. §§ 102 and 103 begins with a determination of the scope of the claim. The properly interpreted claim must then be compared with the prior art. Claim interpretation must begin with the language of the claim itself. **See Smithkline Diagnostics, Inc. v. Helena Laboratories Corp.**, 859 F.2d 878, 882, 8 USPQ2d 1468, 1472 (Fed. Cir. 1988). Accordingly, we will initially direct our attention to appellants' claim 5 to derive an understanding of the scope and content thereof.

Before turning to the proper construction of the claims, it is important to review some basic principles of claim construction. First, and most important, the language of the claim defines the scope of the protected invention. **Yale Lock Mfg. Co. v. Greenleaf**, 117 U.S. 554, 559 (1886) ("The scope of letters patent must be limited to the invention covered by the claim, and while the claim may be illustrated it cannot be enlarged by language used in other parts of the specification."); **Autogiro Co. of Am. v. United States**, 384 F.2d 391, 396, 155 USPQ 697, 701 (Ct. Cl. 1967) ("Courts can neither broaden nor narrow the claims to give the patentee something different than what he has set forth [in the claim]."). **See also Continental Paper Bag Co. v. Eastern Paper Bag Co.**, 210 U.S. 405, 419 (1908); **Cimiotti Unhairing Co. v. American Fur Ref. Co.**, 198 U.S. 399, 410 (1905). Accordingly, "resort must be had in the first instance to the words of the claim" and words "will be given their ordinary and

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accustomed meaning, unless it appears that the inventor used them differently."

Envirotech Corp. v. Al George, Inc., 730 F.2d 753, 759, 221 USPQ 473, 477 (Fed. Cir. 1984). Second, it is equally "fundamental that claims are to be construed in the light of the specification and both are to be read with a view to ascertaining the invention." **United States v. Adams**, 383 U.S. 39, 49, 148 USPQ 479, 482 (1966).

Furthermore, the general claim construction principle that limitations found only in the specification of a patent or patent application should not be imported or read into a claim must be followed. **See In re Priest**, 582 F.2d 33, 37, 199 USPQ 11, 15 (CCPA 1978). One must be careful not to confuse impermissible imputing of limitations from the specification into a claim with the proper reference to the specification to determine the meaning of a particular word or phrase recited in a claim. **See E.I. Du Pont de Nemours & Co. v. Phillips Petroleum Co.**, 849 F.2d 1430, 1433, 7 USPQ2d 1129, 1131 (Fed. Cir. 1988), **cert. denied**, 488 U.S. 986 (1988). What we are dealing with in this case is the construction of the limitations recited in the appealed claims. From our review of the specification and the language of the claims, claim 5 is directed to an invention having a plurality of reset conditions and initializing selected portions of the volatile memory which are determined by the type of reset. Some portions of the memory must be reset in each type of reset.

Again, the examiner has not provided a clear correspondence of the specific portion of Nagasawa which is being relied upon to teach the claimed invention. Therefore, we review Nagasawa with the limited guidance of the examiner. From our review of Nagasawa, we find that Nagasawa teaches the evaluation of the volatile memory and determining the type of reset, but Nagasawa teaches only initializing the memory for a power-on reset. (See Nagasawa at col. 3.) Nagasawa states:

After a reset start by the application of the power current, the CPU 1 monitors the Q output signal level of the FF 11 through the I/O unit 4. If the Q output signal is at the low level as shown in FIG. 2C, the CPU 1 judges that the power-on reset should be done, and performs the initial setting such as a RAM clear operation. If, on the other hand, the output signal level of the Q output signal of FF 11 is high, a normal back-up power voltage is applied and the backup operation of the time of power down is performed, and further the CPU 1 judges that a reset of the release from the power down mode should be effected, and the CPU 1 operates so as not to perform the initial setting of the RAM data. In FIG. 2F, the character a indicates the operation of the level detection of the FF 11, and the character b indicates the operation of the initialization of the RAM. In the case of the initialization of the RAM, the FF 11 is set by means of the output signal from the I/O unit 4 so as to provide for the next cut-off of the system power supply. (Column 3, lines 12-31) (Emphasis added.)

Nagasawa later states that:

The system of the present invention is based on the difference between this irregularity of data in the time of normal power-on resetting and the preservation of the data after the "power down mode", and characterized by storing the check code CD₂ [sic] and/or a particular pattern code PC₃ in the RAM 3. Thus, it becomes possible to determine the type of reset operation by detecting the check code CD₂ or the

particular pattern code PC_3 at the time of the reset start of the CPU 1. If there is no change in the check code CD_2 and/or in the particular pattern code PC_3 , the reset operation is determined as the reset operation after being released from the "power down mode". If, on the other hand, there is a change, the reset operation is determined as the normal power-on reset operation, and the initialization of the data in the RAM 3 is performed [sic]. At the same time, a new check code CD_2 and/or a new particular pattern code PC_3 are generated and then written in the RAM 3. (Column 4, lines 22-39.)

In our view, Nagasawa teaches the recognition of 2 different resets, but with an initialization of memory in only one of the reset operations. Therefore, Nagasawa does not teach "initializing selected portions of the volatile memory, the selected portions being determined by the type of reset" as required by claim 5. Therefore, we will not sustain the rejection of independent claim 5 and its dependent claims 6-12.

CLAIMS 2 and 13

The examiner maintains that it would have been obvious to "initialize memory locations other than state information locations because Hamilton et al. suggests initializing portions of a memory." (See Answer at page 3.) We disagree with the examiner's conclusion. The examiner has not shown support in Hamilton for the initialization of only portions of the memory. Moreover, the examiner has not provided a convincing line of reasoning to initialize locations other than state information in the memory. Therefore, we will not sustain the rejection of claims 2 and 13.

CONCLUSION

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To summarize, the decision of the examiner to reject claims 1 and 3-12 under 35 U.S.C. § 102 is reversed, and the decision of the examiner to reject claims 2 and 13 under 35 U.S.C. § 103 is reversed.

REVERSED

JAMES D. THOMAS)	
Administrative Patent Judge)	
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)	BOARD OF PATENT
LEE E. BARRETT)	APPEALS
Administrative Patent Judge)	AND
)	INTERFERENCES
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JOSEPH L. DIXON)	
Administrative Patent Judge)	

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JONATHAN P. MEYER
MOTOROLA, INC.
INTELLECTUAL PROPERTY DEPARTMENT (JJK)
600 NORTH U.S. HWY 45
LIBERTYVILLE, IL 60048