

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 15

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte DAVID J. FOSTER,
ARMANDO GARCIA,
and ROBERT B. PEARSON

Appeal No. 1997-3426
Application 08/373,052¹

ON BRIEF

Before HAIRSTON, BARRETT, and FRAHM, Administrative Patent Judges.

BARRETT, Administrative Patent Judge.

DECISION ON APPEAL

¹ Application for patent filed January 17, 1995, entitled (as amended in Paper No. 6) "Methods For Performing Diagnostic Functions In A Multiprocessor Data Processing System Having A Serial Diagnostic Bus," which is a division of Application 07/733,767, filed July 22, 1991, now U.S. Patent 5,469,542, issued November 21, 1995.

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This is a decision on appeal under 35 U.S.C. § 134 from the final rejection of claims 12-30.

We reverse.

BACKGROUND

The disclosed invention is directed to a method for communicating a packet of diagnostic-related information between a master and a plurality of nodes. The nodes each include a data processor and other circuitry coupled to the data processor through the data processor signal lines. The other circuitry can assume control of the data processor signal lines to mimic local processor-generated control signals, such as read/write, in accordance with functions specified by the packet.

Claim 12 is reproduced below.

12. In a multiprocessor system having a plurality of nodes each of which includes a data processor and other circuitry coupled to a data processor through data processor signal lines, a method for communicating diagnostic-related information between a master and the plurality of nodes, comprising the steps of:

transmitting a packet of diagnostic-related information in a bit serial format from the master to a first one of the nodes;

receiving the packet with the first node;

determining if the packet is intended for the first node; and if so

storing the packet within the first node;

transmitting the packet from the first node to a next node; and

while the step of transmitting is occurring, and if the packet was determined to be intended for the first node, performing in the first node an operation specified by the packet, wherein at least one received packet causes a portion of the other circuitry to assume control of at least some of the data processor signal lines for executing a function specified by the packet.

The Examiner relies on the following prior art:²

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|------|------------------------------|-------------------------|------------|
| 1980 | Underwood et al. (Underwood) | 4,181,940 | January 1, |
| 1992 | Lampport et al. (Lampport) | 5,138,615 | August 11, |
| | | (filed June 22, 1989) | |
| 1993 | Awiszio et al. (Awiszio) | 5,193,149 | March 9, |
| | | (filed October 8, 1991) | |
| 1994 | Douglas et al. (Douglas) | 5,333,268 | July 26, |

(effective filing date October 3, 1990)

² The Examiner also cites Schroeder et al., U.S. Patent 5,088,091, and Chang et al., U.S. Patent 5,367,643, in the list of Prior Art of Record (Examiner's Answer, pages 2-3). The references are not applied in any of the rejections. The listing of prior art in an Examiner's Answer should be limited to the references relied on in the rejections on appeal. See Manual of Patent Examining Procedure § 1208.

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Claims 12, 18-24, and 28 stand rejected under 35 U.S.C. § 103 as being unpatentable over Lamport, Douglas, and Underwood.

Claims 13-17, 25-27, 29, and 30 stand rejected under 35 U.S.C. § 103 as being unpatentable over Lamport, Douglas, and Underwood as applied to claims 12 and 28, further in view of Awiszio.

We refer to the Final Rejection (Paper No. 7) (pages referred to as "FR__") and the Examiner's Answer (Paper No. 12) (pages referred to as "EA__") for a statement of the Examiner's position, and to the Appeal Brief (Paper No. 11) (pages referred to as "Br__") and the Reply Brief (Paper No. 13) (pages referred to as "RBr__") for Appellants' arguments thereagainst.

OPINION

Appellants argue that the combination of Lamport, Douglas, and Underwood does not teach or suggest at least the limitation "wherein at least one received packet causes a portion of the other circuitry to assume control of at least some of the data processor signal lines for executing a function specified by the packet" of claim 12 (e.g., Br12-16)

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and the similar limitation in claim 28. We consider this limitation dispositive of the obviousness rejections.

The Examiner does not mention this limitation as being taught by Lamport in the statement of the rejection (FR2-3), but also does not expressly find the limitation to be a difference. It appears that the Examiner implicitly admits that Lamport does not teach or suggest this limitation because the Examiner relies on Douglas and Underwood for the teaching of "other circuitry" that assumes control of the data processor signal lines (FR3). Nevertheless, we have reviewed Lamport and find that it does not teach or suggest the limitation. The signal lines of the switch control processor (SCP) 216 in the node circuitry of Figure 8 of Lamport is not controlled by other circuitry in the node.

The Examiner states that Douglas discloses "other circuitry" in Figure 8, item 202, which is caused to assume control of the data processor signal lines (Fig. 8, item 206, col. 199, lines 17-21, and col. 207, lines 26-31) (FR3).

Appellants note that the portion of Douglas specifically referred to by the Examiner at column 199 refers to the diagnostic network node used by the data router in Figure 13A.

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Appellants argue that what is described is the internal workings of one of the diagnostic nodes 100 (Figs. 6A-6C) in cooperation with an unillustrated local diagnostic processor (Br13) and that there is no disclosure that any circuitry assumes control over signal lines of the leaf node processors 200 (Br14).

In response, the Examiner basically repeats the statements in the Final Rejection (EA9-10).

Appellants further argue (RBr6-7): "In that the network interface 202 is coupled to the processor 200 through the memory bus 203, it is not seen where or how the network interface 202 can 'assume control of at least some of the data processor signal lines for executing a function' specified by a received packet."

We agree with Appellants that it is unknown how the network interface 202 in Figure 8 can "assume control of at least some of the data processor signal lines for executing a function specified by the packet" since it is connected to the processor 200 through the memory bus 203. The Examiner does not explain how network interface 202 or diagnostic network interface 206 can assume control of the processor 200. The

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lines referred to by the Examiner at columns 199 and 207 do not even appear to describe the functioning of the interfaces 202 and 206. In view of the length and complexity of the reference, we review only those portions specifically relied on by the Examiner. We find that Douglas does not teach or suggest the limitation that "at least one received packet causes a portion of the other circuitry to assume control of at least some of the data processor signal lines for executing a function specified by the packet" (claim 12) or "assuming control over at least some of the data processor signal lines and reading data from a memory location that is accessible to the data processor" (claim 28). Therefore, we do not need to reach the issue of motivation.

The Examiner states that item 16 in Figure 1 of Underwood includes other circuitry which is caused to assume control of the data processor signal lines (FR3).

Appellants note that Underwood discloses a multiprocessor system wherein one processor performs an automatic fault isolation test (FIT) on another processor. One of the processors is selected to be a master and the processor to be tested is the slave. The master exercises control over the

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slave by means of halt, clear, initiate, and interrupt commands sent via input/output 14 causing the slave to execute test programs (col. 8, lines 41-44). "Underwood et al. are thus not seen to expressly disclose or suggest that the master processor assumes control over the signal lines of the slave processor." (Br14.)

In response, the Examiner basically repeats the statements in the Final Rejection (EA10).

Appellants reply (RBr7):

The transfer switch 16 appears to control access to the memories 24-28 for processors 10 and 12 (col. 3, lines 39-46). It is not seen where the transfer switch 16 assumes control over signal lines of the processors 10 and 12 to perform a diagnostic-related function. Furthermore, a single-stepped processor, although being single-stepped through instructions by another processor, would still have control over its own signal lines while executing each instruction.

We agree with Appellants that Underwood does not disclose the master processor assuming control over the signal lines of the slave processor. The slave executes the programs, not the master. Moreover, the processors 10 and 12 do not even communicate directly, but communicate indirectly by placing instructions or data in either the input/output 14 or one of the memories 24, 26, and 28 (col. 3, lines 13-17). Thus, one

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processor cannot assume control of the signal lines of the other processor. As for the Examiner's reliance on the transfer switch 16 as the "other circuitry," we fail to see how the switch 16 assumes control over signal lines of the processors 10 and 12. The transfer switch 16 merely performs a switching function. The Examiner offers no explanation beyond pointing to element 16. We find that Underwood does not teach or suggest the limitation that "at least one received packet causes a portion of the other circuitry to assume control of at least some of the data processor signal lines for executing a function specified by the packet" (claim 12) or "assuming control over at least some of the data processor signal lines and reading data from a memory location that is accessible to the data processor" (claim 28).

Therefore, we do not need to reach the issue of motivation.

For the reasons stated above, we conclude that the Examiner has failed to establish a prima facie case of obviousness with respect to independent claims 12 and 28. Awiszio does not cure the deficiencies of Lampport, Douglas, and Underwood. The rejections of independent claims 12 and 28 and dependent claims 13-27, 29, and 30 are reversed.

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REVERSED

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| KENNETH W. HAIRSTON |) | |
| Administrative Patent Judge |) | |
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| |) | BOARD OF PATENT |
| LEE E. BARRETT |) | APPEALS |
| Administrative Patent Judge |) | AND |
| |) | INTERFERENCES |
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| ERIC FRAHM |) | |
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