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Paper No. 35

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte AKIRA NISHIMURA, SUNAO OGAWA,
YASUO YAMADA and AKIRA KANUMA

Appeal No. 1997-2983
Application No. 08/482,792

HEARD: September 14, 2000

Before FLEMING, LALL, and BARRY, Administrative Patent Judges.
BARRY, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134 from the rejection of claims 1-4 and 6-14. We affirm-in-part.

BACKGROUND

The invention at issue in this appeal is a single chip microcomputer (MCU) featuring a system bus (SYSBUS), a dedicated data bus (SDBUS), and a bank address bus (BABUS). The SYSBUS is used to transfer normal addresses and data. The

SDBUS is used to transfer context data saved from or restored to a register set (RF), program counter (PC), and processor status word (PSW). When a currently executing program is interrupted by a program to be executed, context data representing the instant execution status of the currently executing program (e.g., the contents of PC and PSW) are transferred from a central processing unit (CPU) to an external memory via the SDBUS and BABUS. Context data for program to be executed are then transferred via the SDBUS and BABUS to replace the previous context data.

Claims 6 and 13, which are representative for our purposes, follow:

6. A single chip microcomputer comprising:

(a) a central processing unit (CPU) for processing programs, said CPU comprising a Processor Status Word Register, a Program Counter Register, and a General Purpose Register Set;

(b) an on-chip RAM;

(c) an on-chip ROM;

(d) a first bus for connecting said CPU, RAM and ROM with one another and passing data between them;

(e) a second bus for passing address data corresponding to the data passed through said first bus;

(f) a third bus for connecting said CPU with said RAM, said third bus being used only for passing data respectively held in said Program Counter Register, said Processor Status Word Register, and said General Purpose Register Set between said CPU and said RAM, a number of bits of said third bus being larger than that of said first bus; and

(g) a fourth bus for connecting said CPU with said RAM and passing address data corresponding to said data passed through said third bus.

13. A microcomputer formed with a single chip, comprising:

a system bus;

a random access memory formed within said single chip and connected to said system bus, at least one register bank being formed in said random access memory;

an I/O device formed within said single chip and connected to said system bus;

a CPU core formed within said single chip and connected to said system bus for performing data processing in cooperation with said random access memory, said CPU core including an interface controller for controlling data exchange through said system bus, a decoder and control circuit for decoding instructions to generate control signals, an arithmetic logic unit for executing instructions, a register file for providing temporary storage, a bank pointer for indicating a location of said register file in said random access memory, and an

internal data bus through which data exchange is performed among said interface controller, said arithmetic logic unit and said register file;

an exclusive-use data bus connected between said register file and said random access memory for data exchange therebetween and provided separately from said system bus; and

a bank address bus connected between said random access memory and a bank pointer and provided separately from said system bus for accessing said random access memory to perform data transfer between said register file and said random access memory through said exclusive-use data bus.

Besides the appellants' admitted prior art (AAPA), the references relied on in rejecting the claims follow:

Levy et al. (Levy)	3,999,163	Dec. 21, 1976
Delagi et al. (Delagi)	4,016,541	Apr. 5, 1977
Tanaka	4,733,346	Mar. 22, 1988
Maejima et al. (Maejima), "A 16-Bit Microprocessor with Multi-Register Bank Architecture," 1986 Proceedings: Fall Joint Computer Conference, 1014-19 (1986).		

Claims 1, 6, 11, 13, and 14 stand rejected under 35 U.S.C.

§ 103(a) as obvious over AAPA in view of Levy and Delagi.

Claims 2, 4, 7-10, and 12 stand rejected under 35 U.S.C. §

103(a) as obvious over AAPA in view of Levy and Delagi further

in view of Tanaka. Claim 3 stands rejected under 35 U.S.C. § 103(a) as obvious over AAPA in view of Levy, Delagi, and Tanaka further in view of Maejima. Rather than repeat the arguments of the appellants or examiner in toto, we refer the reader to the briefs and answer for the respective details thereof.

OPINION

In deciding this appeal, we considered the subject matter on appeal and the rejection advanced by the examiner. Furthermore, we duly considered the arguments and evidence of the appellants and examiner. After considering the totality of the record, we are persuaded that the examiner erred in rejecting claims 1-4 and 6-12, and 14. We are also persuaded that he did not err in rejecting claim 13. Accordingly, we affirm-in-part.

We begin by noting the following principles from In re Rijckaert, 9 F.3d 1531, 1532, 28 USPQ2d 1955, 1956 (Fed. Cir. 1993).

In rejecting claims under 35 U.S.C. Section 103, the examiner bears the initial burden of presenting a prima facie case of obviousness. In re Oetiker, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992).... "A prima facie case of obviousness is established when the teachings from the prior art itself would appear to have suggested the claimed subject matter to a person of ordinary skill in the art." In re Bell, 991 F.2d 781, 782, 26 USPQ2d 1529, 1531 (Fed. Cir. 1993) (quoting In re Rinehart, 531 F.2d 1048, 1051, 189 USPQ 143, 147 (CCPA 1976)).

We next find that the references represent the level of ordinary skill in the art. See In re GPAC Inc., 57 F.3d 1573, 1579, 35 USPQ2d 1116, 1121 (Fed. Cir. 1995)(finding that the Board of Patent Appeals and Interference did not err in concluding that the level of ordinary skill was best determined by the references of record); In re Oelrich, 579 F.2d 86, 91, 198 USPQ 210, 214 (CCPA 1978) ("[T]he PTO usually must evaluate ... the level of ordinary skill solely on the cold words of the literature."). Of course, "[e]very patent application and reference relies to some extent upon knowledge of persons skilled in the art to complement that [which is] disclosed'"

In re Bode, 550 F.2d 656, 660, 193 USPQ 12, 16 (CCPA 1977)
(quoting In re Wiggins, 488 F.2d 538, 543, 179 USPQ 421, 424
(CCPA 1973)). Those persons "must be presumed to know
something" about the art "apart from what the references
disclose."

In re Jacoby, 309 F.2d 513, 516, 135 USPQ 317, 319 (CCPA
1962).

The appellants argue, "the dedicating of the exclusive-
use third and fourth buses for the passing of context data
from a currently-executing program to a to-be-executed program
is nowhere taught or suggested by any of the cited art of
record, nor is it 'well known in the data processing art.'" (Reply Br. at 4.) The examiner responds, "[a]s to dedicating
the bus to a particular function, is it well known in the data
processing art that a dedicated bus will improve processing
speed for that particular function." (Examiner's Answer at
5.) We consider the persuasiveness of the argument and
response with respect to the following groups of claims:

- claims 1-4, 6-12, and 14
- claim 13.

Claims 1-4, 6-12, and 14

Claims 1-4 and 7-12 specify in pertinent part the following limitations: "third and fourth buses being exclusively used for switching between the presently executing program and the different program" Similarly, claim 6 specifies in pertinent part the following limitations: "a third bus for connecting said CPU with said RAM, said third bus being used only for passing data respectively held in said Program Counter Register, said Processor Status Word Register, and said General Purpose Register Set between said CPU and said RAM, ... a fourth bus for connecting said CPU with said RAM and passing address data corresponding to said data passed through said third bus....." Also similarly, claim 14 specifies in pertinent part the following limitations:

- a) executing a first program using said execution unit of said microcomputer, wherein said execution of said first program uses a processor status word, a program counter value and a register bank corresponding to said first program;
- b) receiving a request to perform a second program while said first program is executing;
- c) saving said processor status word, said program counter value and data stored in said register bank corresponding to said first program in a designated location in said RAM via a dedicated data bus and a dedicated address bus connecting said executing unit of said microcomputer and said RAM;

d) retrieving a processor status word, a program counter value and data to be stored in a register bank corresponding to said second program from another location in said RAM via said dedicated data bus and said dedicated address bus

Accordingly, claims 1-4, 6-12, and 14 require using dedicated buses only for context switching.

The examiner fails to show a suggestion of the limitations in the prior art. "The Patent Office has the initial duty of supplying the factual basis for its rejection. It may not ... resort to speculation, unfounded assumptions or hindsight reconstruction to supply deficiencies in its factual basis."

In re Warner, 379 F.2d 1011, 1017, 154 USPQ 173, 178 (CCPA 1967). "The range of sources available ... does not diminish the requirement for actual evidence. That is, the showing must be clear and particular. See, e.g., C.R. Bard Inc. v. M3 Sys., Inc., 157 F.3d 1340, 1352, 48 USPQ2d 1225, 1232 (Fed. Cir. 1998). Broad conclusory statements regarding the teaching of multiple references, standing alone, are not 'evidence.'" In re Dembiczak, 175 F.3d 994, 999, 50 USPQ2d 1614, 1617 (Fed. Cir. 1999)(exemplary citations omitted).

Here, the examiner admits that the AAPA does not disclose using dedicated buses for any reason, let alone only for context switching. He specifically concedes, "[a]pplicant's admission fails to detail the third and fourth bus." (Examiner's Answer at 5.) The examiner asserts, "Levy et al. (col. 6, lines 1-6) and Delagi et al. (col. 2, lines 5-10 et seq.; fig. 2) expressly detail the use of dedicated buses from the CPU to the RAM and a separate system bus." (Examiner's Answer at 5.) Although the references teach using dedicated buses, the buses are not used for context switching. In fact, the examiner does not allege, let alone show, that either Levy or Delagi even mention context switching. He also fails to show that Tanaka or Maejima remedy the defect of AAPA, Levy, and Delagi.

Because the examiner does not meet the requirement for actual evidence, we are not persuaded that teachings from the prior art would have suggested the limitations of "third and fourth buses being exclusively used for switching between the presently executing program and the different program;" "a

third bus for connecting said CPU with said RAM, said third bus being used only for passing data respectively held in said Program Counter Register, said Processor Status Word Register, and said General Purpose Register Set between said CPU and said RAM, ... a fourth bus for connecting said CPU with said RAM and passing address data corresponding to said data passed through said third bus"; and "a) executing a first program using said execution unit of said microcomputer, wherein said execution of said first program uses a processor status word, a program counter value and a register bank corresponding to said first program; ... saving said processor status word, said program counter value and data stored in said register bank corresponding to said first program in a designated location in said RAM via a dedicated data bus and a dedicated address bus connecting said executing unit of said microcomputer and said RAM; d) retrieving a processor status word, a program counter value and data to be stored in a register bank corresponding to said second program from another location in said RAM via said dedicated data bus and said dedicated address bus" The examiner fails to establish a prima facie case of obviousness. Therefore, we

reverse the rejections of claims 1, 6, 11, and 14 as obvious over AAPA in view of Levy and Delagi; claims 2, 4, 7-10, and 12 as obvious over AAPA in view of Levy and Delagi further in view of Tanaka; and claim 3 as obvious over AAPA in view of Levy, Delagi, and Tanaka further in view of Maejima. We next address claim 13.

Claim 13

"In the patentability context, claims are to be given their broadest reasonable interpretations. Moreover, limitations are not to be read into the claims from the specification."

In re Van Geuns, 988 F.2d 1181, 1184, 26 USPQ2d 1057, 1059 (Fed. Cir. 1993)(citing In re Zletz, 893 F.2d 319, 321, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989)). Here, claim 13 merely specifies in pertinent part the following limitations: "an exclusive-use data bus connected between said register file and said random access memory for data exchange therebetween and provided separately from said system bus" Giving the claim its broadest reasonable interpretation, the limitations recite using a dedicated bus to transfer data between a

register and a memory. The limitations do not require using the bus for context switching.

The combination of references would have suggested the limitations. "Non-obviousness cannot be established by attacking references individually where the rejection is based upon the teachings of a combination of references." In re Merck & Co., 800 F.2d 1091, 1097, 231 USPQ 375, 380 (Fed. Cir. 1986)(citing In re Keller, 642 F.2d 413, 425, 208 USPQ 871, 881 (CCPA 1981)). In determining obviousness, furthermore, a reference "must be read, not in isolation, but for what it fairly teaches in combination with the prior art as a whole." Id., 231 USPQ at 380.

Here, the rejection is based on a combination of AAPA, Levy, and Delagi. Regarding the AAPA, the appellants admit that MCUs were known to transfer data between a register in a CPU and a memory to execute an interrupt, switch a task, or call a subroutine. For example, they specifically concede, "[a]t this time, data held in the registers must be

temporarily saved in another location (usually, an external memory), and data necessary for the different program must be newly read from the outside and set in the registers." (Spec. at 1.) Both Levy and Delagi, moreover, teach using a dedicated bus to transfer data between a CPU and a memory. Levy specifically mentions "a fast memory **73**, which is coupled to the central processing unit **60** through dedicated bus **74**." Col. 6, ll. 5-6. For its part, Delagi specifically discloses that "[a] second port **8** of the high speed memory **7** is coupled directly to the arithmetic and logical unit **9** of central processor **2** by a high speed dedicated bus **10**." Col. 2, ll. 44-47. Persons skilled in the art, moreover, would have known that the central processing unit of Levy and the central processor of Delagi include registers to and from which data are transferred.

When the teachings of Levy and Delagi of using a dedicated bus to transfer data between a CPU and a memory were combined with the teaching of AAPA to transfer data between a register in a CPU and a memory, the result would be a

dedicated bus used to transfer data between a register and a memory. Accordingly, we are persuaded that the teachings of AAPA, Levy, and Delagi in combination with the prior art as a whole would have suggested the claimed limitations of "an exclusive-use data bus connected between said register file and said random access memory for data exchange therebetween and provided separately from said system bus" Therefore, we affirm the rejection of claim 13 as obvious over AAPA in view of Levy and Delagi. Our affirmance is based only on the arguments made in the brief. Arguments not

made therein are not before us, are not at issue, and are considered waived.

CONCLUSION

In summary, the rejection of claims 1, 6, 11, and 14 under 35 U.S.C. § 103(a) as obvious over AAPA in view of Levy and Delagi; the rejection of claims 2, 4, 7-10, and 12 under 35 U.S.C. § 103(a) as obvious over AAPA in view of Levy and Delagi further in view of Tanaka; and the rejection of claim 3 under 35 U.S.C. § 103(a) as obvious over AAPA in view of Levy, Delagi, and Tanaka further in view of Maejima are reversed. The rejection of claim 13 under 35 U.S.C. § 103(a) as obvious over AAPA in view of Levy and Delagi, however, is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a).

AFFIRMED-IN-PART

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Administrative Patent Judge)	
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Appeal No. 1997-2983
Application No. 08/482,792

Page 18

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