

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 40

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte ROBERT J. GOVE, KEITH BALMER,
NICHOLAS K. SIMMONS and
KARL M. GUTTAG

Appeal No. 97-2473
Application No. 08/264,582¹

ON BRIEF

Before THOMAS, HAIRSTON, and BARRY, Administrative Patent Judges.

BARRY, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on the appeal under 35 U.S.C. § 134 from the final rejection of claims 1-3, 23, 24, and 44-67.

¹ The application, entitled "Reduced Area of Crossbar and Method of Operations," was filed June 22, 1994. The application is a continuation of Application Serial No. 07/437,852, which was filed November 17, 1989 and is now abandoned.

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The appellants filed an amendment after final rejection on August 1, 1996, which was entered. The amendment canceled claims 1-67 and added claims 68-83. We reverse.

BACKGROUND

The invention at issue in this appeal relates to interconnecting the components of a multi-processor system. It interconnects the system's plural processors and plural memories by a crossbar switch. The switch can be reconfigured to achieve different combinations of distributed and shared memory arrangements. The switch, processors, and memories are integrated on a single chip to facilitate communications among these components.

Claim 68, which is representative for our purposes, follows:

68. A multi-processing system comprising:
a plurality of n processors, each of said processors operable from an instruction stream provided from a memory source for controlling a process, said process relying on the movement of data to and from one or more addressable memories, each processor having a first data port and a second data port;
a plurality of m memory sources, each memory source having a unique addressable space;
a switch matrix having first links connected to said memories and second links connected to said first and second data ports of said processors, said

switch matrix selectively connecting said first and second links whereby said first data port of each of said n processors may access any of said m memory sources and said second data port of each of said n processors may access only a predetermined corresponding subset of said m memory sources. (Appeal Br. at 18.)

The references relied on by the patent examiner in rejecting the claim follow:

Barnes et al. (Barnes) 1982	4,365,292	Dec. 21,
Chang 1991	5,056,000	Oct. 8,
	(effective filing date of June 21,	
1988)		
Ewert 1993	5,247,689	Sept. 21,
	(effective filing date of Feb. 25,	
1985).		

Claims 68, 69, 72-77, and 80-83 stand rejected under 35 U.S.C. § 103 as obvious over Barnes in view of Chang or Ewert. (Examiner's Answer at 4.)² Rather than repeat the arguments of the appellants or examiner in toto, we refer to the appeal

² Claims 70, 71, 78, and 79 stand objected to as being dependent on rejected base claims. (Examiner's Answer at 2.)

and reply briefs and the examiner's answers for the respective details thereof.

OPINION

In reaching our decision in this appeal, we considered the subject matter on appeal and the rejection and evidence advanced by the examiner. We also considered the appellants' and examiner's arguments. After considering the record before us, it is our view that the evidence and level of skill in the art would not have suggested to one of ordinary skill in the art the

invention of claims 68, 69, 72-77, and 80-83. Accordingly, we reverse.

We begin our consideration of the obviousness of the rejected claims by recalling that in rejecting claims under 35 U.S.C. § 103, the patent examiner bears the initial burden of establishing a prima facie case of obviousness. A prima facie case is established when the teachings from the prior art itself would appear to have suggested the claimed subject matter to a person of ordinary skill in the art. If the examiner fails to establish a prima facie case, an obviousness rejection is improper and will be overturned. In re Rijckaert, 9 F.3d 1531, 1532, 28 USPQ2d 1955, 1956 (Fed. Cir. 1993). With this in mind, we analyze the examiner's rejection.

Regarding independent claim 68, the examiner notes that Barnes teaches a data processing system comprising a plurality of n processors, each of said processors operable from an instruction stream provided from a memory for controlling a

process; a plurality of memory sources having unique addressable space; and a switching matrix having links connected to the processing units and memory sources. The examiner admits that

Barnes does "not specifically detail that his switching network was connected to a plurality of data ports."

(Examiner's Answer at 4.)

The examiner observes that Chang teaches a multi-processing system including an interconnection switching network for selectively interconnecting processing units and a memory source. The examiner also observes that Ewert teaches a plurality of processing units in which each processing unit has a plurality of data ports and is selectively interconnected through a switching network to a common, main memory. (Id.)

The examiner concludes that it would have been obvious to a person of ordinary skill in the art to combine the teachings of Barnes and Chang or Ewert "because they all are directed to the solutions to the problems of plural processing units and memory source interconnection. Especially, the plural ports and selective interconnections of Ewert and Chang et al. [W]ould give very flexible and cheaper system to Barnes et

al.[,s] system." (Id. at 4-5.) The examiner adds, "[s]ince the steps in the method claims are performed by the apparatus of the apparatus claims, the method claims are rejected based on the rejections of the apparatus claims." (Id. at 5.) "As to claim the master processor of claim 82," asserts the examiner, "Barnes et al. [E]xactly taught master control for instruction scheduling and synchronization control" (Id.)

In response, the appellants submit that neither Barnes nor Chang "contain any indication that each of the processors have the two data ports" recited in independent claims 68, 74, and 82. (Appeal Br. at 7.) They also submit that Chang "includes no teaching" that the reference's interconnection switch allows connection of the two data ports of its processors to differing sets of memories. (Id. at 9.) In addition, the appellants argue that neither the combination of Barnes and Ewert nor Ewert alone teaches "or makes obvious" the subject matter of the first data port of each processor having access to all memories while the second data port of

each processor has access to only a subset of the memories.

(Reply Br. at 4.)

Regarding independent claims 68, 74, and 82; we find Barnes, Chang, and Ewert fail to teach or to have suggested the first and second data ports as claimed. The claims recite in pertinent part that each of a plurality of processors has a first and a second data port. The claims further recite that a switch matrix is connected to the ports, by which the first port may access "any of said m memory sources," (Appeal Br. at 18, 20, 22), while the second port may access "only a predetermined corresponding subset of said m memory sources." (Id.) Comparison of the claim language to Barnes, Chang, and Ewert, evidences that the references neither teach nor would have suggested the claimed first and second data ports.

Barnes discloses a connection network 15 for interconnecting an array of data processors 29 with an array of memory modules 13. Col. 1, ll. 13-15. The examiner admits that the reference does not disclose two data ports.

(Examiner's Answer at 6, Final Rejection at 2.) Indeed, Figures 2 and 3 of Barnes depict only a single port in each processor for coupling it to the connection network. The reference, furthermore, lacks any teaching of or suggestion to restrict access of the single port to only a subset of the memory modules.

Chang teaches a computer having a plurality of processors. One processor is a master processor 26; the others are slave processors 20, 22, and 24. Each processor is connected through an interconnection switch 42 to a shared multiaccess memory (MAM) with multiple memory modules 44, 46, 48, and 50. Col. 2, ll. 12-21.

The examiner does not show or even allege that Chang discloses two data ports. In fact, Figures 2 and 8 of Chang depict only a single data line between each of the slave processors and the interconnection switch. Figure 9 similarly depicts only a single MAM interface 130, with a single data port, for each processor. Chang lacks any teaching of or

suggestion to connect the data port of a processor to only a subset of the MAM modules. To the contrary, the reference discloses that the interconnection switch can be configured so that any processor is connected to any MAM module. Id. at col. 3, ll. 36-40.

Ewert discloses a parallel digital processor including a plurality of parallel processing modules (PPMs) coupled to a common, main memory. Col. 17, ll. 9-11. Each PPM includes three ports, col. 4, l. 3, including two data ports. Col. 2, ll. 52-55. The first and second data ports are associated with A register 12 and B register 13, respectively, in the PPM. Col. 4, ll. 3-5.

The memory is organized in rows and columns. A single, separate memory column is dedicated to each port. Id. at col. 2, ll. 59-60. For example, MA1 memory column 22 is coupled to A register 12 of the PPM via A-bus 32. MB1 memory column 23 is coupled to B register 13 via B-bus 33. In contrast to the claimed invention, which permits the first port access to any

of the memory sources, Ewert does not teach connecting register A 12 to exchange data with any memory other than the MA1. Nor does the reference teach connecting register B 13 to exchange data with any memory other than MB1.

The examiner cites column 3, lines 25-34, of Ewert as teaching the limitation that the first port may access any of the memory sources while the second port may access only a subset thereof. (Supplemental Examiner's Answer, ¶ 4.) The cited portion of the reference describes "being able to transfer data laterally" Col. 3, ll. 29-30. Laterally transferring data refers to exchanging data between PPMs or between columns in memory. Id. at 30-31. Ewert does not permit lateral data transfer between processors and memories. Without some indication that such transfer is feasible, one skilled in the art would not have been motivated to employ the reference's switches and lateral transfer buses to couple registers A 12 and B 13 to any memory other than MA1 and MB1, respectively.

For the foregoing reasons, the examiner failed to show that Barnes, Chang, and Ewert teach or would have suggested the first and second data ports of independent claims 68, 74, and 82. Therefore, we find the examiner's rejection does not amount to a prima facie case of obviousness. Because the examiner has not established a prima facie case, the rejection of claims 68, 69, 72-77, and 80-83 over Barnes in view of Chang or Ewert is improper. Therefore, we reverse the rejection of the claims under 35 U.S.C. § 103.

CONCLUSION

To summarize, the decision of the examiner to reject claims 68, 69, 72-77, and 80-83 under 35 U.S.C. § 103 is reversed.

REVERSED

JAMES D. THOMAS)	
Administrative Patent Judge)	
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)	BOARD OF PATENT
KENNETH W. HAIRSTON)	APPEALS
Administrative Patent Judge)	AND
)	INTERFERENCES
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LANCE LEONARD BARRY)	
Administrative Patent Judge)	

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