

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 10

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte NILESH SHAH, JAMES COKE,
JASMIN AJANOVIC,
DAHMANE DAHMANI, and
RAJEEV PRASAD

Appeal No. 97-2470
Application No. 08/201,817¹

ON BRIEF

Before HAIRSTON, KRASS, and BARRY, Administrative Patent Judges.
BARRY, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on the appeal under 35 U.S.C. § 134 from the final rejection of claims 1 through 21. We reverse.

¹ The application was filed February 24, 1994.

BACKGROUND

The invention at issue in this appeal relates to bridges for interconnecting buses. A fast, Peripheral Component Interconnect (PCI) bus and a slow, secondary bus connect the components of a computer. Accesses to one of the buses by a component, i.e., a "bus master," on the other bus is accomplished through a bridge connecting the buses.

The bridge accelerates the transfer of data in the computer by two means. First, after a PCI bus master is denied access to the secondary bus when it is busy, the bridge masks any retry by the bus master until the bus is again available. Because retries are masked, the PCI bus is not occupied needlessly by a retrying bus master. Second, after the secondary bus is again available, the bridge guarantees a PCI bus master access to the bus in favor of a secondary bus master. This reduces "thrashing" on the PCI bus that results when a PCI bus master is forced to continually retry access to the secondary bus.

Claim 1, which is representative for our purposes,
follows:

Claim 1. A bridge circuit adapted to be associated
with first and second bus circuits to transfer
data therebetween comprising:

data buffers for storing data being transferred
between the buses,

a circuit for causing a bus master on the first bus
which has attempted an access of the second bus
through the bridge circuit to retry its access,

circuitry for masking any retry until the second bus
is again available, and

circuitry for providing an interval during which a
bus master on the secondary bus may not gain access
to the second bus after the second bus is
relinquished so that a sequence of retry operations
causing a thrashing condition on the first bus is
not generated.

The reference relied on by the patent examiner in
rejecting the claims follows:

Heil et al. (Heil)	5,418,914	May
23, 1995		
	(effective filing date Sept. 17, 1991)	

Claims 1 through 21 stand rejected under 35 U.S.C.
§ 102(e) as anticipated by Heil. (Examiner's Answer, ¶ 9.)
Rather than repeat the arguments of the appellants or examiner

in toto, we refer to the appeal and reply briefs and the examiner's answers for the respective details thereof.

OPINION

In reaching our decision in this appeal, we considered the subject matter on appeal and the rejection and evidence advanced by the examiner. We also considered the appellants' arguments.

It is our view that the applied reference does not anticipate the invention of claims 1 through 21. Accordingly, we reverse.

We begin our consideration of the novelty of the claims by recalling that a prior art reference anticipates a claim only if the reference discloses expressly or inherently every limitation of the claim. Absence from the reference of any claimed element negates anticipation. Rowe v. Dror, 112 F.3d 473, 478, 42 USPQ2d 1550, 1553 (Fed. Cir. 1997). With this in mind, we analyze the examiner's rejection.

The examiner begins the rejection of claims 1 through 21 by noting Heil discloses a processor means, main memory means, first bus adapted to be connected to bus master means and bus slave means, second bus means adapted to be connected to bus master and bus slave, and an interface module for transferring addresses and data between the first and second buses.

(Examiner's Answer, ¶ 9.) The interface module, further observes the examiner, comprises data buffer means for storing data being transferred between the buses, means for

generating a busy signal when the second bus is in a busy state, logic for generating a retry signal, and means for masking any retry until the second bus is again available. The examiner concludes the rejection by opining that the interface module also comprises "the claimed means for providing an interval (See Fig. 3; especially signals "PRQ_L", "PACK_L", "MC_BUSY_L" and Clock 6-20)". (Id.) Amplifying the last point, the examiner notes "column 5, line 31 - column 6, line 8 'The applicable MCRETRYL signal is driven low ... Clock 16-20 Processor 22 successfully accesses interface 28.'" (Id., ¶ 11.) "In these two paragraphs," asserts the examiner, Heil discloses the claimed interval providing means. (Id.)

In response, the appellants assert that Heil fails to show any means for providing an interval as set forth by the present invention. They add the reference's timing diagram, viz., Fig. 3, fails to illustrate any function like that provided by the timer of the present invention. (Appeal Br. at 6.) The appellants also submit that Heil does not show the capability of denying a secondary bus master ownership of the secondary bus. (Id. at 7-8.)

Regarding independent claims 1 and 6, we find Heil fails to teach the circuitry for providing an interval as claims. The claims recite in pertinent part circuitry for providing an interval during which a bus master on the second bus may not gain access to the second bus after the second bus is relinquished so that a sequence of retry operations causing a thrashing condition on the first bus is not generated. (Spec. at 26, 28.) Comparison of the claim language to the teaching of Heil evidences that the reference does not teach the claimed circuitry for providing an interval.

Heil teaches a retry scheme for eliminating deadlock on a first bus containing transactions directed to a second, unavailable bus. Col. 1, ll. 9-11. An interface circuit connects the first and second buses. The interface circuit includes logic for generating a busy signal when the second bus is busy and logic for generating a retry signal when the interface circuit is addressed by a bus master while the second bus is busy. Each bus master includes logic for receiving the retry signal and relinquishing control of the

first bus upon receipt of the retry signal. A bus arbiter includes logic for receiving the busy signal and preventing any bus master seeking access to the second bus from participating in arbitration for control of the first bus until the busy signal has been negated. Col. 2, ll. 55-68.

The reference further teaches, “[u]pon negation of the busy signal, all bus masters will be permitted to compete for ownership of the bus.” Id. at ll. 52-54 (emphasis added). Heil does not provide an interval during which a bus master on the secondary bus is denied access to the secondary bus after negation of the busy signal, i.e., after the second bus is relinquished. The absence of the claimed circuitry for providing an interval from the reference negates anticipation of independent claims 1 and 6 and their dependent claims 2 through 5 and 8 through 10, respectively.

Similar to claims 1 and 6, the other independent claims; viz., claims 11 and 15, 18, and 21; specify a timer circuit, means for providing an interval, and a step of precluding a bus master, respectively. These limitations similarly are not

taught by Heil. The absence of the claimed elements from the reference negates anticipation of the respective independent claims and their dependent claims. Therefore, we reverse the rejection of claims 1 through 21 under 35 U.S.C. § 102(e).

CONCLUSION

To summarize, the decision of the examiner to reject claims 1 through 21 under 35 U.S.C. § 102(e) is reversed.

REVERSED

KENNETH W. HAIRSTON)	
Administrative Patent Judge)	
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)	BOARD OF PATENT
ERROL A. KRASS)	APPEALS
Administrative Patent Judge)	AND
)	INTERFERENCES
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LANCE LEONARD BARRY)	
Administrative Patent Judge)	

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