

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 33

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte SAFDAR M. ASGHAR,
and JOHN G. BARTKOWIAK

Appeal No. 1997-2160
Application 07/548,709

ON BRIEF

Before KRASS, BARRETT, and GROSS, Administrative Patent Judges.

KRASS, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 1 through 9, 22, 23 and 26 through 30, all of the claims pending in the application.

The invention is directed to a communications processor for voice-band telecommunications.

More particularly, a single integrated circuit chip is employed and on that

chip is a central processing unit (CPU) and a digital signal processing unit (DSP). A static scheduler partitions execution of the signal processing algorithm between the CPU and the DSP.

Representative independent claim 1 is reproduced as follows:

1. An apparatus, comprising:

in a single integrated circuit chip, the combination of:

a central processing unit (cpu) having a cpu instruction set, an execution unit with an arithmetic logic unit, a program counter, a bus interface, and an interrupt processor including a non-maskable interrupt input;

a digital signal processor (dsp) having a dsp instruction set to carry out a digital signal processing algorithm, an execution unit for carrying out multiply and accumulate operations and an external interface, said dsp being capable of executing simultaneously with said cpu;

an address bus connected between said cpu and said dsp;

a memory accessible by said cpu and said dsp;

a scheduling means for statically scheduling execution of one algorithm between said cpu and said dsp, said scheduling means transmitting non-maskable interrupts to said cpu non-maskable interrupt input to effect execution of portions of said algorithm to be executed by said cpu; and

a data bus connected between said cpu and said dsp.

The examiner relies on the following references:

Ino	4,896,576	Jan. 30, 1990
Tokuume	4,979,102	Dec. 18, 1990
Yamazaki et al. (Yamazaki)	5,293,586	Mar. 8, 1994 (filed Sept. 29, 1989)

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Claims 1 through 9, 22, 23 and 26 through 30 stand rejected under 35 U.S.C. § 103. As evidence of obviousness, the examiner cites Yamazaki in view of Tokuume with regard to claims 1 through 6, 8, 9, 22, 23 and 26 through 30, adding Ino with regard to claim 7.

Reference is made to the briefs and answers for the respective positions of appellants and the examiner.

OPINION

We will reverse the rejection of claims 1 through 9, 22, 23, 28 and 30 under 35 U.S.C. §103 but we will sustain the rejection of claims 26, 27 and 29 under 35 U.S.C. § 103.

Turning first to independent claims 1 and 30, each of these claims recites a “scheduling means for statically scheduling execution” of one algorithm between said cpu and said dsp (claim 1) or "of the signal processing algorithm between said digital signal processor and said cpu” (claim 30).

Appellants argue that while Yamazaki does disclose a CPU and DSP on a single chip, it differs from the instant claimed invention because while Yamazaki enables two different routines to be executed simultaneously by a CPU and a DSP, the present invention enables a single routine to be executed in the most efficient manner by a CPU and DSP [principal brief-page 5].

Appellants contend that this difference is brought out in the recitation of a “static scheduler” because the static scheduler partitions the instructions of a single routine between the CPU and the DSP.

We disagree with appellants and hold that Yamazaki clearly discloses a static scheduler in that the DSP in Yamazaki is scheduled to process fonts, under the condition that the required font is not in the CPU-addressed cache (working area 2A in memory – see Figure 2 of Yamazaki), while the CPU handles all other processing requirements. Accordingly, Yamazaki schedules each of the CPU and DSP to different tasks and these tasks are assigned in a predetermined manner. Since it has been determined beforehand as to what jobs the DSP will handle (font processing) and what jobs the CPU will handle (all other processing), it is clear to us that what Yamazaki has disclosed is a “static scheduler.” Clearly, Yamazaki does not “dynamically” determine which processor will handle which job based on what went on before. On the contrary, Yamazaki determines, in a predetermined manner, i.e., statically, which processor is to handle which job. Thus, Yamazaki does disclose a static scheduler, as claimed.

However, claims 1 and 30 also require that the scheduling means transmit “non-maskable interrupts to said cpu non-maskable input...” [claim 1] or transmit “interrupt signals to said cpu non-maskable interrupt input” [claim 30]. It is this claimed limitation that we do not find disclosed or suggested in the applied references.

The examiner contends that the claimed transmission of “non-maskable interrupts” is “nothing

more than handshake signals between two processors” [Page 8-principal answer], that Yamazaki discloses communication between the CPU and the DSP, at column 7, lines 44-46, and that whether or not a handshake is maskable is dependent on the importance of the job to be processed. It appears to us that the examiner misses the point. The language of claims 1 and 30 requires the non-maskable interrupts to be transmitted “*to said cpu.*” This means that it is the CPU, in the instant invention, which is being controlled, i.e., the CPU would be the slave in a master/slave relationship. In Yamazaki, it is the CPU that takes precedence and does the controlling. We find nothing within the disclosure of Yamazaki, or of Tokuume for that matter, which suggests that any non-maskable interrupt signals are sent to the CPU.

Accordingly, we will not sustain the rejection of claims 1 and 30 under 35 U.S.C. § 103 and, as a consequence, we also will not sustain the rejections of claims 2 through 9, 22 and 23, dependent thereon. With regard to claim 7, we do not find that Ino provides for the deficiencies noted above with regard to a lack of teaching the claimed transmission of non-maskable interrupts to the CPU by Yamazaki and Tokuume.

With regard to independent claim 26, we will sustain the rejection of this claim under 35 U.S.C. § 103 because it does not contain the limitation of a transmission of a non-maskable interrupt to the CPU. Appellants’ only argument, regarding the rejection of this claim, is that the applied references do not suggest the claimed “scheduling means for statically scheduling execution of the signal processing

algorithm ...” However, as explained supra, it is our view that Yamazaki does, indeed, disclose such a static scheduling means, as broadly claimed. We would also note that to the extent that appellants’ static “scheduling means” is something more than a predetermined schedule of which processor handles which job, the instant specification offers scant detail as to this scheduling means, it not even being very clear as to what disclosed structure comprises such “scheduling means.”

We will also sustain the rejection of claims 27 and 29 under 35 U.S.C. § 103 since they depend from independent claim 26 and appellants present no separate arguments as to the merits of these claims.

With regard to claim 28, appellants do argue the merits of this claim separately, i.e., that the applied references do not show or suggest the claimed CPU and DSP instruction sets having “minimum overlapping instructions.” The examiner’s response is to point to column 3, lines 24 et seq. of Yamazaki to show that the DSP and CPU can proceed independently with different processing . However, that portion of Yamazaki emphasizes that the CPU and DSP can process completely different instruction sets and there would be no overlap occurring under those conditions. While the claimed “minimum overlapping instructions” might be interpreted as *no* overlap, since no overlap is certainly a *minimum* overlap, we do not think this would be a fair interpretation in view of appellants’ disclosure of *some* overlap of processing operations.

The examiner states that the “instructions in Yamazaki can be overlap [sic] also if the same

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instruction is useable by both processors or if both processors are required to perform the same operation identified in an instruction” [Page 8-principal answer]. However, the examiner has provided no evidence of what instruction sets of Yamazaki overlap or might overlap, as claimed. Accordingly, we will not sustain the rejection of claim 28 under 35 U.S.C. § 103 based on the evidence provided by the examiner.

We have sustained the rejection of claims 26, 27 and 29 under 35 U.S.C. § 103 but we have not sustained the rejection of claims 1 through 9, 22, 23, 28 and 30 under 35 U.S.C. § 103. Accordingly, the examiner’s decision is affirmed-in-part.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a).

AFFIRMED-IN-PART

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