

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 29

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte SILVIA PADOAN and CARLA GOLLA

Appeal No. 1997-2034
Application No. 08/347,788

HEARD: November 7, 2001

Before FLEMING, GROSS, and LEVY, Administrative Patent Judges.
GROSS, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the examiner's final rejection of claims 1, 2, 4, 6, 7, 9, 11, 13 through 18, 23, and 26 through 30. Claims 3, 5, 8, 10, 12, 24, and 25 have been canceled. Claims 19 through 22 have been withdrawn from consideration as directed to a non-elected invention.

Appellants' invention relates to a circuit for generating a stable reference voltage by compensating for temperature and process parameters. In particular, the circuit is formed with two natural transistors of opposite conductivity type, with

the reference voltage being the difference between the threshold voltages of the two transistors. Claim 1 is illustrative of the claimed invention, and it reads as follows:

1. A circuit comprising:

a first diode-connected natural field effect transistor connected, in series with a load element, between first and second power supply connections; said first transistor and said load element having an intermediate node therebetween;

a second diode-connected natural field effect transistor connected between said intermediate node and an output node;

wherein said first and second transistors are of opposite conductivity types, and said first transistor has a threshold voltage whose absolute value is more than the absolute value of the threshold voltage of said second transistor;

whereby said output terminal provides a voltage which is equal to the threshold voltage of said first transistor reduced by the absolute value of the threshold voltage of said second transistor.

The prior art references of record relied upon by the examiner in rejecting the appealed claims are:

Lee et al. (Lee) 1974	3,805,095	Apr. 16,
Yoshida et al. (Yoshida) 28, 1976	4,000,429	Dec.
Numata et al. (Numata) 1978	4,096,382	Jun. 20,

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Claims 1, 2, 4, 6, 7, 9, 11, 13 through 18, 23, and 26 through 30 stand rejected under 35 U.S.C. § 103 as being unpatentable over Numata in view of Yoshida or Lee.

Claims 1, 2, 4, 6, 7, 9, 11, 13 through 18, 23, and 26 through 30 stand rejected under 35 U.S.C. § 103 as being unpatentable over Yoshida or Lee.

Reference is made to the Examiner's Answer (Paper No. 18, mailed December 11, 1996) for the examiner's complete reasoning in support of the rejections, and to appellants' Brief (Paper No. 17, filed October 22, 1996) and Reply Brief (Paper No. 19, filed January 15, 1997) for appellants' arguments thereagainst.

OPINION

We have carefully considered the claims, the applied prior art references, and the respective positions articulated by appellants and the examiner. As a consequence of our review, we will reverse the obviousness rejections of claims 1, 2, 4, 6, 7, 9, 11, 13 through 18, 23, and 26 through 30.

Independent claims 1, 9, and 23 require two natural field effect transistors. Claim 15 requires two field effect transistors which "do not include any dopant concentration in

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the respective channels thereof corresponding to said VT-adjust implant," the definition given on page 7 of the specification for natural transistors. Thus, all of the claims include two natural field effect transistors.

The examiner admits (Answer, page 4) that none of the references (Numata, Yoshida, and Lee) explicitly discloses natural transistors. Nonetheless, the examiner concludes that the use of natural transistors in the combination of the three references would have been obvious because "appellants' definition of 'natural' transistors is simply that the transistors have no VT-adjust implanting, i.e., their thresholds will vary proportionately to changes in temperature/process variations. Since the FETs of the three references clearly have such a characteristic (indeed, this is how the references perform their temperature compensation)," the use of natural transistors in the combination of the references would have been obvious.

We find no evidence in any of the references that natural transistors are employed and no suggestion as to why they should be utilized. In particular, as Numata uses diodes, not transistors, we, unlike the examiner, find it difficult to

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draw inferences about the FETs of Numata. As to Yoshida, we find no mention whatsoever of temperature compensation. Therefore, the examiner's reasoning that Yoshida's thresholds clearly vary proportionately to changes in temperature and process variations because that is how Yoshida performs temperature compensation is puzzling to us. Lastly, although Lee is directed to threshold variations, Lee makes no mention of temperature compensation. Therefore, the examiner's assertion as to the characteristics of Lee's FETs appears to be unfounded. Furthermore, we infer from Lee's disclosure that natural transistors actually are not used as Lee requires an additional transistor T16 to achieve a constant output voltage. Thus, the examiner has failed to establish a *prima facie* case of obviousness.

We note that the examiner's further motivations for modifying the references fail to meet the standards set forth in *In re Fine*, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988), wherein the court held that the examiner must establish a factual basis to support the legal conclusion of obviousness. In so doing, the examiner is required to make

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the factual determinations set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 17-18, 148 USPQ 459, 467 (1966). The examiner must provide a reason why one having ordinary skill in the pertinent art would have been led to modify the prior art to arrive at the claimed invention. Such reason must stem from some teaching, suggestion or implication in the prior art as a whole or knowledge generally available to one having ordinary skill in the art. *Uniroyal, Inc. v. Rudkin-Wiley*, 837 F.2d 1044, 1052, 5 USPQ2d 1434, 1438 (Fed. Cir. 1988), *cert. denied*, 488 U.S. 825 (1988); *Ashland Oil, Inc. v. Delta Resins & Refractories, Inc.*, 776 F.2d 281, 293, 227 USPQ 657, 664 (Fed. Cir. 1985), *cert. denied*, 475 U.S. 1017 (1986).

In the present case, the examiner concludes (Answer, pages 4-5) that making the threshold of the FET between the intermediate node and ground higher than that of the FET between the intermediate node and the output (as recited in independent claims 1 and 9) would have been obvious "for the purpose of simplifying the circuit." The examiner provides no factual basis for this conclusion. Similarly, the examiner baldly asserts, with no corroborating evidence (Answer, page

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5), that making the two diode-connected FETs of opposite conductivity (as recited in independent claims 1, 9, and 15) would have been obvious "since it is notoriously well-known in the semiconductor art that NMOS and PMOS field effect transistors can be substituted for each other without any unexpected results or change in circuit operation." In fact, the examiner ignores the explicit disclosures of Yoshida and Lee that either n-channel or p-channel transistors may be used for both FETs. Accordingly, we cannot sustain the obviousness rejections of claims 1, 2, 4, 6, 7, 9, 11, 13 through 18, 23, and 26 through 30.

CONCLUSION

The decision of the examiner rejecting claims 1, 2, 4, 6, 7, 9, 11, 13 through 18, 23, and 26 through 30 under 35 U.S.C. § 103 is reversed.

REVERSED

MICHAEL R. FLEMING)
Administrative Patent Judge)
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RAYMOND M. GALASSO
JENKENS & GILCHRIST
1445 ROSS AVENUE
SUITE 3200
DALLAS, TX 75202-2799