

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 24

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES

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Ex parte KARL M. GUTTAG, KEITH BALMER,  
ROBERT J. GOVE, CHRISTOPHER J. READ, JEREMIAH E. GOLSTON,  
SYDNEY W. POLAND, NICHOLAS ING-SIMMONS and PHILIP MOYSE

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Appeal No. 97-1057  
Application 08/160,298<sup>1</sup>

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ON BRIEF

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Before HAIRSTON, KRASS and JERRY SMITH, Administrative Patent Judges.

JERRY SMITH, Administrative Patent Judge.

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<sup>1</sup> Application for patent filed November 30, 1993.

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DECISION ON APPEAL

This is a decision on the appeal under 35 U.S.C. § 134 from the examiner's final rejection of claims 1-97, which constitute all the claims in the application. Appellants have indicated that the appeal is withdrawn with respect to claims 28 and 69 [supplemental reply brief, page 5]. Accordingly, this appeal now involves only claims 1-27, 29-68 and 70-97.

The final rejection of the claims under 35 U.S.C. § 112 was withdrawn in the initial examiner's answer [page 11], but a new rejection of some of the claims on this ground was made in this answer [pages 8-9]. The first supplemental answer subsequently indicated that the new rejection under Section 112 had been withdrawn [page 1], and the second supplemental answer listed no rejections under Section 112. Thus, there are no longer any pending rejections of the claims under 35 U.S.C.

§ 112. In the second supplemental examiner's answer, the examiner indicated that a rejection of claims 4-8, 14, 15, 29-33, 35, 45-49, 55, 56, 70-74 and 76 under 35 U.S.C. § 103 had been withdrawn [page 2].

The claimed invention pertains to a data processing apparatus having an arithmetic logic unit (ALU) with three separate multibit digital inputs. The ALU performs mixed arithmetic and Boolean operations on the three inputs. A shifter is connected to one of the three inputs for shifting the digital signal received at that input. A mask generator is also provided which generates a multibit digital mask signal as one of the three inputs to the ALU. A function control input to the ALU determines which operations will be performed on the three multibit digital inputs received by the ALU.

Representative claim 1 is reproduced as follows:

1. A data processing apparatus comprising:

an arithmetic logic unit having first, second and third data inputs for multibit digital signals representing corresponding first, second and third input signals, and a function control input for receiving a function signal, said arithmetic logic unit generating at an output a multibit digital signal representing a mixed arithmetic and Boolean combination of said first, second and third inputs corresponding to said function signal, said mixed arithmetic and Boolean combination including at least the following two mixed arithmetic and Boolean combinations (1) an arithmetic combination of only said first and second inputs, and (2) an arithmetic combination of only said first and third inputs;

a first data source supplying a first multibit digital signal to said first data input of said arithmetic logic unit;

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a second data source supplying a second multibit digital signal;

a shifter having a data input connected to said second data source, a shift control input receiving a shift control signal, and a data output connected to said second data input of the arithmetic logic unit, said shifter shifting said second multibit digital signal an amount corresponding to said shift control signal and supplying said shifted second multibit digital signal to said second data input of said arithmetic logic unit;

a third data source supplying a third multibit digital signal; and

a mask generator having a data input connected to said third data source and a data output connected to said third data input of said arithmetic logic unit, said mask generator generating a multibit digital mask signal corresponding to said third multibit digital signal.

The examiner relies on the following references:

Chu et al. (Chu)	4,785,393	Nov. 15, 1988
Pfeiffer et al. (Pfeiffer)	5,146,592	Sep. 08, 1992
Vassiliadis et al. (Vassiliadis)	5,299,319	Mar. 29, 1994
		(filed Mar. 29, 1991)

Claims 1-27, 29-68 and 70-97 stand provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-93 of copending application Serial No. 08/160,111. Claims 1-3, 9-13, 16-27, 34, 36-44, 50-54, 57-68, 75, 77-82 and 95-97 also stand rejected under 35 U.S.C. § 103 as unpatentable over the

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teachings of Chu and Vassiliadis. Finally, claims 83-97 also stand rejected under 35 U.S.C. § 103 as unpatentable over the teachings of Chu, Vassiliadis and Pfeiffer.

Rather than repeat the arguments of appellants or the examiner, we make reference to the briefs and the answers for the respective details thereof.

#### OPINION

We have carefully considered the subject matter on appeal, the rejections advanced by the examiner and the evidence of obviousness relied upon by the examiner as support for the rejections. We have, likewise, reviewed and taken into consideration, in reaching our decision, the appellants' arguments set forth in the briefs along with the examiner's rationale in support of the rejections and arguments in rebuttal set forth in the examiner's answers.

It is our view, after consideration of the record before us, that the provisional obviousness-type double patenting rejection should be sustained. We are also of the view that the collective evidence relied upon and the level of skill in the particular art would have suggested to one of ordinary skill in the art the obviousness of the invention as

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set forth in claims 1-3, 9-13, 39, 42-44, 50-54, 80 and 83-97. We reach the opposite conclusion with respect to claims 16-27, 34, 36-38, 40, 41, 57-68, 75, 77-79, 81 and 82. Accordingly, we affirm.

We consider first the provisional rejection of claims 1-27, 29-68 and 70-97 on the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-93 of copending application Serial No. 08/160,111. According to the examiner, the only difference between the claims of this application and the claims of the copending application is the recitation of a barrel rotator in the claims of the copending application in place of the shifter recited in the claims in this application. The examiner provides a reason as to why it would have been obvious to the artisan to use a shifter in place of the claimed barrel rotator of the copending application [answer, pages 3-4].

Appellants' only response to this rejection is to indicate that the rejection should be held in abeyance until all other issues have been resolved in accordance with the procedure of MPEP § 804 [brief, page 4]. The section of the MPEP referred to by appellants merely provides guidance to the

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examiner as to what to do when an application is otherwise ready for allowance except for the double patenting rejection. The MPEP does not relieve an applicant of the burden of arguing the merits of the rejection. In fact, section 804 specifically states that the merits of a provisional double patenting rejection can be addressed by the examiner and applicant without waiting for a patent to issue [page 800-15, section B]. Thus, the merits of the obviousness-type double patenting rejection can be considered even though there are other rejections pending against the claims.

Since the examiner has pointed out the difference between the claims of this application and the claims of copending application Serial No. 08/160,111 and the obviousness of this difference, and since appellants have provided no substantive response to this rejection, we are constrained on this record to sustain the examiner's provisional rejection of claims 1-27, 29-68 and 70-97 on the ground of obviousness-type double patenting.

We now consider the rejection of claims 1-3, 9-13, 16-27, 34, 36-44, 50-54, 57-68, 75 and 77-97 under 35 U.S.C. § 103. As a general proposition in an appeal involving a

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rejection under 35 U.S.C. § 103, an examiner is under a burden to make out a prima facie case of obviousness. If that burden is met, the burden of going forward then shifts to the applicant to overcome the prima facie case with argument and/or evidence. Obviousness is then determined on the basis of the evidence as a whole and the relative persuasiveness of the arguments. See In re Oetiker, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992); In re Hedges, 783 F.2d 1038, 1039, 228 USPQ 685, 686 (Fed. Cir. 1986); In re Piasecki, 745 F.2d 1468, 1472, 223 USPQ 785, 788 (Fed. Cir. 1984); and In re Rinehart, 531 F.2d 1048, 1052, 189 USPQ 143, 147 (CCPA 1976).

We now consider the rejection of claim 1 as unpatentable over Chu and Vassiliadis. Claims 11-13, 39, 42, 51, 52 and 80 are not separately argued and have been grouped with claim 1. The examiner has pointed out that Chu teaches an ALU which performs mixed arithmetic and logical operations on three inputs received at the ALU. The examiner indicates that Chu does not teach the claimed operations performed only on the first and second inputs and on the first and third inputs [answer, pages 4-6]. The examiner cites Vassiliadis to

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teach an ALU which performs mixed arithmetic and logical operations on any two inputs of a three input ALU. The examiner also explains why it would have been obvious to the artisan to replace the Chu ALU with the Vassiliadis ALU. In our view, the examiner has at least presented a prima facie case of the obviousness of claim 1. Therefore, we consider appellants' arguments and the relative persuasiveness of the arguments.

Appellants' first argument is that Chu does not teach the claimed ALU for performing the operations  $A \pm B$  and  $A \pm C$  as recited in claim 1. The examiner has acknowledged this deficiency in Chu which is why the reference was combined with Vassiliadis. Appellants argue that Vassiliadis also does not provide this teaching because Vassiliadis teaches that two operand ALU functions are achieved by forcing one input to zero [brief, page 7]. According to appellants, claim 1 recites that the ALU combinations are achieved by control of the function of the ALU and not by forcing one input to zero. Based on this argument, appellants assert that claim 1 is not suggested by the collective teachings of Chu and Vassiliadis.

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In our view, appellants' interpretation of claim 1 is not commensurate with the language of claim 1. Claim 1 does not require that the two operand functions be implemented in any specific manner. Claim 1 only recites that the ALU receive a control function input and that the ALU perform the operations  $A \pm B$  and  $A \pm C$ . The ALUs of Chu and Vassiliadis clearly receive an input function control signal, and Vassiliadis clearly performs the noted operations as pointed out by the examiner. Appellants are attempting to import their disclosed preferred embodiment into the claim which is not appropriate. Claims are given their broadest reasonable interpretation during prosecution before the Patent and Trademark Office.

Since we have determined that the examiner has presented a prima facie case for the obviousness of claim 1, and since appellants have not presented a compelling reason to find error in the examiner's case, we sustain the rejection of claim 1 and of claims 11-13, 39, 42, 51, 52 and 80 which are grouped therewith.

We now consider the rejection of claims 2 and 43 which are grouped together and of claims 3 and 44 which are grouped

together. Claim 2 depends from claim 1 and recites that the shifter performs a right shift or a left shift based on the digital state of a predetermined bit of the shift control signal. Claim 3 depends from claim 2 and recites that the predetermined bit is the most significant bit of the shift control signal. The examiner has provided a reasonable analysis as to why the shift control, as broadly recited in claims 2 and 3, would have been obvious to the artisan in view of the applied prior art. Appellants argue that Chu does not teach that a predetermined bit of a control bus should be used to control the shift direction because Chu uses a bit of the data buses to carry out this shift direction control. The examiner responds that it does not matter where the control signal comes from, and the artisan would have found it obvious to apply either a data signal or a control signal to the shift control input of the Chu shifter. We agree. Whatever input controls the direction and amount of shift in Chu can be considered as the claimed shift control input. The artisan would have found it obvious that any bit at the shift control input can be the directional control bit, including the most

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significant bit. Therefore, we sustain the rejection of claims 2, 3, 43 and 44.

We now consider the rejection of claims 9 and 50 which are grouped together. Claim 9 depends from claim 1 and recites that a plurality of data registers receives an input from the output of the ALU and an input from the output of the shifter. The examiner has provided a reasonable analysis as to why the presence of registers, as broadly recited in claim 9, would have been obvious to the artisan in view of the applied prior art. Appellants argue that Chu does not show such a register at the output of the shifter, but this argument fails to address the obviousness of broadly providing such a register. Appellants also argue that "claims 9 and 50 require storage of both the output of the arithmetic logic unit and the output of the shifter during the same operation. Neither Chu et al nor Vassiliadis et al show the claimed simultaneous storage of these two outputs in any mode" [brief, page 10]. We agree with the examiner that this argument of appellants is not commensurate in scope with the claimed invention. We find nothing in claim 9 which requires the simultaneous storage as argued by appellants. Since

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appellants' arguments are not persuasive of error by the examiner, we sustain the rejection of claims 9 and 50.

With respect to claims 10 and 51 which are grouped together, the examiner asserts that Chu teaches a one's constant source to supply a shifter [answer, page 7]. Appellants argue that insertion of 1's into the shifter of Chu does not make obvious the specific digital signal whose value is "0001" as recited in claim 10 [brief, page 9]. The examiner responds that Chu can provide a single bit of value "1" to the shifter which would meet the recitation of claim 10 [answer, page 14]. Appellants reply that their inputs to the shifter are so different from the Chu rotator that Chu does not make the claimed invention obvious [reply brief, pages 13-14].

When the scope of claim 10 is considered, we agree with the examiner that the broad recitation of applying a data input of value "0001" would have been obvious to the artisan in view of Chu's teaching of inserting 1's into the shifter 118. We are of the view that the artisan would have recognized the obviousness of making any number of the least significant bits "1" based upon the amount of shift or

rotation desired. Therefore, we sustain the rejection of claims 10 and 51.

With respect to claims 16 and 57 which are grouped together, the examiner relies on the mask of Chu to render the invention of these claims obvious [answer, page 7]. Appellants argue that Chu does not form the mask as recited in claim 16 [brief, pages 11-12]. We agree with appellants' argument with respect to these claims. The mask in Chu is used to modify one of the other two inputs to Chu's ALU, and is not used as the third operand input to an ALU. The examiner has not indicated why the mask in Chu would have been modified to correspond to the third multibit digital input signal when the Chu ALU is replaced by the Vassiliadis ALU. The examiner also has not explained why a specific mask value as recited in claim 16 cannot be patented. The examiner has simply stated that any mask value would have been obvious to the artisan. Although the examiner's conclusion may be correct in theory, it is not supported by any evidence on this record, and appellants have made a point of arguing the patentability of this specific feature. Since appellants have specifically argued the limitations of claim 16, and since the examiner's general

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conclusion of obviousness is not supported by the record, we do not sustain the Section 103 rejection of claims 16 and 57.

Claims 19, 22 and 25 recite a specific mask signal in a manner similar to claim 16. The examiner's rejection of these claims is supported in the same manner as the rejection of claim 16. Therefore, we also do not sustain the Section 103 rejection of these claims for the same reasons just discussed. Claims 60, 63 and 66 are grouped with these claims. Claims 17, 18, 20, 21, 23, 24, 26 and 27 depend from one of claims 16, 19, 22 and 25 and incorporate the limitations just discussed. Claims 58, 59, 61, 62, 64, 65, 67 and 68 depend from one of claims 57, 60, 63 and 66 and incorporate the limitations just discussed. Accordingly, we do not sustain the Section 103 rejection of any of these claims.

Claims 34 and 36 recite that the mask is formed from a repetition of or replication of a pattern. The examiner argues that the Chu mask generator meets this claim recitation while appellants argue that the insertion of 1's in Chu does not perform the claimed repeated digital pattern. We agree with appellants that the examiner has not demonstrated how the

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Chu mask generator would meet the claim limitations when the Chu ALU is replaced with the Vassiliadis ALU. Claims 75 and 77 are grouped with these claims. Claims 37 and 78 depend from claims 36 and 77, respectively. Thus, we do not sustain the Section 103 rejection of any of these claims.

With respect to claims 38, 40 and 41, the examiner has grouped these claims with the rejection of claims 34, 36 and 37, but the examiner has not specifically addressed the features of these claims. Appellants argue that the examiner has failed to point to any teaching or suggestion in the applied prior art which renders the limitations of these claims obvious. We agree. The examiner has failed to establish a prima facie case of obviousness for the invention as recited in claims 38, 40 and 41. Claims 79, 81 and 82 are grouped with these claims. Therefore, we do not sustain the Section 103 rejection of these claims.

We now consider the rejection of claims 83-97 as unpatentable over the teachings of Chu, Vassiliadis and Pfeiffer. Although appellants nominally indicated that these claims were grouped with claim 42, this rejection includes the additionally applied Pfeiffer reference so that the nominal

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grouping is technically not applicable. The only argument offered by appellants for the patentability of these claims is that they incorporate the limitations of claim 42 by dependence. Since we have previously determined that the rejection of claim 42 would be sustained, and since appellants have offered no compelling reason for the patentability of claims 83-97, we also sustain the Section 103 rejection of these claims.

In summary, the provisional rejection of claims 1-27, 29-68 and 70-97 on the ground of obviousness-type double patenting is sustained. The rejection of claims 1-3, 9-13, 16-27, 34, 36-44, 50-54, 57-68, 75 and 77-97 under 35 U.S.C. § 103 is sustained with respect to claims 1-3, 9-13, 39, 42-44, 50-54, 80 and 83-97 but is reversed with respect to claims 16-27, 34, 36-38, 40, 41, 57-68, 75, 77-79, 81 and 82. Accordingly, the decision of the examiner rejecting claims 1-27, 29-68 and 70-97 is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED

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Administrative Patent Judge	)	
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