

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today  
(1) was not written for publication in a law journal and  
(2) is not binding precedent of the Board.

Paper No. 13

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES  
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Ex parte GARY A. FRAZIER  
\_\_\_\_\_

Appeal No. 97-0707  
Application 08/001,474<sup>1</sup>  
\_\_\_\_\_

ON BRIEF  
\_\_\_\_\_

Before HAIRSTON, BARRETT and TORCZON, Administrative Patent  
Judges.

HAIRSTON, Administrative Patent Judge.

DECISION ON APPEAL

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<sup>1</sup> Application for patent filed January 7, 1993.

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This is an appeal from the final rejection of claims 1 through 6 and 8 through 23. In an Amendment After Final<sup>2</sup> (paper number 7), claims 1, 5, 8, 9, 13, 15, 17, 20, 21 and 23 were amended, and claims 2 through 4, 14, 18, 19 and 22 were canceled. Accordingly, claims 1, 5, 6, 8 through 13, 15 through 17, 20, 21 and 23 remain before us on appeal.

The disclosed invention relates to a method and device for storing and recalling address associative information in an address space.

Claims 1 and 17 are illustrative of the claimed invention, and they read as follows:

1. A device for storing and recalling information, comprising:

an address space, defined by a plurality of memory chips, for holding address associative information;

a plurality of key addresses within said address space;

a radius of capture corresponding to each key address, said key addresses partitioning said address space such that a hypersphere defined by said radius of capture of each key address does not overlap any other hypersphere within each memory chip in order to allow information within said address space to be associated with at most one key address;

a dedicated address decoder corresponding to each key address for receiving an address over an address signal path in

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<sup>2</sup> As indicated in the Advisory Action (paper number 8), the amendment had the effect of overcoming the rejection of claim 9 under the fourth paragraph of 35 U.S.C. § 112.

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order to activate said key address; and

a memory element corresponding to each key address for storing said address associative information; wherein each memory element includes a plurality of multiple bit binary counters, each multiple bit binary counter corresponding to a separate bit position of information stored at each key address.

17. A method of storing and recalling information, comprising the steps of:

defining an address space within a memory chip;

randomly generating key addresses within said address space;

selecting a radius of capture for each key address;

partitioning said address space such that a hypersphere defined by said radius of capture of any key address does not overlap a hypersphere defined by said radius of capture of any other key address;

receiving address associative information;

activating a key address having said address associative information, said address associative information activating at most one key address within said memory chip;

storing said address associative information at said activated key address in response to a write command;

transmitting an output from said activated key address in response to a read command, said output having bit positions corresponding to said address associative information; and

summing said bit positions of said output for each activated key address on multiple memory chips to determine a result for each bit position.



With respect to claims 1 and 13, appellant argues that Jaeckel does not teach a "dedicated address decoder corresponding to each key address," and a "memory element that includes . . . multiple bit binary counters with each counter corresponding to a separate bit position of information stored at each key address" (Brief, pages 4 and 6). Figure 1 of Jaeckel shows an address decoder 19 at each hard memory (i.e., key address) location. A plurality of multiple bit binary counters C1 through CM are at each hard memory location, and each multiple bit binary counter corresponds to a separate bit position of information stored at each hard memory location/key address. With respect to the address decoders, Jaeckel explains that: "[f]or each implemented memory location, which will be called a 'hard memory location', there is an address decoder that determines whether or not to activate that location during a read or a write operation" (column 1, lines 48 through 51); "[t]he function of the address decoder at each hard memory location is to compute the Hamming distance between the given read or write address and the address of the hard memory location" (column 2, lines 12 through 15); "[o]ne way to implement the present invention relating to a Sparse Distributed Memory is to implement the system by having an address decoder for each hard memory location" (column 11, lines

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52 through 55); and "the address decoder for each hard memory location has ten inputs," and "if all ten match, the location is activated" (column 13, lines 24 through 31). With respect to the multiple bit binary counters, Jaeckel explains that: "[w]hen a data word (a binary vector) is written to the memory at address  $x$ , the word is added to the counters at each of the activated hard memory locations" (column 2, lines 18 through 20); "[a] computer memory system according to the invention includes a plurality of hard memory locations in number equal to  $K$ , where  $K$  is an integer greater than one, each hard memory location comprising  $M$  counters,  $C_1$  through  $C_M$ , where  $M$  is an integer greater than zero" (column 4, lines 31 through 36); and "[f]or each of the hard memory locations, there is a set of  $M$  counters, . . . such as  $C_1$  through  $C_M$  which are associated with hard memory location 24" (column 12, lines 26 through 30).

In view of the foregoing, it is evident that Jaeckel discloses all of the contested limitations of claims 1 and 13. Thus, the 35 U.S.C. § 102(e) rejection of claims 1 and 13 is sustained.

The 35 U.S.C. § 102(e) rejection of claim 5 is sustained because "when performing a write operation" in Jaeckel, "[i]n the case where the data is in the form of bits, the processor element

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15 increments or decrements each of the counters, according to the value of the corresponding bit in the data" (column 12, lines 39 through 55). To be more specific, the counters in Jaeckel are incremented when storing a binary one, and decremented when storing a binary zero (column 2, lines 22 through 24).

The 35 U.S.C. § 102(e) rejection of claims 6 and 8 is sustained because we agree with the examiner (Answer, page 7) that Jaeckel discloses (column 12, lines 19 through 68) that "the multiple bit binary counters receive data from a data signal path equal in width to a number of multiple bit binary counters (see figure 1, items 23 and 12 and C1-Cm) and output for each bit position of information in response to a read command and activation of the hard memory location (see also figure 1)."

The 35 U.S.C. § 102(e) rejection of claim 9 is reversed because Jaeckel does not teach "partitioning said address space such that said hyperspheres corresponding to each key address do not overlap<sup>4</sup> a hypersphere of any other key address." The 35 U.S.C. § 102(e) rejection of claims 10 through 12 is reversed because these claims depend from claim 9.

The 35 U.S.C. § 102(e) rejection of claims 15 and 16 is

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<sup>4</sup>As indicated supra, appellant did not contest this limitation in the arguments made for claims 1 and 13. An argument not made is an argument that is waived.

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sustained because we agree with the examiner (Answer, page 7) that "Jaeckel further discloses summing circuitry . . . and threshold circuitry - see figure 1 items 25, 27 and 29."

With respect to method claims 17 and 23, we agree with the examiner (Answer, page 7) that these claims "are the method claims that correspond to the operation detailed above for claims 1, 5-6, 8 . . . 13 and 15-16 and the rationale of Jaeckel's anticipation of these apparatus claims can be applied to the corresponding method claims." For all of the reasons expressed supra in connection with claims 1, 5, 6, 8, 13, 15 and 16, the 35 U.S.C. § 102(e) rejection of claims 17 and 23 is sustained.

Claims 20 and 21 are directed to the lack of "overlapping hyperspheres" or to the elimination of "overlaps of the hyperspheres," respectively. The 35 U.S.C. § 102(e) rejection of these claims is reversed because Jaeckel is silent concerning such teachings.

Although claim 11 is an originally filed claim, the specification does not provide any explanation concerning how a tree adder<sup>5</sup> can add outputs in "logarithm time units." We can speculate as to how this would be done by a tree adder, but it is

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<sup>5</sup>As indicated on page 359 of the attached publication by Rogers, optimization of processes in sparse distributed memory (SDM) is achieved by use of a tree adder.

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not our duty to explain the invention where appellant has failed to do so. More importantly, we do not know the metes and bounds of the claim in view of the questioned language. If the prior art rejection of this claim had not been reversed because of its dependency from claim 9, then we would have had to resort to speculation and assumptions to apply the prior art to the limitations of the claim. See In re Steele, 305 F.2d 859, 862-63, 134 USPQ 292, 295 (CCPA 1962).

REJECTIONS UNDER 37 CFR § 1.196(b)

Pursuant to the provisions of 37 CFR § 1.196(b), we hereby enter the following new grounds of rejection:

Claim 11 is rejected under the first and second paragraphs of 35 U.S.C. § 112. As indicated supra, the originally filed application disclosure does not provide an enabling disclosure for a tree adder that can add outputs in "logarithm time units." In view of the lack of any explanation in the application disclosure for such an addition operation, the claim is indefinite because it fails to set out and circumscribe a particular area with a reasonable degree of precision and particularity when read in light of the application disclosure. See In re Moore, 439 F.2d 1232, 1235, 169 USPQ 236, 238 (CCPA 1971).

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DECISION

The decision of the examiner rejecting claims 1, 5, 6, 8 through 13, 15 through 17, 20, 21 and 23 under 35 U.S.C. § 102(e) is affirmed as to claims 1, 5, 6, 8, 13, 15 through 17 and 23, and is reversed as to claims 9 through 12, 20 and 21. Accordingly, the decision of the examiner is affirmed-in-part.

In addition to affirming the examiner's rejection of claims 1, 5, 6, 8, 13, 15 through 17 and 23, this decision contains new grounds of rejection of claim 11 pursuant to 37 CFR § 1.196(b) (amended effective Dec. 1, 1997, by final rule notice, 62 Fed. Reg. 53,131, 53,197 (Oct. 10, 1997), 1203 Off. Gaz. Pat. & Trademark Office 63, 122 (Oct. 21, 1997)). 37 CFR § 1.196(b) provides, "A new ground of rejection shall not be considered final for purposes of judicial review."

Regarding any affirmed rejection 37 CFR § 1.197(b) provides:

(b) Appellant may file a single request for rehearing within two months from the date of the original decision . . . .

37 CFR § 1.196(b) **also provides that the appellant, WITHIN TWO MONTHS FROM THE DATE OF THE DECISION, must exercise one of the following two options with respect to the new grounds of rejection to avoid termination of proceedings (37 CFR § 1.197(c)) as to the rejected claims:**

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(1) Submit an appropriate amendment of the claims so rejected or a showing of facts relating to the claims so rejected, or both, and have the matter reconsidered by the examiner, in which event the application will be remanded to the examiner . . . .

(2) Request that the application be reheard under § 1.197(b) by the Board of Patent Appeals and Interferences upon the same record . . . .

Should the appellant elect to prosecute further before the Primary Examiner pursuant to 37 CFR § 1.196(b)(1), in order to preserve the right to seek review under 35 U.S.C. §§ 141 or 145 with respect to the affirmed rejection, the effective date of the affirmance is deferred until conclusion of the prosecution before the examiner unless, as a mere incident to the limited prosecution, the affirmed rejection is overcome.

If the appellant elects prosecution before the examiner and this does not result in allowance of the application, abandonment or a second appeal, this case should be returned to the Board of Patent Appeals and Interferences for final action on the affirmed rejection, including any timely request for rehearing thereof.

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No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED-IN-PART  
37 CFR § 1.196(b)

KENNETH W. HAIRSTON	)	
Administrative Patent Judge	)	
	)	
	)	
LEE E. BARRETT	)	BOARD OF PATENT
Administrative Patent Judge	)	APPEALS AND
	)	INTERFERENCES
	)	
	)	
RICHARD TORCZON	)	
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