

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 27

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES

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Ex parte ROBERT P. COLWELL, MICHAEL A. FETTERMAN, GLENN J.  
HINTON, ROBERT W. MARTELL, and DAVID B. PAPWORTH

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Appeal No. 97-0266  
Application No. 08/176,370<sup>1</sup>

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ON BRIEF

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Before HAIRSTON, KRASS, and GROSS, Administrative Patent Judges.  
GROSS, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the examiner's final rejection of claims 1 and 3 through 43, which are all of the claims pending in this application. In the Examiner's Answer, the examiner objected to claims 18, 19, 32 through 34, and 41 through 43 as being dependent upon rejected base claims. With the Reply Brief filed on October 2, 1995, claims 18, 19, 32

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<sup>1</sup> Application for patent filed December 30, 1993.

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through 34, and 41 through 43 were amended to overcome the objection. In the Supplemental Examiner's Answer, mailed October 3, 1995, the examiner allowed claims 18, 19, 32 through 34, and 41 through 43. Accordingly, the claims which remain before us on appeal are claims 1, 3 through 17, 20 through 31, and 35 through 40.

The appellants' invention relates to achieving maximum throughput of dependent operations in a pipelined microprocessor. More specifically, a designation location designator of a result of one instruction is compared to stored source operand location designators of dependent instructions. When a match is found, a dependent instruction is dispatched for execution, thereby maximizing the efficiency in which the processor determines the availability of the source operands and provides them to the execution unit executing the dependent instruction. Claim 1 is illustrative of the claimed invention, and it reads as follows:

1. In a processor having at least one execution unit for executing a plurality of instructions to thereby generate execution results, each instruction specifying an opcode and being associated with at least one source operand location designator indicating a storage location of a source operand

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of said each instruction in a storage buffer, each instruction further associated with a destination location designator indicating a storage location in the storage buffer of the result of the execution of said each instruction, wherein each of at least one dependent instruction of the plurality of instructions is dependent upon at least one source instruction of the plurality of instructions such that at least one source operand location designator of the at least one dependent instruction is identical to a corresponding destination location designator of the at least one source instruction, the at least one source operand location designator of the at least one dependent

instruction being stored in a memory device of the processor, the memory device including a content addressable memory for storing the source operand location designators of the at least one dependent instruction as tags of the content addressable memory, a method for determining the availability of a source operand of a dependent instruction for dispatch of the dependent instruction to an execution unit, the method comprising the steps of:

receiving a first destination location designator of a first result, the first result being the result of the execution of a first source instruction by a first execution unit;

determining a first condition, the first condition being whether the received first destination location designator is identical to any of the stored source operand location designators of the at least one dependent instruction, each dependent instruction that satisfies the first condition thereby being a dependent instruction that will have at least one source operand available for dispatch of the dependent instruction to an execution unit, wherein said determining step comprises the step of:

associatively comparing the first destination location designator with the stored source operand location designators of the dependent instructions to determine which of the

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dependent instructions are dependent instructions satisfying the first condition.

The prior art references of record relied upon by the examiner in rejecting the appealed claims are:

Murray et al. (Murray)	5,142,633	Aug. 25, 1992
Tran	5,345,569	Sep. 06, 1994

(filed Sep. 20, 1991)

Val Popescu, et al., "The Metaflow Architecture," IEEE Micro (June 1991), pp. 10-13 and 63-73. (Popescu)

Claims 1, 3 through 17, 20 through 31, and 35 through 40 stand rejected under 35 U.S.C. § 103 as being unpatentable over Tran in view of Murray and Popescu.<sup>2</sup>

Reference is made to the Examiner's Answer (Paper No. 17, mailed July 25, 1995) and the Supplemental Examiner's Answer (Paper No. 19, mailed October 13, 1995) for the examiner's complete reasoning in support of the rejections, and to the appellants' Brief (Paper No. 21, filed October 2, 1995) and

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<sup>2</sup> Although the Examiner's Answer includes the statement of the rejection, the statement is not followed by an explanation nor a reference to a prior paper which includes a complete statement and explanation of the rejection. However, we believe we understand the examiner's position. Further, as appellants have discussed all claimed limitations at length with respect to the three applied references, appellants clearly have had an opportunity to respond to the rejection, such that there has been no lack of due process.

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Reply Brief (Paper No. 22, filed October 2, 1995) for the appellants' arguments thereagainst.

OPINION

We have carefully considered the claims, the applied prior art references, and the respective positions articulated by the appellants and the examiner. As a consequence of our review, we will reverse the obviousness rejection of claims 1, 3 through 17, 20 through 31, and 35 through 40.

Appellants make two arguments that are applicable to all of the claims. First, appellants assert (Brief, page 7) that

Tran utilizes the term "dispatch" to connote an instruction being released from a decoder (Tran also describes this as being "issued," see column 5, line 29) and sent to a queuing device for later execution. The present invention utilizes the term "dispatch" to connote an instruction being released from a queuing device for immediate execution.

In response, the examiner refers to column 1, lines 18-23, of Tran, which states that the instruction is dispatched to the reservation station, which "may check the results bus from the functional units for data returning to the reorder buffer and on detection of the appropriate tag, can directly receive the result for immediate processing." The examiner concludes that

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"[t]his statement in Tran clearly states that an instruction is 'dispatched' to the functional unit for immediate processing."

The portion of Tran relied upon by the examiner (particularly column 1, lines 18-19) refers to "the dispatched instruction to the reservation station." On the other hand, claim 1 reads, "dispatch of the dependent instruction to an execution unit" and claims 20 and 35 (the only other independent claims) read, "at least one row is ready for dispatch to an execution unit." Therefore, Tran clearly uses the term "dispatch" to connote sending to the reservation station, whereas the claims employ the term for sending to an execution unit.

However, Tran's different usage of the term "dispatch" does not necessarily mean that Tran fails to perform appellants' dispatching step. In fact, Tran states (column 2, lines 44-46) that "instructions are either being executed or waiting in a reservation station to be executed." Thus, Tran implies that the instructions are sent to the execution units

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for immediate execution, even though Tran does not use the term "dispatch" in that particular context. Appellants focus only on the particular language used. Nowhere on pages 7-9 of the Brief do appellants discuss whether the instructions in Tran are sent from the reservation station (where they are queued after all dependencies are reconciled (column 2, lines 66-68)) to the execution units for immediate execution, as in appellants' invention. Accordingly, we cannot reverse the rejection based on the different application of the term "dispatch."

On the other hand, for the second argument that pertains to all of the claims, appellants state (Brief, page 9) that

[t]he Tran system includes a compare-hit circuit (Figure 2) for generating a compare-hit signal in response to a match of a respective source indicator in the next-to-be-dispatched (e.g., issued) instruction with the destination indicator of an earlier stored instruction within the storage device (ROB 22). (underlining in original)

Claim 1, though, requires a comparison between "stored source operand location designators" and a "received first destination location designator." Similarly, claims 20 and 35

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(the only other independent claims) require "a match between the received first destination location designator and a stored source operand location designator." In other words, whereas Tran stores the destination indicators and compares them with a new source indicator, the claims call for storing the source indicators and comparing them to newly received destination indicators.

The examiner responds (Answer, page 5) by pointing to portions of columns 5 and 6 of Tran to show that Tran teaches "matching information from the output of the execution unit (destination indicator) with the source indicator stored in the reservation station for immediate execution by the functional unit." Within the sections noted by the examiner, Tran defines source address information as "identif[ying] an address in register 24 (see FIG. 1) at which information required for execution of an instruction (such as operand) is stored" (column 5, lines 55-58) and destination information as "identif[ying] an address within register file 24 at which results from execution of an instruction is to be stored after execution of the respective instruction" (column 5, lines 59-63). However,

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whether the source or destination operand designator is used before or after it is stored is not clear from these definitions. On the other hand, Tran indicates (column 5, lines 12-16) that "[if] a match occurs between the source operand and the previous-stored destination operand in reorder buffer 22 and the data is valid, then reorder buffer 22 will supply the data to an appropriate functional unit" (underlining added for emphasis). Thus, as pointed out by appellants, Tran stores the destination operands in the reorder buffer and then compares them to source operands, contrary to the claimed limitation of storing only the source operands.

The examiner further mentions (Answer, page 5) that "Popescu shows . . . a bypass path to permit the result of an execution (destination indicator) on one clock cycle as an operand (source indicator) on the next cycle." We agree that Popescu uses such a bypass path, and that the bypass path, viewed in a vacuum, would meet the claimed limitation. However, the examiner has not even stated that it would have been obvious to modify Tran. Consequently, the examiner's reason for presenting Popescu is unclear. To support the

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legal conclusion of obviousness, the examiner is required to provide a reason why one having ordinary skill in the pertinent art would have been led to modify the prior art or to combine prior art references to arrive at the claimed invention. Such reason must stem from some teaching, suggestion or implication in the prior art as a whole or knowledge generally available to one having ordinary skill in the art. Uniroyal, Inc. v. Rudkin-Wiley, 837 F.2d 1044, 1052, 5 USPQ2d 1434, 1438 (Fed. Cir.), cert. denied, 488 U.S. 825 (1988); Ashland Oil, Inc. v. Delta Resins & Refractories, Inc., 776 F.2d 281, 293, 227 USPQ 657, 664 (Fed. Cir. 1985), cert. denied, 475 U.S. 1017 (1986); ACS Hospital Systems, Inc. v. Montefiore Hospital, 732 F.2d 1572, 1577, 221 USPQ 929, 933 (Fed. Cir. 1984). Here the examiner has pointed to nothing that would indicate to one of ordinary skill in the art how or why to modify Tran to include such a bypass path. Accordingly, we cannot sustain the rejection.

Appellants have presented numerous additional arguments pertaining to individual claims or small groups of claims. For example, appellants contend that Murray fails to disclose

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a content addressable memory, for claims 1 and 16 (Brief, page 13), that the combination of references fails to suggest "setting a source valid bit corresponding to the source operand, thereby indicating that source operand is available" once the first condition is met, as recited in claim 4 (Brief, page 15), and that the cited art fails to teach that the two claimed source instructions are executed within the same clock cycle of the processor, for claim 6 (Brief, page 16). However, since we have found a defect in the rejection that is applicable to all of the claims, we will not address individual arguments for each of the proposed eighteen groups remaining after the examiner's allowance of claims 18, 19, 32 through 34, and 41 through 43.

CONCLUSION

The decision of the examiner rejecting claims 1, 3 through 17, 20 through 31, and 35 through 40 under 35 U.S.C. § 103 is reversed.

REVERSED

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KENNETH W. HAIRSTON	)	
Administrative Patent Judge	)	
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	)	BOARD OF PATENT
ERROL A. KRASS	)	APPEALS
Administrative Patent Judge	)	AND
	)	INTERFERENCES
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ANITA PELLMAN GROSS	)	
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