

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today
(1) was not written for publication in a law journal and
(2) is not binding precedent of the Board.

Paper No. 35

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte CARL K. WAKELAND
and
JOHN M. PRICKETT

Appeal No. 96-4169
Application 08/378,066¹

ON BRIEF

Before JERRY SMITH, FLEMING and CARMICHAEL, **Administrative
Patent Judges**.

¹ Application for patent filed January 25, 1995. According to Appellants, the application is a continuation of Application 08/232,320, filed April 25, 1994, abandoned; which is a continuation of Application 07/648,113, filed January 31, 1991, abandoned.

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FLEMING, *Administrative Patent Judge*.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 1 through 19, 24 and 25, all of the claims pending in the present application. Claims 20 through 23 are withdrawn from consideration.

The invention relates to a dual path computer control system for regulating the operation of a peripheral device associated with a computer system. Appellants disclose on page 8 of the specification that Figure 1 is a block diagram of a computer system having a dual path control system constructed in accordance with the teachings of the present invention. Furthermore, Appellants disclose that Figure 2 is a schematic diagram illustrating the interconnections between the host computer and the independent control circuit of Figure 1 as well as the interconnections between the components of the independent control circuit. On page 9 of the

specification, Appellants disclose that Figure 1 shows the independent control circuit 10 which is connected in parallel with host computer 12, thereby enabling the two to operate simultaneously. On page 11 of the specification, Appellants disclose that Figure 2 shows the dual path computer control system in greater detail. In particular,

Figure 2 shows that the independent control circuit 10 includes a state machine 32 which enables the independent control circuit 10 and the host computer 12 to operate simultaneously.

Independent claim 1 is reproduced as follows:

1. A computer system comprising:

a host computer;

an independent control circuit;

a peripheral device having inputs electrically connected to an output of said host computer and to an output of said independent control circuit, respectively;

a single input means for generating control signals to be input to said peripheral device and data and control signals to be input to said host computer;

means having an input connected to an output of said single input means and outputs connected to said independent

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control circuit and said host computer, respectively, and responsive to receipt of signals from said single input means for directing said peripheral device control signals to said independent control circuit for processing and for directing said host computer data and control signals only to said host computer for processing;

means connected between said independent control circuit and said peripheral device for transmitting control signals produced by said processing of said peripheral device control signals by said independent control circuit to said peripheral device; and

wherein said independent control circuit is not subject to control by said host computer.

The Examiner relies on the following references:

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|------------------------|-----------|---------------|
| Galbraith | 3,936,600 | Feb. 3, 1976 |
| Niimi | 4,184,400 | Jan. 22, 1980 |
| Kaiser et al. (Kaiser) | 4,942,606 | July 17, 1990 |
| DeLaTorre | 5,088,378 | Feb. 18, 1992 |
| Raasch et al. (Raasch) | 5,237,692 | Aug. 17, 1993 |

Claims 1 through 17, 19, 24 and 25 stand rejected under 35 U.S.C. § 103 as being unpatentable over Raasch in view of Galbraith. Claims 9 through 17, 19 and 25 stand rejected under 35 U.S.C. § 103 as being unpatentable over Raasch in view of Galbraith, further in view of Kaiser. Claim 18 stands rejected under 35 U.S.C. § 103 as being unpatentable over Raasch in view of Galbraith and Kaiser, further in view of Niimi.

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Rather than reiterate the arguments of Appellants and the Examiner, reference is made to the brief² and answer for the respective details thereof.

OPINION

We will not sustain the rejection of claims 1 through 19, 24 and 25 under 35 U.S.C. § 103.

The Examiner has failed to set forth a ***prima facie*** case. It is the burden of the Examiner to establish why one having ordinary skill in the art would have been led to the claimed invention by the express teachings or suggestions found in the prior art, or by implications contained in such teachings or suggestions. ***In re Sernaker***, 702 F.2d 989, 995, 217 USPQ 1, 6 (Fed. Cir. 1983). "Additionally, when determining obviousness, the claimed invention should be

² We note that Appellants' appendix found in the brief incorrectly sets forth claim 14. As amended by Amendment B, the words "peripheral device controlling" are deleted.

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considered as a whole; there is no legally recognizable 'heart' of the invention." ***Para-Ordnance Mfg. v. SGS Importers Int'l, Inc.***, 73 F.3d 1085, 1087, 37 USPQ2d 1237, 1239 (Fed. Cir. 1995), ***cert. denied***, 117 S.Ct. 80 (1996) ***citing W. L. Gore & Assoc., Inc. v. Garlock, Inc.***, 721 F.2d 1540, 1548, 220 USPQ 303, 309 (Fed. Cir. 1983), ***cert. denied***, 469 U.S. 851 (1984).

Claims 1 through 17, 19, 24 and 25 stand rejected under 35 U.S.C. § 103 as being unpatentable over Raasch in view of Galbraith. On page 5 of the brief, Appellants argue that neither Raasch nor Galbraith teaches or suggests modifying the Raasch system to allow direct control of the peripheral devices by the keyboard. Appellants further argue that the Examiner failed to clearly state exactly how Galbraith's teaching would be used to modify the Raasch system.

The Federal Circuit states that "[t]he mere fact that the prior art may be modified in the manner suggested by the

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Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." **In re Fritch**, 972 F.2d 1260, 1266 n.14, 23 USPQ2d 1780, 1783-84 n.14 (Fed. Cir. 1992), **citing In re Gordon**, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984). "Obviousness may not be established using hindsight or in view of the teachings or suggestions of the inventor." **Para-Ordnance Mfg.**, 73 F.3d at 1087, 37 USPQ2d at 1239, **citing W. L. Gore**, 721 F.2d at 1551, 1553, 220 USPQ at 311, 312-313.

Upon our review of the references relied upon by the Examiner, we fail to find any suggestion or reason to modify the Raasch system so as to allow the host computer not to control the independent control circuit. In column 1 of Raasch, lines 5-14, Raasch teaches that their invention relates to facilitating control within Industrial Standard Architecture (ISA). Specifically, the invention involves a peripheral controller which emulates the functions of conventional peripheral controllers and interrupt controllers within the peripheral controller which generates internal interrupts in response to a number of devices connected to the

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ISA computer. Raasch teaches that the peripheral controller enters a low power mode of

operation while it awaits an interrupt from various devices, rather than actively polling these devices to determine which device or devices need service. In column 1, lines 53-58, Raasch teaches that in laptop computers in which power consumption is critical, it is important to consider any way to reduce the power consumption. In column 2, lines 6-14, Raasch discloses that conventional designs provide that the peripheral controller continuously polls various devices to determine if any data transferred from the keyboard is required. Power is unnecessarily consumed in these active polling processes. In column 2, lines 50-57, Raasch teaches that they have solved this unnecessary power consumption by utilizing memory mapped address decode architecture. In column 2, line 63, through column 3, line 4, Raasch discloses that their invention provides an interrupt controller for an interrupt driven peripheral controller for use in a host Industrial Standard Architecture compatible computer system,

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wherein the peripheral controller has a core microprocessor configured to receive at least one interrupt and capable of operating in a low power mode while awaiting interrupts, and also has addressable memory space.

On the other hand, Galbraith is concerned with a completely different problem. In column 1, lines 5-50, Galbraith

teaches that the problem in the prior art is that electronic data processing equipment designed to operate with information data in parallel is generally not compatible with electronic data processing equipment designed to transmit and receive information data serially. In column 1, lines 52-63, Galbraith teaches that their invention overcomes this problem by providing an electronic asynchronous buffered interface circuit between the central data processing unit, which communicates in serially coded ASCII, and a data terminal comprising a printer and keyboard both of which are designed to operate with information data in parallel. In column 2, lines 39-54, Galbraith refers to Figure 1 which shows a

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central data processing unit 10 and an interface 12 interconnected by a transmission line 14. The interface 12 is connected to a printer 16 and a keyboard 18 by means of a transmission lines 20 and 22, respectively. Electronic data information exchanged between the central processing unit 10 and the interface 12 through the transmission line 14 is a standard serial transmitted ASCII data format. The electronic data information that is transferred from the keyboard 18 to the interface 12 and from the interface 12 to printer 16 through the data transmission lines 22 and 20, respectively, are in parallel.

Galbraith teaches in column 2, lines 55-58, that Figure 2 shows the architecture of the data terminal of the invention and indicates the flow of data and control signals between the various components which are represented schematically. In column 3, lines 9-21, Galbraith teaches that interface 12 shown in Figure 2 is capable of operating in a local mode and an on-line mode. Control means 42 acts as a switch to

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connect the keyboard and printer directly, a local mode, or to connect the keyboard via the host computer to the printer 16, an on-line mode.

Thus, Raasch is concerned with an interrupt driven peripheral controller for use in an Industry Standard Architecture compatible computer in order to minimize power consumption. Galbraith, on the other hand, is concerned with an asynchronous buffered interface for interconnecting a data processing apparatus adapted to communicate in serially coded ASCII data format and a terminal comprising the printer and a keyboard, both of which are adapted for data communication in parallel format. We note that the Examiner has not explained how Raasch's interrupt controller is to be modified by Galbraith's keyboard-printer terminal interface. We fail to find any reason

or suggestion to use the teaching of Galbraith in the Raasch interrupt controller. Therefore, we will not sustain the Examiner's rejection of claims 1 through 17, 19, 24 and 25.

Claims 9 through 17, 19 and 25 stand rejected under

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35 U.S.C. § 103 as being unpatentable over Raasch, Galbraith, and in view of Kaiser. We note that the Examiner is using the same reasoning as above to combine Raasch and Galbraith. We will not sustain this rejection as well for the same reasons as above in that we find no reason or suggestion to modify Raasch with the Galbraith teachings.

We have not sustained the rejection of claims 1 through 19, 24 and 25 under 35 U.S.C. § 103. Accordingly, the Examiner's decision is reversed.

REVERSED

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| | JERRY SMITH |) | |
| | Administrative Patent Judge |) | |
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| PATENT | |) | |
| | MICHAEL R. FLEMING |) | APPEALS AND |
| | Administrative Patent Judge |) | |
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| | JAMES T. CARMICHAEL |) | |
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MRF:psb

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