

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today
and (1) was not written for publication in a law journal
and (2) is not binding precedent of the Board.

Paper No. 50

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte ANTHONY Y. WONG, ANNA TAM
and DANIEL WONG

Appeal No. 1996-4050
Application 08/410,375¹

ON BRIEF

Before THOMAS, HAIRSTON, and HECKER, Administrative Patent

¹ Application for patent filed March 27, 1995. According to appellants, this application is a continuation of 08/014,084, filed February 04, 1993, which is a continuation of 07/754,201 filed August 19, 1991, which is a continuation of 07/523,445 filed May 14, 1990.

Appeal No. 1996-4050
Application No. 08/410,375

Judges.

HECKER, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 1 through 20, all of the claims pending in the application.

Appellants' invention relates to a logic array integrated circuit structure including complementary MOS field effect transistors (P-channel and N-channel) and bipolar transistors, referred to as a BiCMOS logic array. This logic array structure is more compact and flexible than the prior art in conserving layout patterns for the conducting lines which interconnect to transistor devices. In particular, as shown in Figure 3, a repeating cell structure has three vertical regions or columns with a first columnar region designated N-CHANNEL, a second columnar region designated P-CHANNEL and a third columnar region designated BIPOLAR. The transistors in the N-channel columnar region form eight NMOS transistors in a P-well region of the substrate. The transistors in the P-channel columnar region form eight PMOS transistors in a N-

Appeal No. 1996-4050
Application No. 08/410,375

well region of the substrate. And, two bipolar transistors
are formed in the bipolar column. Representative

claim 10 is reproduced as follows:

10. In a repeating BiCMOS logic gate array integrated circuit structure in a semiconductor substrate, said substrate having first and second columnar regions, said first columnar region of a first conductivity type and said second columnar region of a second conductivity type, each of said columnar regions having active regions with gate electrodes vertically separating said active regions into source/drain regions, the improvement comprising:

a third columnar region of said first conductivity type, said third columnar region having a collector, base and emitter region of a first bipolar transistor and a collector, emitter and base region of a second bipolar transistor, said regions aligned vertically in said third columnar region and aligned with respect to said gate electrodes and said source/drain regions of said first and second CMOS regions;

whereby a macrocell can be formed from said first, second and third columnar regions with a grid of vertical and horizontal routing tracks over said columnar regions, no matter what order said columnar regions are located horizontally adjacent to each other.

No references are relied upon by the Examiner.

Claims 1 through 20 stand rejected under 35 U.S.C. § 112, first paragraph, as not supported by an enabling disclosure.

Rather than repeat the arguments of Appellants or the Examiner, we make reference to the brief, reply brief and the answer for the respective details thereof.

Appeal No. 1996-4050
Application No. 08/410,375

OPINION

We have carefully considered the subject matter on appeal, i.e., the enablement of the disclosure. It is our view that the disclosure in this application is enabling in a manner which

complies the requirements of 35 U.S.C. § 112, and we will not sustain the rejection of the claims on this ground.

The specification of a patent must teach those skilled in the art how to make and use the full scope of the claimed invention without undue experimentation.

The Examiner states:

The specification is objected to under 35 U.S.C. § 112, first paragraph, as non-enabling to make and use the recited arrangements with "columnar regions" and "taps" **for the bipolar transistors**, as discussed previously and above.

Claims 1-20 are rejected under 35 U.S.C. § 112, first paragraph, as not supported by [an] enabling disclosure to make and use, as described previously and above. (Emphasis added.) (Answer-page 4.)

Attempts to equate the recited "columnar regions" with the **entire P type substrate** (which is most definitely not a "columnar region", as recited in the claims) clearly is inappropriate.

Appeal No. 1996-4050
Application No. 08/410,375

Note that, as here claimed, the "third columnar regions" are **not** the P type substrate (the P type substrate extends throughout the semiconductor device, it is not in the form of "columnar regions" only where the bipolar transistors are. (Answer-page 5.)

The specification states:

The Bipolar **column**, shown at the left of Fig. 3, of the cell contains two bipolar transistors. The first bipolar transistor B1 has a surface collector region B11, a base region B12 and an emitter region B13 within the base region B12; the second bipolar transistor B2 has a surface collector region B21, a

base region B22 and an emitter region B23 within the base region B22. Both transistors have a **buried collector region** which extends below the base regions B12 and B22 respectively, as is common in integrated circuit bipolar transistor structures. The base region B22 of the second transistor B2 has an extension, a lightly doped region B24, which can act as a resistor. Finally the Bipolar **column** has a heavily doped P-type tap region T5 which makes an electrical connection to the lightly doped P-type substrate. In this embodiment the bipolar transistors are NPN-type. Thus the collector and emitter regions are N-type, and the base and resistive extension region B24 P-type. All of these collector, base and emitter regions of the two bipolar transistors are vertically aligned, together with the region B24 and the tap region T5. (Page 11, line 29-page 12, line 12.) (Emphasis added.)

We agree with Appellants that the transistor structure described supra is common in the art, and as such is presented in an enabling manner. When T5 is used to reverse bias the

Appeal No. 1996-4050
Application No. 08/410,375

lightly doped P-type substrate and N-type buried collector regions, both NPN-type transistors are electrically isolated from each other and should operate properly. The third type columnar region is clearly that, a columnar region **of the substrate** where the two bipolar transistors reside. Although the third columnar region is part of the entire substrate, this does not negate operability or enablement.

We find nothing in the claims or specification that requires the "third columnar region", recited in the claims, to be a structure separate from the substrate. We read this limitation as a particular portion, i.e., **region**, of the substrate wherein the bipolar transistor **column** resides. Consistent with this reading we find the specification to be clearly enabling, and need not reach the declarations submitted under Rule 132.

Therefore, we will not sustain the rejection of claims 1 through 20 under 35 U.S.C. § 112 as being based on a non enabling disclosure.

The decision of the examiner rejecting claims 1 through 20 is reversed.

Appeal No. 1996-4050
Application No. 08/410,375

REVERSED

James D. Thomas)	
Administrative Patent Judge)	
)	
)	BOARD OF PATENT
Kenneth W. Hairston))
Administrative Patent Judge)	APPEALS AND
)	
)	INTERFERENCES
)	
Stuart N. Hecker)	
Administrative Patent Judge)	

SH/dm

LSI Logic Corporation
1551 McCarthy Blvd., MS D-106
Milipitas, CA 95035