

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 12

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte KEVIN K. WALSH,
ROMAN KORSUNSKY
and JAMES D. REINKE

Appeal No. 96-4032
Application 08/054,496¹

ON BRIEF

Before KRASS, FLEMING and LALL, *Administrative Patent Judges*.

FLEMING, *Administrative Patent Judge*.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 7 through 14. Claims 1 through 6

¹ Application for patent filed April 26, 1993.

have been withdrawn from consideration.

The invention relates to a clock circuit for implantable medical devices. Appellants disclose on page 2 of the specification that accurate clock signals are essential for proper functioning of programmable pacemakers. On page 3 of the specification, Appellants disclose that master clock circuits for these devices are susceptible to failure because EMI and Caution can cause the master clock signal to have a too narrow signal. This narrow signal causes an operational failure of the microprocessor because the clock signal does not meet the clock duty cycle requirements.

Appellants disclose on page 3 of the specification that their invention solves this problem by providing a new subsystem block that receives the output clock signal from the master clock and generates a modified master clock signal. The function of the new subsystem block is to guarantee that the modified master clock signal delivers to the system clock signals that have a duration to ensure correct functionality of the system microprocessor. Appellants disclose on page 4 that this function is achieved by ensuring that the clock signal does not change state until the pulse generator and the system microprocessor have generated an event completion signal.

On page 8 of the specification, Appellants disclose that Figure 2 is a simplified schematic diagram of the new subsystem block 200. Appellants state that the purpose of the subsystem 200 is to lock out all transitions on the modified master clock signal MCLK 202 until the system

microprocessor (CPU) and the pulse generator (PG) have finished their instructions. Appellants further state that the function of the sub-system 200 is to prevent a noise glitch on the master clock signal from causing another operation to start before the one in process has finished.

On pages 9-11 of the specification, Appellants disclose the operation of sub-system 200 shown in Figure 2. In particular, signals 204, 206 and 208 are generated by CPU and PG. The CPURISEEN 204 signal is a signal from the CPU which is normally high except while the CPU is in the process of performing an instruction which is started on the falling edge of MCLK 202 whereby the signal is held low. The CPUFALLEN 206 signal is a signal from the CPU which is normally high except while the CPU is in the process of performing an instruction which is started on the rising edge of MCLK 202 whereby the signal is held low. The PGFALLEN 208 signal is a signal from the PG which is normally high except while the PG is processing data which is started on the rising edge of MCLK 202 whereby the signal is held low. The circuitry of Figure 2 delays the transition state of MCLK 202 until CPURISEEN 204, CPUFALLEN 206 and PGFALLEN 208 signals have all returned to the normally high state indicating that both the CPU and PG have finished and are ready to start processing another instruction.

The independent claim 7 is reproduced as follows:

7. A clock circuit for providing a main clock signal having periodic logic state transitions to an associated circuit which performs actions in response to said logic state transitions of said main clock signal and provides completion signals indicating completion of said actions performed in response to a preceding logic state transition of said main clock signal, wherein said clock circuit

comprises:

a main clock output means for providing said main clock signal to said associated circuit;

a clock signal input means for receiving an input clock signal having periodic logic state transitions;

completion signal input means for receiving said completion signals from said associated circuit;

means responsive to occurrence of a logic state transition of said input clock signal for causing a logic state transition of said main clock signal, said responsive means further comprising logic means responsive to receipt of a said completion signal indicating completion of actions performed in response to a preceding logic state transition of said main clock signal, for delaying said transition of said logic state of said main clock signal until receipt of said completion signal.

The Examiner relies on the following references:

Essig et al. (Essig)	4,745,629	May 17, 1988
Sawtell	5,227,672	July 13, 1993 (filed Mar. 31, 1992)

Claims 7 through 14 stand rejected under 35 U.S.C. § 103 as being unpatentable over Sawtell in view of Essig.

Rather than reiterate the arguments of Appellants and the Examiner, reference is made to the brief and answer for the respective details thereof.

OPINION

We will not sustain the rejection of claims 7 through 14 under 35 U.S.C. § 103.

The Examiner has failed to set forth a *prima facie* case of obviousness. It is the burden of the Examiner to establish why one having ordinary skill in the art would have been led to the claimed

invention by the express teachings or suggestions found in the prior art, or by implications contained in such teachings or suggestions. *In re Sernaker*, 702 F.2d 989, 995, 217 USPQ 1, 6 (Fed. Cir. 1983).

"Additionally, when determining obviousness, the claimed invention should be considered as a whole; there is no legally recognizable 'heart' of the invention." *Para-Ordnance Mfg. v. SGS Importers Int'l, Inc.*, 73 F.3d 1085, 1087, 37 USPQ2d 1237, 1239 (Fed. Cir. 1995), *cert. denied*, 117 S.Ct. 80 (1996) *citing* *W. L. Gore & Assocs., Inc. v. Garlock, Inc.*, 721 F.2d 1540, 1548, 220 USPQ 303, 309 (Fed. Cir. 1983), *cert. denied*, 469 U.S. 851 (1984).

Appellants argue on pages 5 and 6 of the brief that Sawtell and Essig, together or individually, fail to teach or suggest feedback from the external circuit to control the duty cycle of the main clock signal based on completion of a task triggered in response to a logic transition of the output clock signal. Appellants further argue that both references lack a teaching or a suggestion of employing a completion signal from an associated circuit indicative of completion of an action performed in response to a previous logic state transition to control the duty cycle of the clock circuit.

We note that Appellants' claim 7 recites:

a main clock output means for providing said main clock signal to said associated circuit; a clock signal input means for receiving an input clock signal having periodic logic state transitions; completion signal input means for receiving said completion signals from said associated circuit; means responsive to occurrence of a logic state transition of said input clock signal for causing a logic state transition of said main clock signal, said responsive means further comprising logic means responsive to receipt of a said completion signal indicating completion of actions performed in response to a preceding logic state transition of said main clock signal, for delaying said transition of

said logic state of said main clock signal until receipt of said completion signal.

We note that the other independent claims recite similar limitations.

Upon a careful review of Sawtell and Essig, we find that neither reference teaches the above limitations as recited in Appellants' claims. In particular, neither reference teaches means responsive to occurrence of a logic state transition of the input clock signal for delaying the transition of a logic state transition of the output clock signal until receipt of the completion signal from the associated circuit.

Sawtell teaches in Figure 2 change over apparatus 320 for selection of either external clock #1 or external clock #2 which is supplied to device 308. Sawtell does not teach that device 308 provides completion signals indicative of completion of actions performed by the device.

Essig teaches in Figure 1 a duty cycle timer 20 for a defrost heating element 22 of an associated refrigerator circuit. The duty cycle time generator 20 includes two counters 30 and 32 which provide a signal to control the relay 23 in which the relay remains off for an interval of 50 minutes and on for an interval of 30 minutes. See column 4, lines 8-21. Thus, the two counters provide a series of square waves of a duration of 10 minutes separated by an interval of 30 minutes. Essig also teaches that the duty cycle timer 20 includes a hold circuit 36 that disables the duty cycle timer when the thermostat 35 signifies the operation of the refrigeration circuit has terminated its cooling operation. See column 4, lines 40-53. Essig teaches that the hold circuit 36 is operative to suspend operation of the duty cycle timer when the refrigeration circuit is

turned off, but resumes operation of the timer from where it stopped when the refrigeration circuit is turned on.

We agree that Essig teaches delaying a transition state of the off/on signal 21, but Essig does not teach completion signals for the associated circuit, defrost element 22, or upon occurrence of a logic state transition of an input clock, delaying an output clock signal state transition until receipt of the completion signals. Thus, Essig does not teach means responsive to occurrence of a logic state transition of the input clock signal for delaying the transition of a logic state transition of the output clock signal until receipt of the completion signal from the associated circuit means responsive to occurrence of a logic state transition of the input clock signal for delaying the transition of a logic state transition of the output clock signal until receipt of the completion signal from the associated circuit as recited in Appellants' claims.

Furthermore, we fail to find any suggestion of modifying Sawtell and Essig to provide a clock circuit as recited in Appellants' claims. The Federal Circuit states that "[t]he mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." *In re Fritch*, 972 F.2d 1260, 1266 n.14, 23 USPQ2d 1780, 1783-84 n.14 (Fed. Cir. 1992), *citing In re Gordon*, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984). "Obviousness may not be

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established using hindsight or in view of the teachings or suggestions of the inventor." *Para-Ordnance Mfg. v. SGS Importers Int'l, Inc.*, 73 F.3d at 1087, 37 USPQ2d at 1239, *citing W. L. Gore*, 721 F.2d at 1551, 1553, 220 USPQ at 311, 312-13.

We have not sustained the rejection of claims 7 through 14 under 35 U.S.C. § 103.

Accordingly, the Examiner's decision is reversed.

REVERSED

ERROL A. KRASS)
Administrative Patent Judge)
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) BOARD OF PATENT
MICHAEL R. FLEMING)
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