

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today
(1) was not written for publication in a law journal and
(2) is not binding precedent of the Board.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte KEITH C. DULAC
and WILLIAM V. COURTRIGHT, II

Appeal No. 1996-3365
Application 08/258,357¹

ON BRIEF

Before THOMAS, JERRY SMITH and HECKER, **Administrative Patent Judges.**

HECKER, **Administrative Patent Judge.**

DECISION ON APPEAL

This is a decision on appeal from the final
rejection of claims 1 and 3. Claims 5 through 7 and 9 through

¹ Application for patent filed June 9, 1994. According to appellants, this application is a continuation of Application 07/701,921, filed May 17, 1991, now abandoned.

10 have been indicated as allowable. Claims 2, 4 and 8 have been canceled.

The invention relates to an apparatus for routing data between first and second bus groups. In particular, referring to Figure 1, a first group of busses 10 is coupled with a second group of busses 20. Bus switch module 40 provides a unidirectional connection between any bus of the first group and any bus of the second group. Parity information, obtained via bus 53, can be ported to any one of the busses of the second group. Parity module 50 includes input connections to each of the busses of the first group for receiving data therefrom, and an output connection to bus 53 for providing parity information to bus switch module 40. Figures 4A and 4B provide a block diagram of the internal structure of bus switch module 40. Module 40 includes six 5:1 multiplexers 141 through 146 with inputs connected to busses of the first group and the output of parity module 50. The outputs of multiplexers 141 through 146 are connected to busses of the second group.

Independent claim 1 is reproduced as follows:

1. Apparatus for selectively connecting busses within a first plurality of busses with busses within a second plurality of busses, comprising:

a first plurality of bus multiplexers including a bus multiplexer corresponding to each bus within said second plurality of busses, each one of said first plurality of bus multiplexers having an output connected to said bus multiplexer's corresponding bus and having a plurality of inputs corresponding to each bus within said first plurality of busses, each one of said inputs being connected to said input's corresponding bus; and

a parity generation circuit having an output and a plurality of inputs corresponding to each bus within said first plurality of busses, each one of said parity generation circuit inputs being connected to said one of said parity generation circuit input's corresponding bus; and

wherein each one of said first plurality of bus multiplexers has an additional input connected to the output of said parity generation circuit.

The Examiner relies on the following references:

Hillis	5,175,865	Dec. 29, 1992 (filed 7/1/91)
Callison et al.	5,206,943	Apr. 27, 1993 (filed 11/3/89)

Claims 1 and 3 stand rejected under 35 U.S.C. § 103 as being unpatentable over Hillis in view of Callison.

Rather than reiterate the arguments of Appellant and the Examiner, reference is made to the brief and answer for the respective details thereof.

OPINION

After a careful review of the evidence before us, we agree with the Appellant and will not sustain the rejection of claims 1 and 3 under 35 U.S.C. § 103.

The Examiner has failed to set forth a *prima facie* case. It is the burden of the Examiner to establish why one having ordinary skill in the art would have been led to the claimed invention by the reasonable teachings or suggestions found in the prior art, or by a reasonable inference to the artisan contained in such teachings or suggestions. *In re Sernaker*, 702 F.2d 989, 995, 217 USPQ 1, 6 (Fed. Cir. 1983). "Additionally, when determining obviousness, the claimed invention should be considered as a whole; there is no legally recognizable 'heart' of the invention." *Para-Ordnance Mfg. v. SGS Importers Int'l.*, 73 F.3d 1085, 1087, 37 USPQ2d 1237, 1239 (Fed. Cir. 1995) (*citing W. L. Gore & Assocs. v. Garlock, Inc.*, 721 F.2d 1540, 1548, 220 USPQ 303, 309 (Fed. Cir. 1983), *cert. denied*, 469 U.S. 851 (1984)).

The Examiner has cited Hillis as teaching the arrangement of busses and bus multiplexers recited in claim 1. Callison is then combined with Hillis to provide the parity

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generation circuit recited in the second half of claim 1. The Examiner states that the combination is obvious:

because it is well known in the data processing art that the parity generation circuit is used in checking for errors in groups of data bits transferred within or between computer systems and memory storage. (Answer-page 5.)

We agree with the Examiner that parity generation in computer systems is well known for checking errors. However, Appellant's claimed implementation has not been shown by Hillis and/or Callison. As with the Appellant, we fail to see the structural configuration recited in claim 1.

For example, Appellant argues:

In this manner, neither Callison nor Hillis, nor the combination thereof, provide the structure of Claim 1 -- which requires that the same plurality of inputs applied to a parity generation circuit also be inputted to a first plurality of multiplexers via a first plurality of busses. (Brief-page 9.)

In response, the Examiner states:

It is noted that Callison taught parity generation circuit check 90 (see 90, fig. 5). Hillis taught a plurality of bus multiplexers([430], fig. 5). It would have been obvious for one of ordinary skill in the data processing art at the time the invention was made that the combination

teachings of Callison and Hillis **would** arrive at the system architecture taught by the appellant. The same plurality of inputs applied to a parity generation circuit **would be inputted** to a first plurality of multiplexers via a first plurality of busses because the parity generation circuit is used to check the data it **should be connected** to an input/output for checking and determining the data is correct after the read/write operation. (Emphasis added.) (Answer-page 8.)

We fail to see, in the Examiner's explanation **supra**, the claimed structure of the same plurality of inputs applied to the parity generation circuit being inputted to the first plurality of multiplexers via the first plurality of busses, or how it would be obvious to create such a structure. The Examiner's explanation of what **would** or **should** be done is recited in generalities which do not meet the structural limitations claimed.

The Federal Circuit states that "[t]he mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." **In re Fritch**, 972 F.2d 1260, 1266 n.14, 23 USPQ2d 1780, 1783-84

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n.14 (Fed. Cir. 1992), **citing In re Gordon**, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984). "Obviousness may not be established using hindsight or in view of the teachings or suggestions of the inventor." **Para-Ordnance Mfg. v. SGS Importers Int'l**, 73 F.3d at 1087, 37 USPQ2d at 1239, **citing W. L. Gore & Assocs., Inc. v. Garlock, Inc.**, 721 F.2d at 1551, 1553, 220 USPQ at 311, 312-13.

Since there is no evidence in the record that the prior art taught or suggested the claimed structure, we will not sustain the Examiner's rejection of claim 1 and likewise claim 3 which is dependent therefrom and contains the same limitations.

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We have not sustained the rejection of claims 1 and 3 under 35 U.S.C. § 103. Accordingly, the Examiner's decision is reversed.

REVERSED

PATENT

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Administrative Patent Judge)	
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Jerry Smith)	BOARD OF
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