

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 18

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte KAZUHITO TSUCHIDA and NAOKO SUWA

Appeal No. 96-2722
Application 08/281,168¹

HEARD: August 5, 1999

Before KRASS, FLEMING, and FRAHM, Administrative Patent Judges.

FRAHM, Administrative Patent Judge.

DECISION ON APPEAL

Appellants have appealed to the Board from the examiner's final rejection of claims 1 to 53,

¹ Application for patent filed July 27, 1994. Appellants rely upon a foreign priority filing date under 35 U.S.C. § 119 of August 17, 1993.

which constitute all of the pending claims in the application before us.

BACKGROUND

The subject matter on appeal is directed to a start-up circuit for starting a bias supply circuit, and more specifically, to the integration of such a start-up circuit in a semiconductor integrated circuit (see specification, page 1). Appellants admit in the specification that the use of start-up circuits, such as shown in Figures 10 to 12, is a conventional way of starting a bias supply circuit (see specification, pages 1 to 6). Appellants recognized that a known problem in the prior art was that large resistances are needed in the start-up circuit, requiring a very large layout area (see specification, page 6).

Appellants also admit that the production of high resistances for R1 creates the need for more masking steps and increases fabrication costs. (see specification, page 6). Most significantly, appellants admit that in the preferred embodiments, "MOS transistors are used to form the start-up circuit and the circuit to be started," and that "the start-up circuit and the circuit to be started may include other insulated gate transistors which provide effects similar to those of the preferred embodiments." (Specification, pages 40 to 41).

Representative claim 1 is reproduced below:

1. A start-up circuit formed in a semiconductor integrated circuit including an insulated gate transistor of a first conductivity type and an insulated gate transistor of a second conductivity type, and connected to first and second power-supply potentials and to a circuit-to-be-started conducting a current between said first and second power-supply potentials when started for starting said circuit-to-be-started, said start-up circuit comprising:

at least one first insulated gate transistor, including at least one MOS transistor, having a gate connected to said first power-supply potential, and a source connected to said second power-supply potential, said first insulated gate transistor being producible by the process step of fabricating said insulated gate transistor of the first conductivity type and said insulated gate transistor of the second conductivity type;

diode means including a second insulated gate transistor connected in series with said first insulated gate transistor in the forward direction between said first power-supply potential and said first insulated gate transistor and having an anode and a cathode for generating a predetermined voltage drop between said anode and said cathode when it is on, a drain of the at least one first insulated gate transistor being connected to a drain of the second insulated gate transistor, said diode means being producible by the process step of fabricating said insulated gate transistor of the first conductivity type and said insulated gate transistor of the second conductivity type;

voltage drop means having a first end connected to said first or second power-supply potential and a second end connected to said circuit-to-be started and having a predetermined resistance between said first end and said second end for causing the current between said first and second power-supply potentials to flow in said circuit-to-be started when started, said voltage drop means being producible by the process step of fabricating said insulated gate transistor of the first conductivity type and said insulated gate transistor of the second conductivity type; and

switching means having an input terminal connected to said second end of said voltage drop means, an output terminal connected to said circuit-to-be started, and a control terminal connected to said cathode of said diode means for accomplishing connection/disconnection between said input terminal and said output terminal in accordance with a potential difference between said control terminal and said input terminal, said switching means being producible by the process step of fabricating said insulated gate transistor of the first conductivity type and said insulated gate transistor of the second conductivity type.

The following references, in addition to applicants' admitted prior art, are relied on by the examiner:²

² We note that while the Answer lists Aoyama et al. (U.S. Patent No. 4,504,743) and Sedra & Smith as examples to support the arguments (Answer, page 3, section 8), we note that neither the statement of the rejection in the Answer (Answer, pages 3 to 4, section 9), the statement in the Final Rejection (Final Rejection, pages 2 to 3, paragraphs 2 to 4), nor the response to arguments in the Final Rejection (Final Rejection, pages 3 to 4) expressly rely

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Whatley	4,342,926	Aug. 3, 1982
Bennett et al. (Bennett)	5,029,295	July 2, 1991
Williams et al. (Williams)	5,296,765	Mar. 22, 1994 (filed Mar. 20, 1992)

Gray and Meyer, "Analysis and Design of Analog Integrated Circuits", John Wiley & Sons, Inc., 3rd. ed., pp. 325-27 (1993).

Claims 1 to 12 and 26 to 35 stand rejected under 35 U.S.C. § 103. As evidence of obviousness, the examiner relies upon applicants' admitted prior art, Gray and Meyer, and Bennett.

Claims 13 to 25 and 36 to 46 stand rejected under 35 U.S.C. § 103. As evidence of obviousness, the examiner relies upon applicants' admitted prior art, Gray and Meyer, Bennett, and Williams.

Claims 47 to 53 stand rejected under 35 U.S.C. § 103. As evidence of obviousness, the examiner relies upon applicants' admitted prior art, Gray and Meyer, Bennett, Williams, and Whatley.

Rather than repeat the positions of appellants and the examiner, reference is made to the Briefs and the Answer for the respective details thereof.³

upon Aoyama et al. and Sedra & Smith. In explaining the rejection of claims 1 to 53 under 35 U.S.C. § 103, the examiner relies on page 308 of Sedra & Smith as proving that FET 40 is in fact a MOS transistor and states that no unexpected results would have been attained (Answer, page 7). We note that even when a reference is relied upon in a minor capacity to support a rejection, "there would appear to be no excuse for not positively including the reference in the statement of rejection." In re Hoch, 428 F.2d 1341, 1342 n.3, 166 USPQ 406, 407 n.3 (CCPA 1970). Neither Aoyama et al. nor Sedra & Smith has been positively included in a statement of the rejection, and thus we find Aoyama et al. and Sedra & Smith not to be relied upon in the rejection of claims 1 to 53.

³ We note that the Reply Brief of May 3, 1996, has been entered and considered by the examiner as per the letter from the examiner of June 4, 1996.

OPINION

In reaching our conclusion on the issues raised in this appeal, we have carefully considered appellants' specification and claims, the applied references, appellants' admitted prior art, and the respective viewpoints of appellants and the examiner. As a consequence of our review, we are in general agreement with the examiner (first Office action, pages 2 to 4) that the combination of the admitted prior art of at least Figures 10 and 12, Gray & Meyer, and Bennett would have fairly suggested the invention of claims 1 to 12 and 26 to 35 on appeal. However, because we agree with appellant (Brief, page 14; Reply Brief, pages 6 to 7) that the applied prior art fails to teach or suggest the recited inverter, we cannot sustain the rejection of claims 13 to 25 and 36 to 53 on appeal. For the reasons which follow, we will sustain the decision of the examiner rejecting claims 1 to 12 and 26 to 35 under 35 U.S.C. § 103, and we will reverse the decision of the examiner rejecting claims 13 to 25 and 36 to 53 under 35 U.S.C. § 103.

Rejection of Claims 1 to 12 and 26 to 35 Under 35 U.S.C. § 103:

Turning first to the rejection of claims 1 to 12 and 26 to 35 under § 103, we find that claims 1 to 12 and 26 to 35 on appeal would have been obvious to one of ordinary skill in the art at the time the

invention was made in light of the collective teachings of applicants' admitted prior art, Gray and Meyer, and Bennett.

We agree with the examiner (Answer, pages 5 to 6) that the ordinarily skilled artisan looking at the combined teachings and suggestions of applicants' admitted prior art, Gray and Meyer, and Bennett would have modified applicants' admitted prior art of figure 10 by replacing the resistor R1 with a FET transistor as taught by Gray and Meyer and Bennett. We also agree with the examiner (Answer, pages 5 to 6) that although the circuits of Gray and Meyer and Bennett are "upside down" with respect to prior art Figure 10, it would further have been obvious in light of applicants' admitted prior art Figure 12 (which is "right side up") to make the connections between the transistors as claimed. We note that while appellants aver that the structure and connections of the recited invention are neither taught nor suggested by Gray and Meyer and/or Bennett (Brief, pages 6 to 7), appellants have not rebutted the examiner's reliance upon Figure 12 of applicants' specification (which is admitted prior art) as teaching or suggesting the recited structure and connections.

The most critical issue in this case before us is whether or not the applied prior art would have taught or suggested replacing Figure 10's resistor R1 with MOS transistor(s) (Q8-Q10). Appellants, through their representative, admitted at the Oral Hearing of August 5, 1999, that it would have been obvious to replace resistor R1 with the FET of Gray and Meyer or Bennett. The question thus becomes whether or not it would have been obvious to use a MOS transistor. The examiner (Answer,

page 7) states that it is well known that FET's include MOS's, and that it would have been obvious to substitute different device technologies (i.e., IGFET's, JFET's, MOSFET's, BJT's, etc.). The examiner offers Sedra & Smith to show that a FET can indeed be a MOS transistor. Appellants argue (Brief, page 11) that there is no motivation for replacing the FET with a MOS, and that Sedra & Smith actually teach a bipolar transistor and not a MOS (Reply Brief, page 5).

We agree with the examiner that it would have been obvious to employ various different device technologies, and that the resulting connections would have been within the ordinary level of skill in the art. This is buttressed by appellants' admission in their specification at pages 40 to 41 that while MOS transistors are used in the start-up circuit of the preferred embodiment, the start-up circuit "may include other insulated gate transistors which provide effects similar to those of the preferred embodiments" (specification, pages 40 to 41).

We also agree with the examiner that Sedra & Smith's Figure 5.9(b) at page 308 shows a MOSFET. We conclude that it was well-known in the art at the time of applicants' invention that surface FET's include MOSFET's and other insulated gate FET's, that MOSFET's are a type of FET, and that field effect transistors (FET's) fall into two general classes: metal-oxide semiconductor (MOS) FET's, and thin-film FET's. See SEVIN, JR., *Field-Effect Transistors*, pp. 24 and 123, McGraw-Hill Book Company (1965); and RICHMAN, *MOS Field-Effect Transistors and Integrated Circuits*, pp. vii

and 1, John Wiley & Sons (1973).⁴ Accordingly, we cannot disagree with the examiner's characterization of Bennett's FET 40 as being a metal-oxide semiconductor (MOS) FET. This is especially so in light of appellants' admission at pages 40 to 41 of their specification that other types of insulated gate transistors may be used in place of MOS transistors.

We cannot agree with appellants' arguments (Brief, pages 7, 9, and 11 to 12; Reply Brief, pages 2 to 4) that claims 1 to 53 are non-obvious because the circuit elements of the claims are formed in the same fabrication step and/or because transistors Q8-Q10 are formed at the same time as Q1. Simply put, our review of the claims on appeal reveals no process claims, only apparatus claims. While claim 1 on appeal recites transistors being made by "the process step of fabricating" one type of transistor and another type of transistor, we note that the claims as broadly interpreted do not require any certain order or timing of process steps or fabrication of the circuit elements. We agree with the examiner (Answer, pages 8 to 9) that the present invention on appeal is not directed toward a process and that no specific details exist in the claims which relate to a process improvement for chip fabrication.

With respect to claims 26 to 35, appellants argue (Brief, page 13; Reply Brief, page 4) that the salient features of these claims of plural transistor gates being connected in common is neither taught nor

⁴ Copies of these references are provided as an attachment to this decision.

suggested by the applied prior art. The examiner states that Aoyama suggests connecting plural transistors in order to increase resistance (Answer, page 7), and appellants disagree (Reply Brief, page 6) stating that Aoyama fails to show gates being connected in common.

We are in agreement with the examiner that the general concept of using plural resistors/transistors connected together to achieve a higher resistance value is known in the art. We are also in agreement with the examiner that employing plural transistors to achieve a high resistance would have been obvious to one of ordinary skill in the art, especially in light of the recognition in the art (e.g., see Sedra & Smith) that it is difficult to obtain high resistance values with transistors. Because it is known to use transistors in place of resistors (see Aoyama), and because it is known to increase resistance by putting plural resistors in series, we find that it would have been obvious to increase resistance by using plural transistors as shown by Aoyama. We agree with the examiner (Answer, page 8) that the specific connections and configurations of transistor resistive elements (e.g., gates connected in common) would have been obvious to one having ordinary skill in the transistor art.

With respect to dependent claims 2 to 12 and 27 to 35, appellants rely on their arguments as to independent claims 1 and 26. Since appellants present no separate arguments as to claims 2 to 12 and 27 to 35, these claims fall with parent claims 1 and 26, discussed supra.

Rejection of Claims 13 to 25 and 36 to 53 Under 35 U.S.C. § 103:

We turn next to the question of the obviousness of claims 13 to 25 and 36 to 53 under § 103. Each of independent claims 13, 36, and 47 and their corresponding dependent claims on appeal recites the details of an inverter. More specifically, these claims call for an inverter which outputs one power-supply potential (V_{GND}) when the input potential (V_{IN}) is closer to another power-supply potential (V_{DD}) than a threshold (V_{TH}), and outputs the another power-supply potential (V_{DD}) when the input potential (V_{IN}) is closer to the one power-supply potential (V_{GND}) than the threshold (V_{TH}). See claims 13, 36, and 47 on appeal. These claims also call for a voltage drop means (resistor R_{12}) and a switching means (transistor Q_{64}).

As argued by appellants (Brief, page 14; Reply Brief, pages 6 to 7) the voltage drop means, switching means, and inverter operate in concert together to achieve an important aspect of appellants' invention of providing a high threshold voltage thereby allowing a lower resistance value (also reducing resistor size) for the voltage drop means to be used. We find that the applied prior art fails to teach or suggest such an inverter. Further, none of the prior art applied, taken singly or in combination, would have suggested modifying the applied prior art with an inverter to achieve the goal of providing a high threshold voltage and thus a low resistor value. We agree with appellants, and accordingly we cannot sustain the examiner's rejection under 35 U.S.C.

§ 103 as to claims 13 to 25 and 36 to 53.

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We find that the inverter of claims 13 to 25 and 36 to 53 is neither taught nor suggested by the applied combination of applicants' admitted prior art, Gray and Meyer, Bennett, Williams, and Whatley.

In light of the foregoing, the differences between the subject matter recited in claims 1 to 12 and 26 to 35 and the prior art are such that the claimed subject matter as a whole would have been obvious within the meaning of 35 U.S.C. § 103. Accordingly, we shall sustain the standing rejections of claims 1 to 12 and 26 to 35. We reach the opposite conclusion with respect to claims 13 to 25 and 36 to 53 which recite the details of the inverter.

CONCLUSION

The decision of the examiner rejecting claims 1 to 12 and 26 to 35 under 35 U.S.C. § 103 is affirmed.

The decision of the examiner rejecting claims 13 to 25 and 36 to 53 under 35 U.S.C. § 103 is reversed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

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AFFIRMED-IN-PART

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Administrative Patent Judge)	
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MICHAEL R. FLEMING)	BOARD OF PATENT
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