

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today
(1) was not written for publication in a law journal and
(2) is not binding precedent of the Board.

Paper No. 36

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte SHIGERU KIKUDA

Appeal No. 96-0511
Application 08/158,837¹

ON BRIEF

Before MARTIN, BARRETT, and TORCZON, Administrative Patent
Judges.

MARTIN, Administrative Patent Judge.

DECISION ON APPEAL

This is an appeal under 35 U.S.C. § 134 from the
examiner's rejection of claims 23-26, 32, 39-43, 50-52, and
53-60 under § 103. The rejection of claims 23, 25, 39-41 and

¹ Application for patent filed November 29, 1993.

55 under § 112, second paragraph was withdrawn in the Answer (at p. 2). Claims 9 and 10 have been allowed. We reverse.

The invention relates to a semiconductor memory structure that permits different test data to be written into and read out of row-adjacent memory cells in order to detect interference between those memory cells (Spec. at p. 13, lines 1-5; p. 14, lines 7-11). Figure 1 shows a semiconductor memory device of the type having a "preliminary" memory 202 with rows of memory cells which can be substituted for defective memory cells in a "normal" memory 201 (Spec. at p. 23, lines 6-12). The two memories have different word line (i.e., "word lines" WL_1-WL_m and "spare word lines" SWL_1-SWL_2) but share the same bit line pairs ($B_1/B_1-B_1/B_1$). The device shown in Figure 1 differs from the prior art by being constructed so as to permit an entire row of data to be transferred simultaneously in either direction between the preliminary memory and the normal memory during one write cycle (Spec. at p. 27, lines 3-9). Specifically,

preliminary row decoder 203b and normal row decoder 203a are controlled in response to a spare enable signal SE and an inversion signal \overline{SE} thereof, so that they can be enabled alternately. When preliminary row decoder 203b is first enabled, spare word line SWL1 or SWL2 selected

by preliminary row decoder 203b is first activated by preliminary word driver 204b, so that storage data of all the memory cells connected to the selected word line appear on corresponding bit line pairs. When normal row encoder 203b [sic, 203a] is then enabled, the normal word line selected by normal row encoder 203[a] is activated by normal word driver 204a. Accordingly, the storage data of all the memory cells connected to the selected spare word line are written into all the memory cells connected to the selected normal word line through their corresponding bit line pairs. Conversely, if normal row decoder 203[a] is first enabled, the normal word line selected by normal row decoder 203a is first activated by normal word driver 204a, and subsequently the spare word line selected by preliminary row decoder 203b is activated by preliminary word driver 204b. Thus, the storage data of all the memory cells connected to the selected normal word line appear on their corresponding bit lines during a period in which normal row decoder 203b is activated, and then written into all the memory cells connected to the selected spare word line. [Spec. at p. 26, line 2 to p. 27, line 2.]

As a result, once a test data pattern has been written (presumably serially) into a row of the preliminary memory or the normal memory, the entire row of test data can be simultaneously transferred to a selected row of the other memory (Spec. at p. 51, line 7 to p. 52, line 14; p. 59, lines 5-21).

Figure 10 shows the details of testing circuit 209, which appears in block form in Figure 1. Externally generated test data from I/O control circuit 206 (identified as 206b in Fig.

1) are applied to lines N3 and N4 of each bit line pair for writing the test data into the memory cells of a row of the preliminary memory (selected by a "spare" word line) or into the cells of a row of the normal memory (selected by a "normal" word line) (Spec. at p. 72, lines 9-18). At the same time, the test data is latched into registers 3 for each bit line pair (Spec. at p. 72, lines 19-21). Next, the word line is selected to read out the stored test data, which is then compared by match detection circuits 2 to the data values stored in respective registers 3 and the results are issued on output line DS (Spec. at p. 72, lines 21 to p. 73, line 4). Because each bit line pair has its own register 3 and match detection circuit 2, different test data can be used to test row-adjacent memory cells (Spec. at p. 73, lines 10-15). Providing plural registers for each bit line pair permits different data patterns to be used to test different rows (Spec. at 74, lines 2-9).

Figure 11 shows an alternative embodiment having two separate memories 1 and 2 of normal memory cells and associated memories 11 and 13 of preliminary memory cells. Identical test data are written into one or more rows of

preliminary memory cells in both preliminary memories 11 and 13). Next, the test data are simultaneously transferred from the memory cells of one row of preliminary memory 11 to the memory cells of one row of normal memory 1. At the same time, data are simultaneously transferred from the memory cells of in one row of the other preliminary memory (13) to the memory cells in one row of the other normal memory (2). The test data stored in the two rows of the normal memories are then simultaneously read and compared with each other to determine whether or not there is a defect in one of the rows of either normal memory.

There are five independent claims before us: claims 23, 24, 32, 52, and 53. Independent claims 23 and 25, which correspond respectively to the two embodiments described above, read as follows:

23. A semiconductor memory device comprising:

and of a plurality of memory cells connected to word lines and bit lines and arranged in a matrix in the direction of rows and the direction of columns;

a plurality of preliminary memory cells connected to preliminary word lines and said bit lines and arranged in a matrix in said direction of rows and said direction of columns;

means for writing predetermined external data for functional testing of said plurality of memory cells into each single row of said plurality of preliminary memory cells;

means for temporarily storing said external data written by said writing means;

means for simultaneously transferring said external data in each single row of said preliminary memory cells connected to one of said preliminary word lines to a corresponding single row of said plurality of memory cells connected to one of said word lines via said bit lines connecting said plurality of memory cells and preliminary memory cells;

means for simultaneously reading data from each single row of said plurality of memory cells; and

means for simultaneously comparing all of said data read by said reading means with all of said external data temporarily stored in said temporarily storing means via bit lines connecting said plurality of memory cells and preliminary memory cells, to detect whether or not there is a defect in any of the rows of said plurality of memory cells.

25. The semiconductor memory device according to claim 23, wherein

means for simultaneously comparing comprises for comparing all of said read data and all of said temporarily stored external data in the correspondence of one to one

We note that although all of the appealed claims include limitations which appear to be in proper means-plus-function

Appeal No. 96-0511
Application 08/158,837

and are thus entitled to be construed in accordance with § 112 ¶ 6, Appellants do not rely on § 112 ¶ 6 to distinguish these limitations from the prior art.

The references relied on by the examiner are as follows:

Tanigawa	4,888,772	Dec. 19, 1989
Childers	4,670,878	Jun. 2, 1987
Furutani et al.	4,817,056	Mar. 28, 1989

Claims 23-26, 32, 39, and 53 stand rejected under § 103 as unpatentable over Tanigawa in view of Childers. Claims 40-43, 50-52, and 54-60 stand rejected under § 103 as unpatentable over Tanigawa in view of Childers and Furutani.

Tanigawa discloses a memory testing circuit that permits complementary test data to be used to test adjacent memory cells for interference defects in a memory has two memory parts 10a and 10b (col. 11, lines 64-68). Referring to Figure 1A, a single column select signal (e.g., CS1) issued by column address decoder 14 closes four selector switches (S_{11} , S_{12} , S_{21} , S_{22}), thereby connecting four bit lines (D_{11} , D_{12} , D_{21} , D_{22}) to data buses DB1, DB2, DB3, and DB4. Figure 1C shows the circuitry for controlling the writing of data into and reading of data from the memories.

Appeal No. 96-0511
Application 08/158,837

For data other than test data, this circuitry writes into and reads from one memory cell at a time, using a selected one of data buses DB1-DB4 (see, e.g., col. 6, lines 41-54; col. 7, lines 4-11). The memory testing circuitry shown in Figure 1B, which is rendered operative by a high test enable signal TE (col. 12, lines 1-8), uses all four data buses at once to simultaneously write test data into and then to simultaneously read the stored data from four memory cells (col. 2, lines 40-48). This circuitry includes circuit elements 56, 58 and 50 for generating complementary test data values to be applied to data buses DB1-DB4. Element 56, which is shown in detail in Figure 3, generates at each of four output terminals TI1-TI4, a voltage representing the input test data (col. 14, line 63 to col. 15, line 5). Terminals TI2 and TI4 are directly connected to data buses DB2 and DB4, respectively, whereas terminals TI1 and TI3 are connected to data buses DB1 and DB3, respectively, through inverters 58 and 60. As a result, the test data values on buses DB1 and DB2, which are to be applied to a pair of row-adjacent memory cells in memory 10a, are complementary, as are the test data values on DB3 and DB4, to be applied to a pair of row-adjacent memory cells in memory

10b. These complementary data values permit testing for interference between the cells in each memory (col. 2, line 68 to col. 3, line 6). During the testing mode of operation, the four test data values are written simultaneously into all four memory cells (col. 2, lines 40-48). The stored data values are then read out simultaneously, with the values on data buses DB2 and DB4 being directly coupled to terminals T02 and T04 of circuit 62 and with the values on DB1 and DB3 being coupled to terminals T01 and T03 via inverters 64 and 66 (Fig. 1B) so that the voltages at all four terminals will have the same value if no memory cell is defective. Referring to Figure 5, which shows the details of circuit 62, the data on terminals T01-T04 (T02 and T04 are identified as DB2 and DB4 in the figure) and their complements are compared to determine whether the data on terminals T01-T04 is all the same; if they are not, a high level signal appears at the output of the circuit (col. 19, line 67 to col. 20, line 8). The foregoing process is then repeated for each remaining group of four memory cells (col. 22, lines 8-40).

Comparing claim 23 to Tanigawa, the examiner appears to read

the claimed "plurality of memory cells" and the claimed "plurality of preliminary memory cells" onto Tanigawa's memories 10a and 10b, respectively. Appellant does not contend that Tanigawa fails to satisfy these limitations. The examiner reads the claimed "means for writing predetermined external data for functional testing of said plurality of memory cells into each single row of said plurality of preliminary memory cells" onto Tanigawa's data write control circuit (Fig. 1C), which appears to be reasonable to us, because it writes test data into a pair of elements in a row of preliminary memory elements (10a) and the language "writing . . . into each single row of said plurality of preliminary memory cells" does not require writing into more than one row of preliminary elements or writing into every memory cell in a row of preliminary elements. Regarding the claimed "means for temporarily storing said external data written by said writing means," the examiner argues (Answer at 3-4 and 9) that such storing means is inherent in Tanigawa because of his disclosure that the output data from data output buffer 36 is applied to an output terminal 38 of the chip and "is sent out from the chip as an output signal D_{out} for comparison with the

Appeal No. 96-0511
Application 08/158,837

original input data signal D_{IN} " (col. 7, lines 11-17). The meaning of this passage in Tanigawa is unclear, because Tanigawa's drawings and detailed description of the testing procedure nowhere show or describe a comparison of D_{out} with D_{IN} . Instead, as noted above, Tanigawa detects defective memory cells by examining the voltages at terminals T01-T04 (Fig.5), all of which are derived from the fetched data appearing on DB1-DB4, to determine whether they are all the same; if they are not, there is a defect in one of the four memory cells being tested. For this reason, Tanigawa does not inherently employ "temporarily storing" means for holding the test data until it can be compared to the fetched data, as required by claim 23. As will appear, neither this deficiency in Tanigawa nor the other deficiencies discussed below are remedied by Childers or Furutani.

The examiner concedes that Tanigawa fails to disclose claim 23's "means for simultaneously transferring said external data in each single row of said preliminary memory cells . . . to a corresponding single row of said plurality of memory cells . . . via said bit lines connecting said plurality of memory cells and preliminary memory cells." For

this teaching, the examiner cites Childers, which discloses a semiconductor memory which is constructed to allow high speed testing to identify row line faults in one example and column or sense amplifier faults in another example without requiring the access of the cells in the array in complex data patterns (col. 1, lines 57-63). The memory array is divided into four memory blocks 101, 10b, 10c, and 10d (Fig. 1). Figure 6 shows circuitry for identifying open circuits in row lines 34 and shorts between row lines (col. 6, lines 10-53). Figure 7, on which the examiner relies, shows circuitry for identifying column or sense amplifier faults. Each of the sense amplifiers 26 is connectable to its corresponding pair of bit lines 33 by transistors 75 and 76 (operable by voltage T) and is also connectable to an adjacent set of bit lines by transistors 75' and 76' (operable by voltage T'). As a result, the same sense amplifier can be selectively connected with either set of bit lines to aid in isolating a column fault (col. 6, line 54 to col. 7, line 16). Another mode of test operation using the Figure 7 circuitry is to write a data pattern into the first row in the array, then repeat this pattern in all 512 other rows without using a complete writing

cycle by shifting the data along the columns using the coupling transistors T' (col. 7, lines 17-21). This may be done by using the on-chip refresh address counter to cycle through the 512 row addresses, while applying externally generated column addresses in a short cycle, or column addresses from an on-chip column address counter (col. 7, lines 21-26). A clearer description of this procedure appears in Childers' claim 14, which reads as follows:

14. A method of writing data into a semiconductor device containing an array of rows and columns of memory cells, comprising the steps of:

writing a data pattern to one of said columns by sequentially addressing said rows while coupling data bits to the columns from a terminal of the device, then writing said data pattern to all other columns of said device by sequentially addressing said rows while coupling said one column to a first adjacent column, then coupling said first adjacent column to a second adjacent column, until all columns are written into. [Emphasis added.]

The sequential addressing of the rows means that the data pattern is not simultaneously transferred from column to another, as the examiner contends (Answer at 11). Therefore, even assuming it would have been prima facie obvious to modify Tanigawa's memory device somehow to employ Childers' column-to-column data pattern transfer technique to shift a data pattern from a row in one of memories 10a and 10b to a row in the other memory, the resulting data transfer would not occur simultaneously, as required by claim 23 and the other independent claims on appeal (i.e., claims 24, 32, 52, and 53). Furthermore, a prima facie case for obviousness has not been established with respect to any of the appealed claims, because the examiner has not adequately explain why one skilled in the art would have been motivated to replace Tanigawa's writing technique, which does not involve transferring test data between memory cells or groups of memory cells (either simultaneously or sequentially), with Childers' technique of sequentially transferring test data between memory cells (column to column). Nor has the examiner adequately explained how Tanigawa's memory device is to be modified to employ Childers' transfer technique, as is

Appeal No. 96-0511
Application 08/158,837

necessary to determine whether the claims can be read on the resulting device.

Regarding claim 23, we also note that Childers does not disclose comparing fetched data with a temporarily stored version of the test data, as required by that claim. Childers does not explain how the fetched data is to be analyzed. Also, neither Tanigawa nor Childers suggest comparing data fetched from one row with data fetched from another row, as required by independent claims 24, 32, and 52.

For the foregoing reasons, the rejection of the independent claims 23, 24, 32, and 53 under 35 U.S.C. § 103 as unpatentable over Tanigawa in view of Childers is reversed, as is the rejection of dependent claims 25, 26, and 39, which also stand rejected over those references. The rejection of independent claim 52 and dependent claims 40-43, 50, 51, 59, and 60 under § 103 as unpatentable over Tanigawa in view of Childers and Furutani is reversed because the deficiencies described above are not remedied by Furutani.

Appeal No. 96-0511
Application 08/158,837

REVERSED

)	
JOHN C. MARTIN)	
Administrative Patent Judge)	
)	
)	
)	BOARD OF PATENT
LEE E. BARRETT)	
Administrative Patent Judge)	APPEALS AND
)	
)	INTERFERENCES
)	
RICHARD L. TORCZON, JR.)	
Administrative Patent Judge)	

Appeal No. 96-0511
Application 08/158,837

DYM

Lowe, Price, Leblanc & Becker
Suite 300, 99 Canal Center Plaza
Alexandria, VA 22314