

**THIS OPINION WAS NOT WRITTEN FOR PUBLICATION**

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 31

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES

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Ex parte LEE W. ATKINSON

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Appeal No. 1996-0347  
Application No. 08/166,609<sup>1</sup>

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ON BRIEF

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Before THOMAS, KRASS and HECKER, Administrative Patent Judges.  
KRASS, Administrative Patent Judge.

**DECISION ON APPEAL**

This is a decision on appeal from the final rejection of claims 1 through 22, all of the claims pending.

The invention is directed to reducing computer system power consumption. More particularly, the computer operating

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<sup>1</sup> Application for patent filed December 13, 1993. According to appellant, this application is a continuation of Application No. 07/809,301 filed December 17, 1991, now abandoned.

Appeal No. 1996-0347  
Application No. 08/166,609

frequency is lowered when high operating speed is not needed in order to conserve power. The frequency adjustment is based on computer activity which is monitored by counting events indicative of such activity. For example, the cache hit rate may be monitored and the frequency of the system clock reduced when the cache hit rate is above a predetermined level.

Representative independent claim 1 is reproduced as follows:

1. An apparatus for use with a computer system for reducing power consumption of the computer system, comprising:

a processor having a clocking input;

memory coupled to said processor;

means for producing a clocking signal having a frequency;

a counter coupled to said processor for counting a number of events indicative of activity of the computer system during a preset period of activity of said processor;

means coupled to said counter for periodically reading the number of events counted by said counter;

means coupled to said periodic reading means and said clocking signal producing means for adjusting the frequency of the clocking signal based on the counted number of events; and

means coupled to said adjusting means for outputting the frequency adjusted clocking signal to said processor clocking input.

Appeal No. 1996-0347  
Application No. 08/166,609

The examiner relies on the following references:

Juzswik et al. (Juzswik) 6, 1987	4,698,748	Oct.
Branson 1989	4,819,164	Apr. 4,

Intel Corporation (Intel), "System and Power Management,"  
Chapters 6 and 14, 386 SL Microprocessor Superset, Programmers  
Reference Manual (1990) pp. 6-1 to 6-50, 10-4 to 10-7 and 14-1  
to 14-23.

Claims 1 through 22 stand rejected under 35 U.S.C. 103 as  
unpatentable over Intel in view of Juzswik. In the principal  
answer, the examiner entered three new grounds of rejection,  
holding claims 1 through 6 and 13 through 18 unpatentable  
under 35 U.S.C. 103 over Intel in view of Branson, holding  
claims 11 and 12 unpatentable under 35 U.S.C. 103 over Branson  
in view of Intel, and holding claims 7 through 10 and 19  
through 22 anticipated under 35 U.S.C. 102(b) over Branson.

Reference is made to the briefs and answers for the  
respective positions of appellant and the examiner.

OPINION

We reverse.

Appeal No. 1996-0347  
Application No. 08/166,609

The examiner applies Intel for the teaching of a processor, a memory coupled thereto, production of a clock signal and the adjustment of a frequency. The teaching of a frequency adjustment is taken from page 14-15 of the reference, wherein it is stated, "In CMOS devices power consumption is closely related to clock speed. In a typical CMOS system fifty to seventy percent of the system power can be controlled by adjusting the clock speed."

The examiner recognizes that Intel does not teach a counter for counting a number of computer events and, so, turns to secondary references, Juzswik and Branson to supply such a teaching.

With regard to the first rejection of claims 1 through 22 under 35 U.S.C. 103, the examiner relies on Intel in view of Juzswik. However, while the examiner relies on Juzswik for teaching the counting of a number of events and means coupled to the counter for reading the number of events, Juzswik clearly does not count any events indicative of computer activity. Juzswik is directed to power conservation and switches between a sleep mode and an active mode. However, the clock in Juzswik appears to count a time period, the

Appeal No. 1996-0347  
Application No. 08/166,609

number of pulses provided by an oscillator. The frequency of the clock in Juzswik is not adjusted, as in the instant claimed invention. As pointed out by appellant, at page 8 of the principal brief, Juzswik does not count events from the processor but, rather, the timer therein sends interrupts to the processor.

Moreover, in response to appellant's argument that Juzswik does not adjust the frequency of the clock, the examiner states that it is Intel which provides this teaching. However, if Juzswik does not provide for an adjustment of clock frequency and Intel does not recognize a need to count computer events, even assuming, arguendo, that the examiner's observations regarding these references are correct, there would appear to be no motivation for combining the teachings of the references since the skilled artisan would have been led by nothing in the applied references to modify Intel by providing for clock frequency adjustment therein based on a count of computer events, as claimed.

Therefore, we will not sustain the rejection of claims 1 through 22 under 35 U.S.C. 103 based on Intel and Juzswik.

Appeal No. 1996-0347  
Application No. 08/166,609

We now turn to the rejections based on Branson (or Branson in combination with Intel). The examiner applies Branson for the same reason Juzswik was applied, that is, to supply a teaching of a counter coupled to a processor for counting a number of events.

We agree with appellant that Branson suffers from the same deficiency as Juzswik, i.e., there is no count of a number of computer events, as claimed. Branson counts cycles of an oscillator but this is not indicative of any computer activity. As appellant explains, at page 5 of the initial reply brief, "events indicative of activity in Branson are the requests to gate network 72 by the Branson CPU 12 for access to a particular chip. These are **not** counted." Thus, combining Branson with Intel would not result in the instant invention as claimed.

Moreover, at column 10, lines 50-51 of Branson, it is recited that the "five bit counter **56**, counter **38** and flip-flop **40**, will always count an odd number of counts." If the count is always set to some odd number, it appears that Branson cannot adjust the frequency of the clocking signal

Appeal No. 1996-0347  
Application No. 08/166,609

"based on the counted number of events." Further, the counting in Branson is for synchronization purposes (column 10, lines 12-14: "The counting sequence of the counter **38** and the flip-flop **40** is synchronous with respect to the 5 MHz clock which is inverted by the NAND gate **50**"). Thus, the frequency of the clock in Branson is not adjusted based on a number of counted computer events, such as the number of times a particular chip is accessed by the CPU. Branson also does not count a number of main memory cycles as required by instant claims 13 and 19.

Still further, even if Branson disclosed the counting of a number of computer events, we remain unconvinced by any reasoning of the examiner as to why the artisan would have been led to use such a count as a basis for adjusting the clock frequency in Intel.

Thus, we will not sustain the rejection of claims 1 through 6 and 13 through 18 under 35 U.S.C. 103 based on Intel and Branson.

For the reasons supra, we also will not sustain the rejection of claims 7 through 10 and 19 through 22 under 35

Appeal No. 1996-0347  
Application No. 08/166,609

U.S.C. 102(b) based on Branson since independent claims 7 and 19 also require the adjustment of clocking frequency based on a counted number of events indicative of the activity level of the computer system during a preset period [claim 7] or of the counted number of main memory cycles [claim 19]. The rejection of dependent claims 11 and 12 under 35 U.S.C. 103 based on Branson and Intel will fall with the rejection under 35 U.S.C. 102(b) since Intel does not provide for the deficiencies of Branson.

We have not sustained the rejection of claims 7 through 10 and 19 through 22 under 35 U.S.C. 102(b) or the rejections of claims 1 through 22 under 35 U.S.C. 103.

Appeal No. 1996-0347  
Application No. 08/166,609

Accordingly, the examiner's decision is reversed.

**REVERSED**

JAMES D. THOMAS	)	
Administrative Patent Judge	)	
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	)	BOARD OF PATENT
ERROL A. KRASS	)	APPEALS
Administrative Patent Judge	)	AND
	)	INTERFERENCES
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STUART N. HECKER	)	
Administrative Patent Judge	)	

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Appeal No. 1996-0347  
Application No. 08/166,609

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