

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 20

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte ROBERT E. STEWART,
TIMOTHY E. LEONARD
and SHERRY TSI-CHUAN LEE

Appeal No.96-0258
Application 08/094,651¹

ON BRIEF

Before KRASS, BARRETT and CARMICHAEL, Administrative Patent Judges.

KRASS, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 13 through 15, the only claims pending in the application.

¹ Application for patent filed July 19, 1993. According to appellants, this Application is a continuation of Application 07/807,950, filed December 10, 1991, now U.S. Patent No. 5,239,635, granted August 24, 1993, which is a continuation of Application 07/202,886, filed June 6, 1988, now abandoned.

The invention pertains to page tables in a virtual memory. More particularly, a mechanism is provided to translate virtual addresses to physical addresses by using the virtual addresses of page table entries. A page table prototype value, representative of an offset between the physical address and the virtual address of any particular page table entry, is stored in a register. Because consecutive pages of the page table in virtual memory reside in consecutive page frames in physical memory, the page frame number of the page table entry prototype is equal to the page frame number of the first page of the page table minus the virtual page number of the first page of the page table. The page frame number of the page table entry prototype is a fixed offset which may be added to the virtual page number of the virtual address of any one particular page table entry to yield the page frame number of the physical address of the particular page table entry.

Representative independent claim 13 is reproduced as follows:

13. A method for loading a translation buffer of a computer system, which computer system includes a virtual memory space having data referenced by virtual addresses and a physical memory space having data referenced by physical addresses; certain ones of the virtual addresses each having a corresponding physical address, the translation buffer being loaded with predetermined portions of preselected virtual addresses and predetermined portions of corresponding physical addresses, the method comprising the steps of:

a) providing a page table memory space in the physical memory space, the page table memory space being referenced by physical addresses which locate locations containing at least a page table entry for a preselected page of the virtual memory space, the page table entry indicating a physical address of the preselected page of the virtual memory space;

b) the page table memory space further referenced by a set of virtual addresses,

which correspond to the physical addresses, for referencing the page table memory space;

c) providing a page table prototype mechanism including known cross reference information between the set of virtual addresses, and the corresponding physical addresses for referencing the page table memory space, the known cross-reference information comprising offset information between the certain ones of the virtual addressees and their corresponding physical addresses;

d) operating the computer system to load information identical to a preselected portion of the page table memory space into the translation buffer, which loading of the translation buffer is implemented by utilizing the page table prototype mechanism to dynamically generate physical address information for referencing the page table memory space from a corresponding one of the set of virtual addresses and the known cross reference information contained in the page table prototype mechanism.

The examiner relies on the following reference:

Sawada et al. (Sawada)	4,628,451	Dec. 9, 1986
------------------------	-----------	--------------

Claims 13 through 15 stand rejected under 35 U.S.C. § 103 as unpatentable over Sawada.²

Reference is made to the brief and answer for the respective positions of appellants and the examiner.

² A rejection of the claims under double patenting of the obviousness type has been withdrawn by the examiner in view of an acceptable terminal disclaimer and is no longer before us on appeal.

OPINION

We will reverse as the examiner has clearly failed to present a prima facie case of obviousness with regard to the claimed subject matter.

The examiner applies Sawada to the instant claims as set forth on pages 4-7 of the answer and then admits [answer, page 7] that Sawada does not expressly disclose the page table prototype mechanism including the “offset information” limitation for providing known cross-reference information between the virtual to physical addresses. The examiner contends, however, that the table look-up mechanism 12 of Sawada “performs the substantially identical claimed function of providing cross reference between the virtual to physical address information” [answer-page 7]. Apparently, the examiner bases this finding on the disclosure, by Sawada, at column 4, lines 3-5, that “the desired page is searched in the address translation table 3 stored in the main memory with the aid of a table look-up mechanism 12...” Therefore, the examiner concludes, at page 8 of the answer, “it would have been obvious...to use a specific type of information such as offset information for referencing virtual to physical addresses in the Sawada’s system.”

The mere fact that the look-up table 12 in Sawada “aids” in the translation of

logical addresses to real addresses does not, necessarily, lead to a teaching of providing the “offset information” claimed. We agree with appellants [page 13 of the brief] that claim 13 does not merely provide cross reference between the virtual to physical information but, rather, it recites “providing a page table prototype mechanism including known cross-reference information...comprising offset information...” We find no such teaching or suggestion in Sawada. The claimed offset information is used to derive physical address information from virtual address information. There is nothing in Sawada to suggest that the type of “aid” offered by the table look-up is offset information used to derive a physical address from a virtual address. The table look-up mechanism 12 of Sawada does not even appear, from Figure 3, to receive physical address information, receiving, instead, the output of comparison circuit 5 which receives, in part, information from the logical, or virtual, address register 1. Therefore, it is difficult to see how Sawada can be said to suggest the provision of a page table prototype mechanism including known cross-reference information comprising offset information between certain ones of the virtual addresses and their corresponding physical addresses, as claimed.

Independent claim 14 contains similar language.

The examiner's response to appellants' arguments includes statements that appellants' arguments lack supporting facts in that appellants point out the claimed limitations "*without supporting why the reference does not teach the claimed limitation*" [answer-pages 8-9]. The initial burden is on the examiner to establish, with evidence, that the claimed subject would have been obvious within the meaning of 35 U.S.C. § 103. Until the examiner establishes a prima facie case of obviousness, Appellants are under no burden to show why the reference does *not* teach the claimed invention.

Further, the examiner responds to appellants' arguments as to why the instant claimed invention patentably distinguishes over Sawada by contending that the use of "known cross-reference information comprising offset information between the certain ones of the virtual addresses and their corresponding physical addresses" was well known to artisans. In support of this allegation, the examiner identifies three U.S. Patents [Anthony and Ozawa at page 9 of the answer and Chang at page 11 of the answer]. If the examiner is relying on these references in any way to support the rejection, there would

Appeal No. 96-0258
Application 08/094,651

appear to be no excuse for not positively including the references in the statement of the rejection. In re Hoch, 428 F.2d 1341, 1342 n.3, 166 USPQ 406, 407 n.3 (CCPA 1970).

Accordingly, we will not consider these references.

The examiner's decision rejecting claims 13 through 15 under 35 U.S.C. §103 is reversed.

REVERSED

ERROL A. KRASS)	
Administrative Patent Judge)	
)	
)	
LEE E. BARRETT)	BOARD OF PATENT
Administrative Patent Judge)	APPEALS AND
)	INTERFERENCES
)	
JAMES T. CARMICHAEL)	
Administrative Patent Judge)	

Appeal No. 96-0258
Application 08/094,651

DIGITAL EQUIPMENT CORPORATION
PATENT LAW GROUP
111 POWDERMILL ROAD - MS02-3/G3
MAYNARD, MASS. 01754-1499