

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 20

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte JEFFREY A. SPROUSE
and WALTER E. GIBSON

Appeal No. 96-0166
Application 08/083,419¹

ON BRIEF

Before BARRETT, FLEMING, and DIXON, Administrative Patent Judges.

BARRETT, Administrative Patent Judge.

DECISION ON APPEAL

¹ Application for patent filed June 28, 1993, entitled "System And Method For Performing Improved Pseudo-Random Testing Of Systems Having Multi Driver Buses."

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This is a decision on appeal under 35 U.S.C. § 134 from the examiner's final rejection of claims 1-20. The amendment received March 27, 1995, (Paper No. 12) has been entered.

We reverse.

BACKGROUND

The disclosed invention is directed to a system and method for performing pseudo-random scan testing of systems that have individual subsystems interconnected by a shared bus.

Claim 1 is reproduced below.

1. Apparatus for permitting scan testing of a digital system of a type having at least two digital units coupled to a bus means that is shared by the two digital units for communication of information therebetween on a mutually exclusive basis during a normal mode of operation, each one of the two digital units including bus enable means coupling each of the two digital units to the bus means, the scan testing being conducted during a test mode of operation by a scan control means coupled to the digital system for placing the digital system in a pseudo-random state, the apparatus comprising:

circuit means associated with each of the two digital units, and coupled to the scan control means, for receiving a predetermined test pattern;

means coupled to the scan control means and responsive to a test signal from the scan control means to couple the circuit means to the bus enable means to ensure that only one of the bus enable means is coupled

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to the bus means at any moment in time during the test mode of operation.

The examiner relies on the following reference:

Powell et al. (Powell) 4,701,921 October 20,
1987

Claims 1-11 and 13-20 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Powell.

Claim 12 stands rejected under 35 U.S.C. § 103 as being unpatentable over Powell.

We refer to the Examiner's Answer (Paper No. 13) (pages referred to as "EA__") for a statement of the examiner's position and to the Brief (Paper No. 11) (pages referred to as "Br__") for a statement of the appellants' position.

OPINION

"Anticipation is established only when a single prior art reference discloses, expressly or under principles of inherency, each and every element of a claimed invention." RCA Corp. v. Applied Digital Data Systems, Inc., 730 F.2d 1440, 1444, 221 USPQ 385, 388 (Fed. Cir. 1984).

The examiner's interpretation of Powell is inconsistent with the limitations of the claims and fails to establish a prima facie case of anticipation for the independent claims.

Claims 1-3 and 18-20

Claim 1 recites "a digital system of a type having at least two digital units coupled to a bus means that is shared by the two digital units for communication of information therebetween on a mutually exclusive basis during a normal mode of operation" (emphasis added). Powell states (col. 4, lines 20-23): "To provide for interface between the modules in the operational mode, an operational bus 27 is provided for carrying signals between various modules." The modules in Powell are configured to provide a defined test boundary for the functional logic when in the test mode (col. 4, lines 40-42): "When this test boundary is defined, the module under test is operationally isolated from the other modules by isolating the input/output of bus 27." Only one of the modules is selected at a time by the address decode/select circuit in the test mode (e.g., col. 6, lines 51-52). Powell also states (col. 4, lines 5-8): "It should be understood that the buses 12, 16, and 20 are only interfaced with the device pins 14, 18 and 24, respectively, during the test mode." Thus, the "bus means" in claim 1 must be read on bus 27 in Powell because it is active during the operational

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(normal) mode and the internal buses 12, 16, and 18 are not. The examiner's rejection, which relies on internal buses 12, 16, and 18 as the "bus means" is inconsistent with the language of claim 1. The rejection of claim 1 and dependent claims 2, 3, and 18-20 is reversed.

Although we have reversed the rejection of claim 1, we address two of appellants' arguments for completeness. Appellants argue that "[i]t follows from a reading of Powell et al. that the modules are incapable of communicating among themselves as in the environment of Applicants' invention during test mode" (Br9) and that "['] ... [t]he present invention permits the bus access circuitry of each subsystem, and the bus itself, to be tested by pseudo-random scan testing methodology without restricting bus access to only one subsystem, and distributing that access during the test to all subsystems'" (Br10, citing the specification, page 4). Thus, appellants argue that claim 1 requires that the units communicate over the bus during the test mode. The examiner correctly discusses (EA8-9) that communication among the units via the bus during the test mode is not claimed, expressly or impliedly. Claim 1 recites that "only one of the bus enable

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means is coupled to the bus means at any moment in time during the test mode of operation." Such language includes, but does not require communication between digital units during a test mode using the bus means. Nor does any other claim language require communication between units during the test mode.

Appellants also argue that "assuming arguendo the correctness of position that the 'multiplex gates' 48/50 and the 'address decode/select circuit' 52 of Powell et al. correspond to the 'circuit means' and 'bus enable means' of Applicants' claim 1, Applicants are unable to find anything in Powell et al. corresponding to the 'means coupled to the scan control means and responsive to a test signal from the scan control means to couple the circuit means to the bus enable means to ensure that only one of the bus enable means is coupled to the bus at any moment in time'" (Br10). The examiner finds that "the 'address decode/select circuit' is the 'coupling means' which controls which module is connected to the bus through the use of the multiplex gates and ensures that 'the module under test is operationally isolated from the other modules'" (EA10). This interpretation does not fit the claim language. The shift register latches (SRLs) 34, 35, 38,

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40, which the examiner finds to be the "circuit means," are always coupled to the multiplex gates 48, 50, which the examiner finds to be "bus enable means." They are not coupled to gates 48, 50 by the address decode/select circuit 52 "responsive to a test signal from the scan control means," as claimed. If claim 1 recited coupling the circuit means to the "bus means" instead of to the "bus enable means," this would be a different issue. This is an additional reason why the rejection of claims 1-3 and 18-20 must be reversed.

Claim 4

Claim 4 recites "digital signals being coupled to the shared bus means by circuit means enabled by the assertion of an enable signal" and a "counter means, associated with circuit means of each of the digital units ... for producing a test enable signal" and "means for presetting the counter means with a predetermined test pattern." Claim 4 does not recite that the shared bus means is operative during a normal mode.

Appellants argue that Powell does not teach "counter means" and it follows that it cannot have "means for presetting the counter means" (Br11). The examiner finds that

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"counter means" reads on the SRLs disclosed at column 6, lines 31-36, of Powell (EA4) because the SRLs form a string of registers like appellants' ring counter 54 and are loaded with a predetermined test pattern (EA10). The examiner's interpretation of Powell does not fit the claim language.

The SRLs in Powell do not perform any counting function. Appellants' ring counter or circular shift register 54 performs a counting function because the predetermined test pattern includes only one "1" in the shift register, which is circulated through the register one step for each cycle (count). The SRLs hold arbitrary test vectors, which are unrelated to any counting function. That the SRLs may resemble appellants' ring counter 54 does not make the SRLs a counter. Furthermore, the output of the last SRL 40 is merely digital data and is not a "test enable signal" as claimed. The claimed "enable signal" is a signal which activates "circuit means" to couple digital signals to a shared bus; the "test enable signal" performs the same function in a test mode. The enable signal in Powell is the input to multiplex gate circuits 48, 50, which is produced by the address decode/select circuit 52, not the output of SRL 40. Because

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Powell does not disclose a "counter means" which produces a "test enable signal," the rejection of claim 4 is reversed.

In addition, appellants argue that "Powell et al. teaches nothing corresponding to Applicant's 'means ... for communicating ... [a] test enable signal from each of the counter means to each associated circuit means in place of ... [an] enable signal" (Br12). A similar limitation is found in claims 6 and 13. The examiner addresses this limitation in connection with claim 13, where the examiner finds "selecting the test signal in place of the enable signal when in the test mode in column 4 lines 11-42" (EA6). We find nothing in the referred to portion of Powell that teaches substitution of an "enable signal" with a "test enable signal," regardless of the names they might be called by in Powell. While the signals applied by the address decoder/select circuit 52 in Powell could be termed "test enable signals," they do not substitute for "enable signals" and also are not produced by a "counter means." Because Powell also does not disclose substituting a "test enable signal" for an "enable signal," the rejection of claim 4 is reversed for this additional reason.

Claim 5

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We will reverse the rejection of claim 5 because we find that Powell does not disclose the claimed step of "providing a counter means for each of the digital subsystems for providing a test enable signal that is coupled to the driver enable circuitry of each digital subsystem," as discussed with respect to the "counter means" and "test enable signal" limitations in claim 4.

Claims 6-12

We will reverse the rejection of claims 6-12 because we find that Powell does not disclose "a digital counter presettable to a predetermined state, and producing a test enable signal," as discussed with respect to the "counter means" and "test enable signal" limitations in claim 4, and because we find that Powell does not disclose "a selector coupled to receive the bus enable signal and the test enable signal to substitute the test enable signal for the bus enable signal during testing," as discussed with respect to the "means ... for communicating the test enable signal ... in place of the enable signal" limitation in claim 4.

Claims 13-17

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We will reverse the rejection of claims 13-17 because we find that Powell does not disclose a "bus enable signal" and a "test enable signal," where the method includes the step of "selecting the test enable signal in place of the bus enable signal when a test signal is asserted," as recited in claim 13, as discussed with respect to the "means ... for communicating the test enable signal ... in place of the enable signal" limitation in claim 4.

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CONCLUSION

The rejections of claims 1-20 are reversed.

REVERSED

LEE E. BARRETT)	
Administrative Patent Judge)	
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)	BOARD OF PATENT
MICHAEL R. FLEMING)	APPEALS
Administrative Patent Judge)	AND
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